JPE 15-5-7

http://dx.doi.org/10.6113/JPE.2015.15.5.1207
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A New DPWM Method to Suppress the Low Frequency Oscillation of the Neutral-Point Voltage for NPC Three-Level Inverters

Jianguo Lyu[†], Wenbin Hu[*], Fuyun Wu[**], Kai Yao[*], and Junji Wu[***]

[†,***]School of Energy and Power Engineering, Nanjing University of Science and Technology, Nanjing, China
[*]School of Automation, Nanjing University of Science and Technology, Nanjing, China
[**]College of Electrical and Automatic Engineering, Sanjiang University, Nanjing, China

Abstract

In order to suppress the low frequency oscillation of the neutral-point voltage for three-level inverters, this paper proposes a new discontinuous pulse width modulation (DPWM) control method. The conventional sinusoidal pulse width modulation (SPWM) control has no effect on balancing the neutral-point voltage. Based on the basic control principle of DPWM, the relationship between the reference space voltage vector and the neutral-point current is analyzed. The proposed method suppresses the low frequency oscillation of the neutral-point voltage by keeping the switches of a certain phase no switching in one carrier cycle. So the operating time of the positive and negative small vectors is equal. Comparing with the conventional SPWM control method, the proposed DPWM control method suppresses the low frequency oscillation of the neutral-point voltage, decreases the output waveform harmonics, and increases both the output waveform quality and the system efficiency. An experiment has been realized by a neutral-point clamped (NPC) three-level inverter prototype based on STM32F407-CPLD. The experimental results verify the correctness of the theoretical analysis and the effectiveness of the proposed DPWM method.

Key words: Discontinuous pulse width modulation (DPWM), Low frequency oscillation, Neutral-point voltage balancing, Three-level inverter

I. INTRODUCTION

The conventional control method for two-level inverters is very simple and easily implemented. However, there are some drawbacks, such as high total harmonic distortion (THD) of the output waveforms, high voltage stress of the switching devices, low system efficiency and so on [1]-[3]. This is especially true in middle and high voltage, or high power conversions. Akira Nabae proposed a new neutral-point clamped (NPC) PWM inverter in 1980, which is the basic three-level inverter [1]. Comparing with the conventional two-level inverter, the three-level inverter has many advantages, such as low voltage stress on switching devices, high equivalent switching frequency, reduced output harmonics, etc. [4]-[6]. Therefore, it is widely used in middle and high voltage, or high power applications [1], [4].

In order to generate phase voltage with three-levels and line voltage with five-levels, the NPC three-level inverter circuit needs two DC bus capacitors connected in series between the positive and negative poles of the DC bus. Ideally, the voltage on each capacitor is half the DC bus voltage. However, due to capacitance errors of the capacitors, different parameters of the switching devices, unbalanced three-phase operation, and other factors[12], a DC bus neutral-point voltage unbalancing problem appears, which influences the output waveforms quality[2], [6]. In addition, this problem makes the output waveforms containing a lot of low frequency harmonics. When the neutral-point voltage unbalancing problem becomes serious, it damages the switching devices and affects the system operation [6]. To solve this problem, many methods have been proposed

Manuscript received Dec. 19, 2014; accepted May 2, 2015
Recommended for publication by Associate Editor Honnyong Cha.
[†]CorrespondingAuthor:lvgd2008@163.com
Tel: +86-025-84303113,Fax: +86-025-84303113, NUST
[*]School of Automation, Nanjing Univ. of Science and Tech., China
[**]College of Electrical and Automatic Eng., Sanjiang University, China
[***]School of Energy and Power Engineering, NUST, China

[2]-[13].

The neutral-point voltage unbalancing problem contains two parts: the dc deviation and the low frequency oscillation of the neutral-point voltage. The dc deviation of the neutral-point voltage can be controlled by many solutions proposed in the literature. For example, zero-sequence voltage injection methods have been proposed in [2], [7], Ref. [3], [5] propose improved space vector modulation (SVM) methods to reduce the neutral-point voltage unbalancing. In addition, they correctly select other vectors, which do not impact on the neutral-point voltage, to replace the small vectors.

The low frequency oscillation of the neutral-point voltage can lead to a lot of low frequency harmonics in the output waveforms, and the voltage stress of the switches is increased [4], [10]-[11]. When the dc deviation of the neutral-point voltage appears, the low frequency oscillation problem can also exacerbate the neutral-point voltage unbalancing, especially in middle or high power applications. However, the low-frequency oscillation problem of the neutral-point voltage is commonly ignored.

Ref. [9], [11] analyze the low frequency oscillation of the neutral-point voltage. However, a solution for this problem is not presented. In [10], a new modulation strategy using small vectors to compensate for the effects of all of the vectors in each carrier cycle is proposed to reduce the neutral-point voltage ripple. Ref. [4] proposes a double modulation waves strategy based on SPWM to enable the average neutral-point current to be zero. So the low frequency oscillation of the neutral-point voltage is eliminated. However, it has a much higher switching frequency when compared with the conventional SPWM control method.

Based on the basic principle of discontinuous pulse width modulation (DPWM), this paper proposes a new DPWM control method to suppress the low frequency oscillation of the neutral-point voltage. By distinguishing the odd and even carrier cycles, and the prior and latter half carrier cycles, the proposed method controls the switches of a certain phase so that there is no switching in each carrier cycle. In addition, in each carrier cycle, the operating time of the positive and negative small vectors in pairs is equal. Therefore, the average value of the neutral-point current is zero in a carrier cycle, and a neural-point voltage without low frequency oscillation can be achieved. When compared with the conventional SPWM control, without adding complex hardware circuits or increasing the switching frequency, the new DPWM control method proposed in this paper can suppress the low frequency oscillation of the neutral-point voltage effectively under different load conditions. This decreases the output waveforms harmonics and significantly increases the system efficiency. The proposed DPWM control method is easy to achieve with digital implementation. Experiments have been realized by a NPC three-level inverter prototype based on STM32F407-CPLD, and the experimental results verify the feasibility and effectiveness of the proposed method.

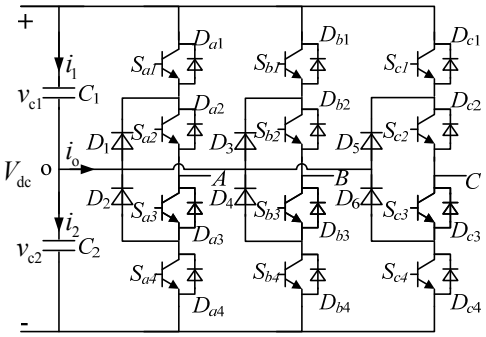


Fig. 1. Main circuit of NPC three-level inverter.

TABLE I
OUTPUT LEVEL OF THREE LEGS AND SWITCHING STATES

Working state	Switching state				Output leg level
	S_{X1}	S_{X2}	S_{X3}	S_{X4}	
P	√	√	×	×	$V_{dc}/2$
0	×	√	√	×	0
N	×	×	√	√	$-V_{dc}/2$

II. THE BASIC PRINCIPLE OF DPWM CONTROL

Fig. 1 shows the main circuit topology of a NPC three-level inverter. The nodal point connected to the DC bus capacitors C_1 and C_2 is neutral-point O for the NPC three-level inverter.

Take phase a as an example, its output leg consists of four switches (S_{a1}, S_{a2}, S_{a3}, S_{a4}), four anti-parallel free-wheeling diodes (D_{a1}, D_{a2}, D_{a3}, D_{a4}), and two clamping diodes (D_1, D_2).

"P", "0", and "N" represent three working states corresponding to the three output levels of the NPC three-level inverter. The neutral-point "O" is defined as the reference point, and the corresponding output levels and switching states are shown in Table I. Where S_{xn} (x=a, b, c, and n=1, 2, 3, 4) represents the four switches of each phase leg for the NPC three-level inverter in Fig. 1. V_{dc} is the input DC bus voltage. "√" and "×" represents the switching on and switching off states, respectively.

The DPWM control method can keep switches no switching at specific areas in a line cycle, and its most significant advantage is reducing switching losses. Thus, the DPWM control method can improve the conversion efficiency of the inverter.

Three conventional control methods based on DPWM are the 120°DPWM, 60°DPWM, and 30°DPWM [14][15]. The 60°DPWM control method is shown in Fig. 2, where v_a, v_b, v_c represents the three-phase modulation waves for a NPC three-level inverter with the conventional SPWM control. It can be seen that the line cycle has been divided into six equal regions.

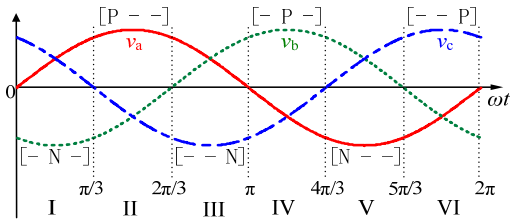


Fig. 2. The operating principle of 60° DPWM.

The regions are defined as follows: I(0–π/3), II(π/3–2π/3), III(2π/3–π), IV(π–4π/3), V(4π/3–5π/3), and VI(5π/3–2π).

In each region, the switches of one certain phase keep no switching. So the corresponding output level is in the "P" or "N" state, the details are as follows:

(1) In regions I(0–π/3), III(2π/3–π), and V(4π/3–5π/3), for the phase modulation wave with the lowest voltage value, the corresponding switches S_{x3}, S_{x4} of this phase are kept in the on-state, and the switches S_{x1}, S_{x2} of this phase are kept in the off-state. Therefore, the output phase leg is in the "N" state,

(2) In regions II(π/3–2π/3), IV(π–4π/3), and VI(5π/3–2π), for the phase modulation wave with the highest voltage value, the corresponding switches S_{x1}, S_{x2} of this phase are kept in the on-state, and the switches S_{x3}, S_{x4} of this phase are kept in the off-state. Therefore, the output phase leg is in the "P" state.

When compared with the conventional SPWM control method, the 60°DPWM control method reduces the equivalent switching frequency by about 33% under resistive load conditions. As a result, it can reduce the switching losses and improve the conversion efficiency of the inverter. However, reducing the equivalent switching frequency causes some problems, which cannot be ignored, such as increasing the output harmonics and decreasing the quality of the output waveforms.

The three conventional DPWM control methods reduce the switching losses by controlling the switches no switching in certain regions [15]. However, they are commonly ineffective for the neutral-point voltage unbalancing control, especially for the low-frequency oscillation problem.

III. The Influence of the Reference Space Voltage Vector on the Neutral-Point Current

As shown in Table I, each phase of a NPC three-level inverter has three working states (P, 0, N). Therefore, the NPC three-level inverter has a total of 27(3^3) kinds of working states. Each working state corresponds to one reference space voltage vector. Thus, there are 27 reference space voltage vectors including 6 big vectors, 6 medium vectors, 12 small vectors, and 3 zero vectors.

When the zero vectors operate, the neutral-point current is zero. As a result, the zero vector has no effect on the neutral-point current. When the big, medium and small vectors operate, the flowing direction of the neutral-point current can be obtained.

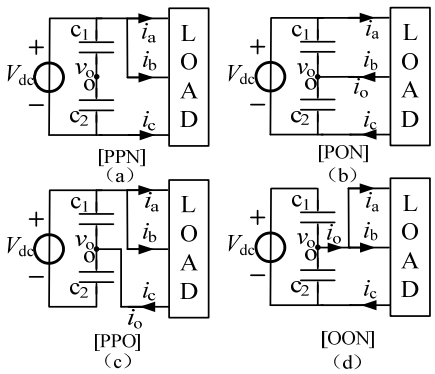


Fig. 3. The impact on the neutral-point voltage of load currents.

The impact on the neutral-point voltage of the load currents is shown in Fig. 3 when the big vector [PPN], medium vector [P0N], positive small vector [PP0], and negative small vector [00N] operates, respectively. Where i_a, i_b, i_c represents the three-phase load currents, v_o represents the neutral-point voltage, and i_o represents the neutral-point current.

Suppose the three-phase loads are symmetrical, as shown in Fig. 3(a). When the big vector [PPN] operates, the three-phase loads are not connected with the neutral-point O. Thus, i_o is zero in this state, and the load currents have no effect on the neutral-point current. From Fig. 3(b), it can be seen that the flowing direction of i_b cannot be determined when the medium vector [PON] operates. It can also be seen that the flowing direction of i_o is uncertain. Therefore, its influence on the neutral-point voltage cannot be determined. From Fig. 3(c), it can be seen that when the positive small vector [PP0] operates, i_o is equal to i_c, and i_o flows into the neutral-point O. As a result, v_o increases. When the negative small vectors operates in Fig. 3(d), it can be seen that i_o flows out of the neutral-point O. Therefore, v_o decreases.

Comparing Fig. 3(c) with Fig. 3(d), it can be seen that when the positive small vector [PP0] and the negative small vector [00N] operates respectively, the flowing directions of i_o are opposite. As a result, their impact on v_o is opposite. In addition, the neutral-point voltage unbalancing problem can be solved by properly selecting the operating time of the positive and negative small vectors.

IV. Methods for Suppressing the Low Frequency Oscillation of the Neutral-Point Voltage

A. Comparing the Conventional SPWM with the Proposed DPWM

The corresponding relationship between the three-phase modulation waves and the space vector distribution is shown in Fig. 4. When the modulation ratio is low, suppose that the

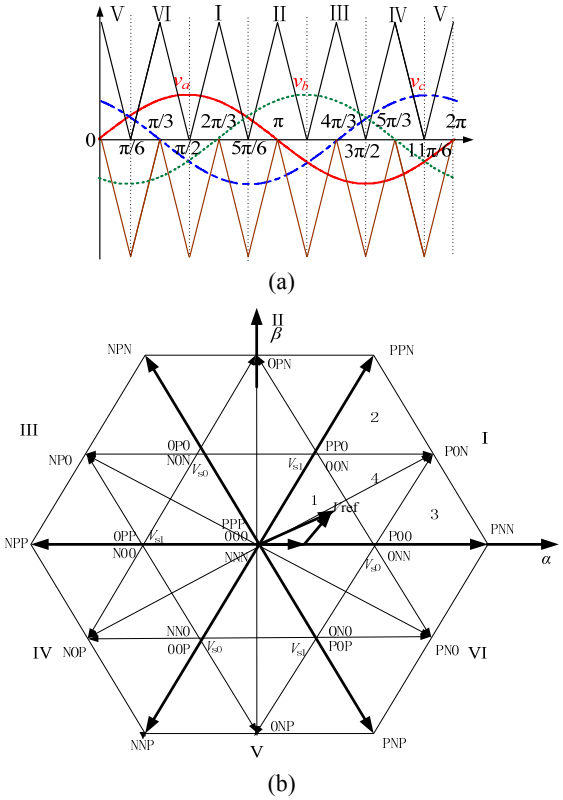


Fig. 4. The relationship between the space vector and the three-phase modulation waves distribution.

three-phase modulation waves are in region I in Fig. 4(a). Thus, the reference voltage vector V_{ref} falls in the small triangle area 1 of sector I as shown in Fig. 4(b).

Taking area 1 of sector I as an example, suppose the amplitude and period of the carrier wave are normalized using the conventional SPWM and the proposed DPWM controls. A detailed analysis is shown in Fig.5, which concerns the operating of the space vectors, and the corresponding neutral-point current.

From Fig. 5, it can be seen that the reference voltage vector is composed of three voltage vectors: V_1[P00, 0NN], V_2[PP0, 00N], and V_3[000]. The vectors [P00] and [0NN] are a pair of positive and negative small vectors, so are the vectors [PP0] and [00N].

When using the conventional SPWM control method, as shown in Fig. 5(a), in a carrier cycle, the three voltage vectors above meet:

$$d_{s1}^{+} + d_{s1}^{-} + d_{s2}^{-} + d_{s3} = 1 \quad (1)$$

Where d_{s1}^{+}, d_{s1}^{-}, d_{s2}^{-}, d_{s3} is the operating time of vectors [P00], [0NN], [00N], and [000], respectively.

The modulation process of the proposed DPWM control method is shown in Fig. 5(b). Define the prior carrier cycle as an odd carrier cycle, and the next adjacent carrier cycle becomes an even carrier cycle. The details of the proposed DPWM control method are as follows:

(1) In the odd carrier cycle, the carrier cycle is divided into two equal parts: the prior and the latter half cycle. In the prior half cycle, the three-phase modulation waves v_a, v_b, v_c are all superimposed by an offset value V_{offset}, where $V_{offset} = -V_{max}$, ($V_{max} > 0$), and V_{max}=max{ v_a, v_b, v_c }. As a result, v_a'= v_a+V_{offset}, v_b'= v_b+V_{offset}, and v_c'= v_c+V_{offset}, where v_a', v_b', v_c' represent the modulation waves with the proposed DPWM control. For the phase with the maximum instantaneous output voltage, its output leg voltage is clamped at the "0" level. In the latter half cycle, v_a, v_b, v_c are all superimposed by an offset value V_{offset}, where $V_{offset} = -V_{min}$, ($V_{min} < 0$), and V_{min}=min{ v_a, v_b, v_c }. Thus, for the phase with the minimum instantaneous output voltage, its output leg voltage is clamped at "0" level.

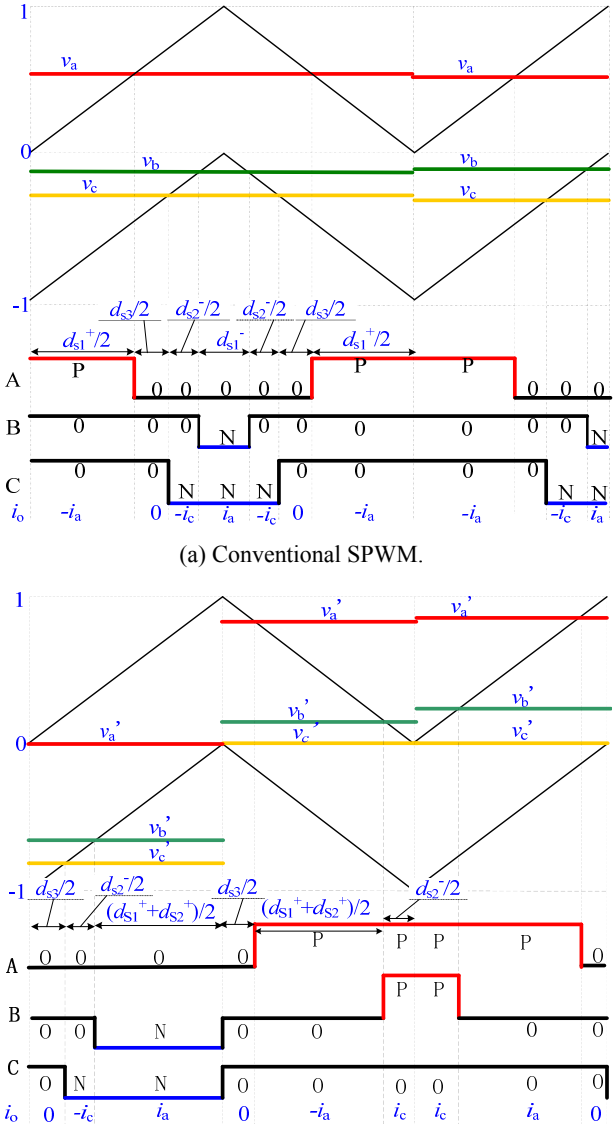
(2) In the even carrier cycle, the carrier cycle is also divided into two equal parts: the prior and the latter half cycle. In the prior half cycle, v_a, v_b, v_c are all superimposed by an offset value V_{offset}, where $V_{offset} = -V_{min}$. Therefore, for the phase with the minimum instantaneous output voltage, its output leg voltage is clamped at the "0" level. In the latter half cycle, v_a, v_b, v_c are all superimposed by an offset value V_{offset}, where $V_{offset} = -V_{max}$. Thus, for the phase with the maximum instantaneous output voltage, its output leg voltage is clamped at the "0" level.

Where v_a, v_b, v_c represent the modulation waves with the conventional SPWM control, and v_a', v_b', v_c' represent the modulation waves with the proposed DPWM control. In addition, d_{s1}^{+}, d_{s1}^{-}, d_{s2}^{-}, d_{s3} is the operating time of vectors [P00], [0NN], [00N], [000], respectively, when using the conventional SPWM control.

From Fig. 5(a) and 5(b), the operating time of the positive and negative small vectors in the proposed DPWM and conventional SPWM control methods can be seen clearly. A performance comparison of the two methods is shown in Table II.

From Table II, it can be seen that when using the conventional SPWM control method, the operating time of the vectors [PP0] and [00N] is 0 and d_{s2}^{-}, respectively, and that the operating time of vectors [P00] and [0NN] is d_{s1}^{+} and d_{s1}^{-} respectively. The operating time of the positive and negative small vectors in pairs is not equal in a carrier cycle, and the neutral-point voltage unbalancing problem exists. When using the proposed DPWM control method proposed in this paper, it can be seen that the operating time of the vectors [PP0] and [00N] are both $d_{s2}^{-}/2$, and that the operating time of the vectors [P00] and [0NN] are both $(d_{s1}^{+}+d_{s1}^{-})/2$. Therefore, the operating time of the positive small vectors is equal to that of the negative small vectors in a carrier cycle.

According to the analysis above, the proposed DPWM control method distinguishes the odd and even carrier cycles. In addition, one carrier cycle is divided into two parts, which are controlled respectively. The operating time of the positive (or negative) small vector in the prior half cycle is equal to that of the negative (or positive) small vector in the latter half



(a) Conventional SPWM.

(b) Proposed DPWM.

Fig. 5. Space vector and neutral-point current.

cycle. The average value of the neutral-point current is zero in a carrier cycle, and the neural-point voltage balance without a low frequency oscillation can be achieved.

B. Suppressing the Low Frequency Oscillation of the Neutral-Point Voltage

As shown in Fig. 1, when the neutral-point voltage is balancing, the voltages of C_1 and C_2 are both half the DC bus voltage. Under this condition, the neutral-point O is defined as the reference zero potential. ΔV_{NP} is the voltage variation of the neutral-point O, which is relative to the reference zero potential, which is simply the neutral-point voltage variation. Thererore, the neutral-point voltage variation ΔV_{NP} can be expressed as:

$$\Delta V_{NP} = -\frac{(v_{c1} - v_{c2})}{2} = -\frac{1}{2C}\int (i_1 - i_2)dt \tag{2}$$

TABLE II

PERFORMANCE COMPARISON BETWEEN THE PROPOSED DPWM AND THE SPWM METHOD

Control method	Positive small vectors		Negative small vectors	
	PP0	P00	00N	0NN
SPWM	0	d_{s1}^+	d_{s2}^-	d_{s1}^-
New DPWM	$d_{s2}^-/2$	$(d_{s1}^+ + d_{s1}^-)/2$	$d_{s2}^-/2$	$(d_{s1}^+ + d_{s1}^-)/2$

Where v_{c1} and v_{c2} represent the voltage of the capacitors C_1 and C_2, C is the capacitance of C_1 and C_2, and i_1 and i_2 represents the currents flowing through C_1 and C_2, respectively.

As a result, when the neutral-point voltage is balancing, ΔV_{NP} is zero. Conversely, the voltages of C_1 and C_2 are not equal, and ΔV_{NP} cannot be zero.

Suppose that the average value of the neutral-point current is equal to its instantaneous value in a carrier cycle. Then, the instantaneous value of the neutral-point current $i_o(t)$ can be approximately expressed as:

$$i_o(t) = i_1 - i_2 = i_o \tag{3}$$

Where i_o is the average value of the neutral-point current in a carrier cycle.

According to (2) and (3), in a carrier cycle, the relationship between ΔV_{NP} and i_o can be derived as:

$$\Delta V_{NP} = \int_0^{T_s} -\frac{1}{2C} i_o(t)dt = -\frac{1}{2C} i_o T_s \tag{4}$$

Where T_s is the period of a carrier cycle.

Using the conventional SPWM control, the neutral-point voltage fluctuates in a low frequency, which is mainly three times the line frequency. This has been analyzed in many literatures [9], [10].

In order to analyze the detailed realization of the proposed DPWM control method in this paper, which can suppress the low frequency oscillation of the neutral-point voltage, a line cycle is discretized to 400 carrier cycles, and the carrier frequency f_s is 20kHZ. Since the proposed DPWM control method distinguishes the odd and even carrier cycles, and the prior and the latter half cycle in one carrier cycle, define half a carrier cycle as a unit, and k as an integer variable, k=0,1…799, so that the number of units in a line cycle is 800.

In a line cycle, the range is [0, 2π], and max(ωt) and min(ωt) and are defined as maximum and minimum instantaneous value of the three-phase sinusoidal waves, which are normalized. The envelop curve can be expressed as:

$$\max(\omega t) = \begin{cases} \sin(\omega t), & \pi/6 < \omega t \le 5\pi/6 \\ \sin(\omega t - 2\pi/3), & 5\pi/6 < \omega t \le 3\pi/2 \\ \sin(\omega t + 2\pi/3), & 0 \le \omega t \le \pi/6 \ or \\ & 3\pi/2 < \omega t \le 2\pi \end{cases} \tag{5}$$

$$\min(\omega t)=\begin{cases}\sin(\omega t), & 7\pi/6<\omega t\le 11\pi/6\\ \sin(\omega t-2\pi/3), & 0\le\omega t\le\pi/2 \ or\\ & 11\pi/6<\omega t\le 2\pi\\ \sin(\omega t+2\pi/3), & \pi/2<\omega t\le 7\pi/6\end{cases} \quad (6)$$

In order to ensure that the amplitude of the three-phase modulation waves with the proposed DPWM control method cannot exceed the amplitude of the triangular carrier wave, the following equation must be satisfied:

$$m\,|\max(\omega t)-\min(\omega t)|\le 1 \quad (7)$$

Derived from the above equation, m is expressed as:

$$0<m\le\sqrt{3}/3 \quad (8)$$

Where m is the modulation ratio.

Thus, the proposed DPWM control method is applied to the three-level inverter at a low modulation ratio. In addition, its reference space voltage vector is only composed of positive small vectors, negative small vectors and the zero vector. Therefore, it is more effective to control the operating time of the positive and negative small vectors to be equal in a carrier cycle to suppress the low frequency oscillation and control the neutral-point voltage balancing.

When ωt is discretized, ωt_k is used instead of ωt. Therefore, ωt_k is defined as:

$$\omega t_k=k\,2\pi/799,\quad k=0,1\ldots799 \quad (9)$$

$$\omega t=\omega t_k \quad (10)$$

According to Fig. 5(b), the three-phase duty cycles are:

$$d_a(\omega t_k)=\begin{cases}m\left(\left|\sin(\omega t_k)-\max(\omega t_k)\right|\right), & k=0,4,8\ldots796 \text{ or } k=3,7,11\ldots799\\ m\left(\left|\sin(\omega t_k)-\min(\omega t_k)\right|\right), & k=1,2,5,6\ldots797,798\end{cases} \quad (11)$$

$$d_b(\omega t_k)=\begin{cases}m\left(\left|\sin(\omega t_k-2\pi/3)-\max(\omega t_k)\right|\right), & k=0,4,8\ldots796 \text{ or } k=3,7,11\ldots799\\ m\left(\left|\sin(\omega t_k-2\pi/3)-\min(\omega t_k)\right|\right), & k=1,2,5,6\ldots797,798\end{cases} \quad (12)$$

$$d_c(\omega t_k)=\begin{cases}m\left(\left|\sin(\omega t_k+2\pi/3)-\max(\omega t_k)\right|\right), & k=0,4,8\ldots796 \text{ or } k=3,7,11\ldots799\\ m\left(\left|\sin(\omega t_k+2\pi/3)-\min(\omega t_k)\right|\right), & k=1,2,5,6\ldots797,798\end{cases} \quad (13)$$

Supposing that m=0.3, the angular frequency ω=100π, and the load are purely resistive loads (cos(φ)=1). Therefore, the three-phase ideal duty cycles are shown in Fig. 6.

The output currents of the NPC three-level inverter are:

$$i_a(\omega t_k)=I_m\sin(\omega t_k-\varphi) \quad (14)$$

$$i_b(\omega t_k)=I_m\sin(\omega t_k-2\pi/3-\varphi) \quad (15)$$

$$i_c(\omega t_k)=I_m\sin(\omega t_k+2\pi/3-\varphi) \quad (16)$$

Where φ is the load power factor angle, and I_m is the amplitude of the three-phase output current.

From the analysis in section III, it can be seen that in a carrier cycle, the average value of the neutral-point current i_o can be expressed as:

$$i_o=-\left(d_a(\omega t_k)i_a(\omega t_k)+d_b(\omega t_k)i_b(\omega t_k)+d_c(\omega t_k)i_c(\omega t_k)\right) \quad (17)$$

Where $i_a(\omega t_k)$, $i_b(\omega t_k)$, and $i_c(\omega t_k)$ are the output currents of the NPC three-phase inverter, and $d_a(\omega t_k)$, $d_b(\omega t_k)$, and $d_c(\omega t_k)$ are the control duty cycles of the inverter.

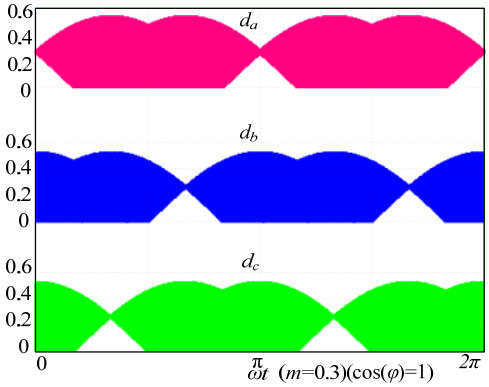


Fig. 6. Ideal duty cycles of proposed DPWM control.

Define the variable so that n= 0, 1 ... 399, and n is an integer, and the number of carrier cycles in a line cycle is 400. Therefore, supposing k= 2n, from (17), the neutral-point current of the prior and latter half cycles in a carrier cycle can be derived. Thus, the average value of the neutral-point current in a carrier cycle is as follows:

$$i_o=\frac{1}{2}(i_{o(2n)}+i_{o(2n+1)}),(n=0,1\ldots399) \quad (18)$$

Where $i_{o(2n)}$ and $i_{o(2n+1)}$ are expressed as:

$$i_{o(2n)}=\begin{bmatrix}1-d_a(\omega t_{2n}) & 1-d_b(\omega t_{2n}) & 1-d_c(\omega t_{2n})\end{bmatrix}\begin{bmatrix}i_a(\omega t_{2n})\\ i_b(\omega t_{2n})\\ i_c(\omega t_{2n})\end{bmatrix},(n=0,1\ldots399) \quad (19)$$

$$i_{o(2n+1)}=\begin{bmatrix}1-d_a(\omega t_{2n+1}) & 1-d_b(\omega t_{2n+1}) & 1-d_c(\omega t_{2n+1})\end{bmatrix}\begin{bmatrix}i_a(\omega t_{2n+1})\\ i_b(\omega t_{2n+1})\\ i_c(\omega t_{2n+1})\end{bmatrix},(n=0,1\ldots399) \quad (20)$$

By substituting (18) into (4), the expression of ΔV_{NP} can be obtained as:

$$\Delta V_{NP}=-\frac{1}{4C}T_s(i_{o(2n)}+i_{o(2n+1)}),(n=0,1\ldots399) \quad (21)$$

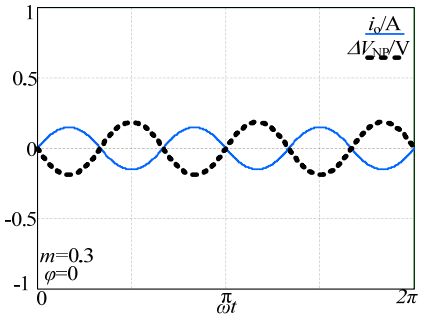
To compare with the conventional SPWM control, supposing m=0.3, φ=0 (under resistive load conditions), and when I_m, C and T_s are normalized, the variation trend of i_o and ΔV_{NP} with the conventional SPWM and proposed DPWM control methods are shown in Fig. 7.

From Fig. 7(a), it can be seen that when using the conventional SPWM control method, i_o and ΔV_{NP} both fluctuate at three times the line frequency.

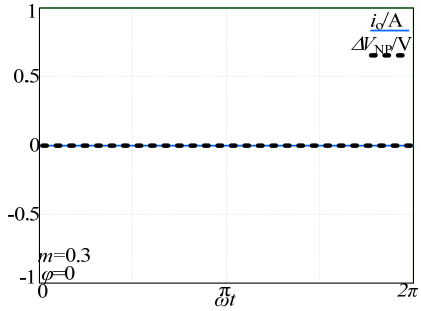
In Fig. 7(b), i_o and ΔV_{NP} are both zero in any carrier cycle with the proposed DPWM control method.

According to (4), (21) and m= 0.3, with the conventional SPWM and proposed DPWM control methods, the surface of ΔV_{NP} as the function of φ and ωt is plotted as shown in Fig. 8. It can be seen that when φ varies from –π to π, or when ωt varies from 0 to 2π, using the conventional SPWM control method in Fig. 8(a), ΔV_{NP} fluctuates, so that the neutral-point voltage has a low frequency oscillation.

From Fig. 8(b), it can be seen that when using the proposed

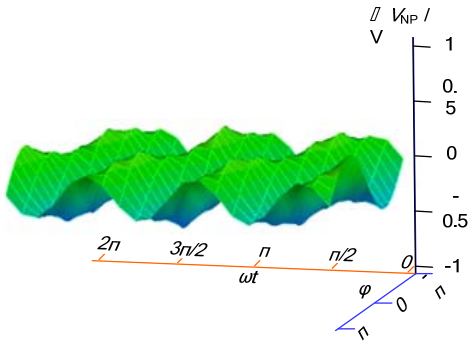


(a) Conventional SPWM control.

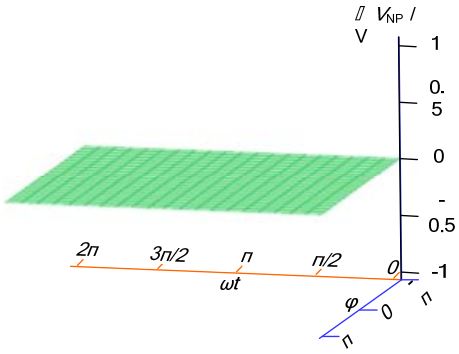


(b) Proposed new DPWM control.

Fig. 7. Curves of i_o and ΔV_{NP}.



(a) Conventional SPWM control.

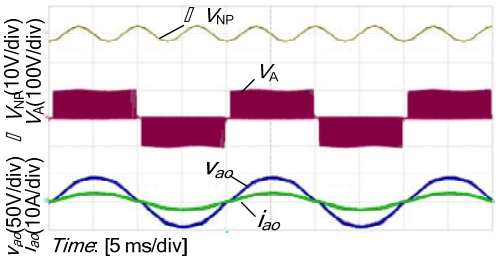


(b) Proposed DPWM control.

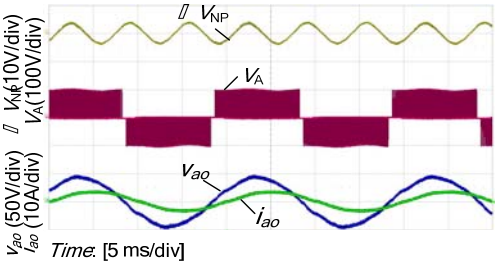
Fig. 8. Surface of ΔV_{NP} as the function with φ and ωt.

DPWM control method, ΔV_{NP} is not varied respect to φ and ωt. It can also be seen that ΔV_{NP}=0 in a line cycle.

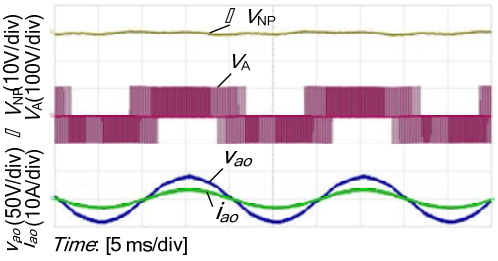
From the above comparison, it can be seen that at different load power factor conditions, the proposed DPWM control method achieves the neutral-point voltage balancing without a low frequency oscillation.



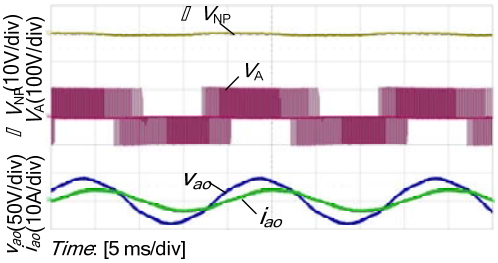
(a) Conventional SPWM control at cos(φ)=1.



(b) Conventional SPWM control at cos(φ)=0.866.



(c) Proposed DPWM control at cos(φ)=1.



(d) Proposed DPWM control at cos(φ)=0.866.

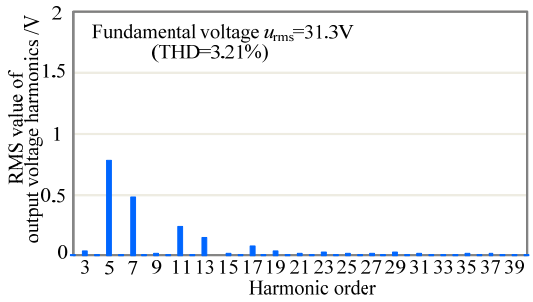
Fig. 9. Experimental waveforms.

V. Experimental Verification

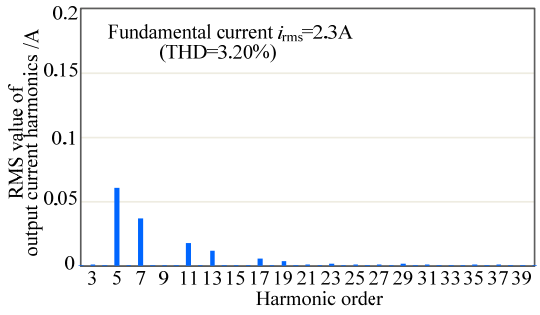
In order to verify the validity of the proposed DPWM control method, which suppresses the low frequency oscillation of the neutral-point voltage, a NPC three-level inverter prototype has been built and tested in the lab.

The specification of the prototype are as follows:

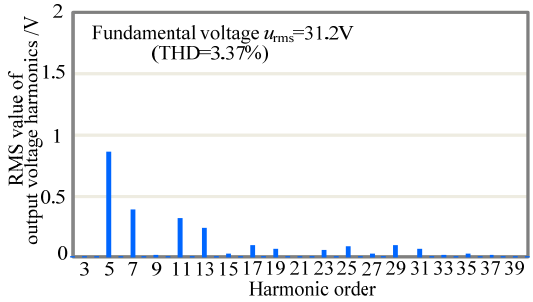
- Input DC bus voltage: V_{dc}=200V
- Input power: P_{in}=50-230W
- DC bus capacitors: C_1=C_2=150uF
- Switching frequency: f_s=20kHZ
- Control processor: STM32F407
- Logical drive processing unit: EPM1270T (CPLD)
- Power switches module: IGBT FZ06NPA070FP
- Output phase filter: L=1.5mH, C=10uF



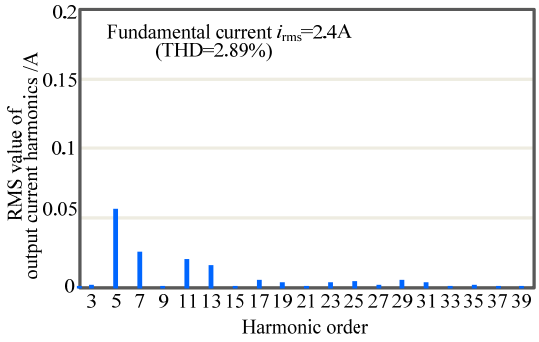
(a) THD analysis of v_{ao} at cos(φ)=1.



(b) THD analysis of i_{ao} at cos(φ)=1.

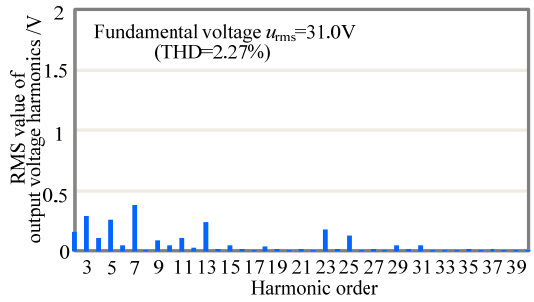


(c) THD analysis of v_{ao} at cos(φ)=0.866.

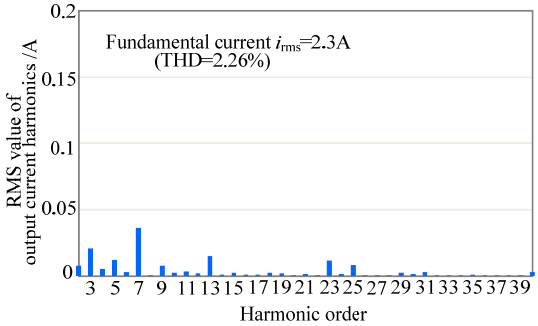


(d) THD analysis of i_{ao} at cos(φ)=0.866.

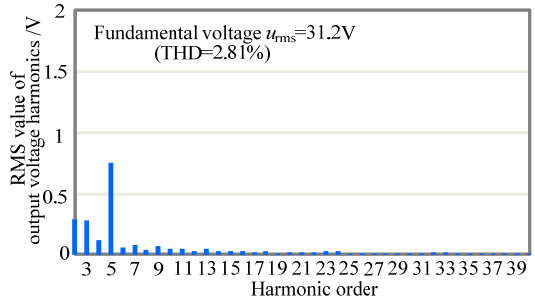
Fig. 10. THD analysis with conventional SPWM control.



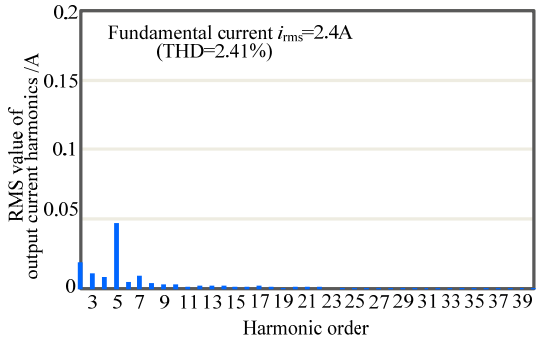
(a) THD analysis of v_{ao} at cos(φ)=1.



(b) THD analysis of i_{ao} at cos(φ)=1.



(c) THD at analysis of v_{ao} cos(φ)=0.866.



(d) THD analysis of i_{ao} at cos(φ)=0.866.

Fig. 11. THD analysis with proposed DPWM control.

When V_{dc}=200V, and P_{in}=200W, the experimental waveforms of ΔV_{NP}, V_A, v_{ao}, and i_{ao} with the conventional SPWM control and proposed DPWM control methods are shown in Fig. 9, where ΔV_{NP} represents the input DC bus neutral-point voltage variation, V_A represents the leg voltage of phase a, v_{ao} represents the output phase voltage of phase a, and i_{ao} represents the output current of phase a.

From Fig. 9, it can be seen that when compared with the conventional SPWM control method under different load power factor conditions, the ripple value of ΔV_{NP} is obviously decreased with the proposed DPWM control method.

Fig. 10-11 show the THD analysis results of v_{ao} and i_{ao} with the conventional SPWM control and the proposed DPWM method in this paper, respectively. Where u_{rms} and i_{rms} represents the Root-Mean-Square(RMS) value of the

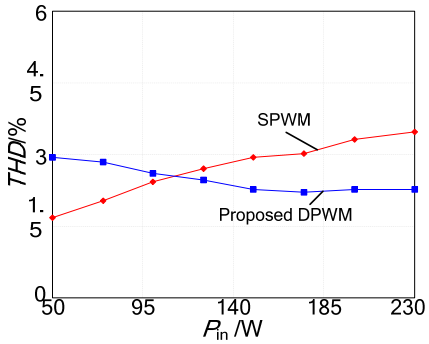


Fig. 12. Measured THD.

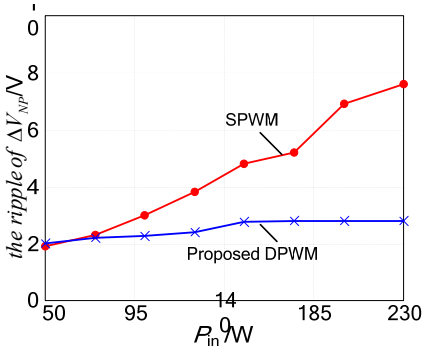


Fig. 13. Measured neutral-point voltage ripple.

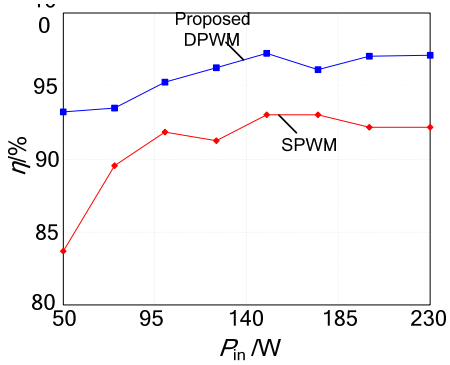


Fig. 14. Measured efficiency.

output voltage and current respectively. By using the proposed DPWM method in this paper, the THD value of i_{ao} decreases from 3.20% to 2.26% at cos(φ)=1, as shown in Fig 10(b) and Fig 11(b). At cos(φ)=0.866, as shown in Fig 10(d) and Fig 11(d), the THD value of i_{ao} decreases from 2.89% to 2.41%. In addition, the THD value of v_{ao} is decreased at different load power factor conditions. Therefore, using the proposed DPWM control method in this paper, the output waveforms show obvious advantages in terms of the THD at different load power factor conditions when compared with the conventional SPWM methods.

At different resistive load conditions, when the input power varies, the ripple value of ΔV_{NP}, the THD value of the output current and the efficiency curves are shown in Fig. 12-14. It can be seen that at various input powers, the proposed DPWM control method proposed in this paper achieves the low frequency oscillation suppression for the neutral-point voltage. When compared with the conventional SPWM, the quality of the output waveforms and the system efficiency are improved with the proposed DPWM control method.

VI. Conclusion

Three-level inverters have many advantages, such as low voltage stress on the switching devices and low output harmonics. As a result, they are suitable for high voltage, and medium or high power applications. When using the conventional SPWM control method, the DC bus neutral-point voltage has a low frequency oscillation, the output current contains a lot of harmonics, and the efficiency of the inverter is relatively low, especially when the input voltage or the input power is higher. To solve this problem, a new DPWM control method is proposed in this paper, which suppresses the low frequency oscillation of the neutral-point voltage, reduces the output current harmonics, improves the quality of the output waveforms, and increases the system efficiency. In order to verify the validity of the proposed DPWM control method, experimental results are obtained based on a NPC three-level inverter prototype. The experimental results verify the correctness of the theoretical analysis and the effectiveness of the proposed method.

Acknowledgment

This work was supported by Science and Technology Support Program of Jiangsu Province (BE2013125), Innovation Foundation of Science and Technology Department of Jiangsu Province(BY2013004-01).

References

[1] A. Nabae, I. Takahashi, and H. Akagi. “A new neutral-point-clamped PWM Inverter,” *IEEE Trans. Ind. Appl.*, Vol. 1A-17, No. 5, pp. 518-522. Sep./Oct. 1981.

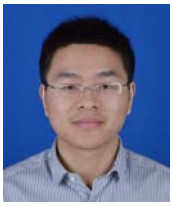
[2] C. C. Wang, Y. D. Li, “Analysis and calculation of Zero-Sequence Voltage Considering Neutral-Point Potential Balancing in Three-Level NPC converters,” *IEEE Trans. Ind. Electron*., Vol. 57, No.7, pp. 2262-2271, Jul. 2010.

[3] J. S. Lee and K. B. Lee, “New Modulation Techniques for a Leakage Current Reduction and a Neutral-Point Voltage Balance in Transformerless Photovoltaic Systems Using a Three-Level Inverter,” *IEEE Trans. Power Electron*., Vol. 29, No. 4, pp. 1720-1732, Apr. 2014.

[4] J. Pou, J. Zaragoza, S. Ceballos, V. M. Sala, R. P. Burgos, D. Boroyevich, “Fast-Processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point,” *IEEE Trans. Ind. Electron*., Vol. 54, No.4, pp. 2288-2294, Aug. 2007.

[5] U. M. Choi, J. S. Lee, and K. B. Lee, “New modulation strategy to balance the neutral-point voltage for three-level

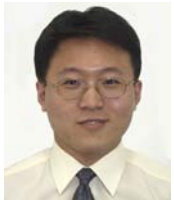
neutral-clamped inverter systems," *IEEE Trans. Energy Convers*., Vol. 29, No. 1, pp. 91-100, Mar. 2014.
[6] U. M. Choi and K. B. Lee, "Space vector modulation strategy for neutral-point voltage balancing in three-level inverter systems," *IET Power Electron.*, Vol. 6, No. 7, pp. 1390-1398, Apr.2013.
[7] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, Vol. 27, No. 2, pp. 642-651, Feb. 2012.
[8] Y. Jiao, F. C. Lee, and S. Z Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, Vol. 29, No. 10, pp. 5579-5591, Oct. 2014.
[9] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron*., Vol. 15, No. 2, pp. 242-249, Mar. 2000.
[10] H. B. Zhang, S. J. Finney, A. Massoud, and B. W. Williams, "An SVM algorithm to balance the capacitor voltages of the three-level NPC active power filter," *IEEE Trans. Power Electron.*, Vol.23, No. 6, pp. 2694-2702, Nov. 2008.
[11] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 6, pp. 1582-1588. Dec. 2005.
[12] U. M. Choi, H. H. Lee, and K. B. Lee, "Simple neutral point voltage control for three-level inverters using a discontinuous pulse width modulation," *IEEE Trans. Energy Convers.*, Vol. 28, No. 2, pp. 434-443, May 2013.
[13] J. Shen, S. Schroder, B. Duro, and R. Roesner, "A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion," *IEEE Trans. Ind. Electron*., Vol. 49, No.1, pp. 138-148, Jan./Feb. 2013.
[14] N. V. Nguyen, B. X. Nguyen, and H. H. Lee, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 9, pp. 3958-3966, Sep. 2011.
[15] Z. Zhang, O. C. Thomsen, and M. A. Andersen, "Discontinuous PWM modulation strategy with circuit-level decoupling concept of three level neutral-point clamped (NPC) inverter," *IEEE Trans. Ind. Electron*., Vol. 60, No. 5, pp. 1897-1906, May 2013.
[16] Y. Cho, T. LaBella, J. S. Lai, and M. K. Senesky, "A carrier-based neutral voltage modulation strategy for multilevel cascaded inverters under unbalanced DC sources," *IEEE Trans. Ind. Electron*., Vol. 61, No. 2, pp. 625-636, Feb. 2014.



Jianguo Lyu was born in Jiangsu province, China, in 1987. He is presently pursuing his Ph.D. degree in Control Science and Engineering at the Nanjing University of Science and Technology (NUST), Nanjing, China. His current research interests include the modeling and control of power converters, power factor correction converters, renewable energy generation systems and motor driving control.

Wenbin Hu was born in Jiangsu province, China, in 1970. He received his B.S. degree in Electrical Engineering and Automation from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1992; his M.S. degree in Control Theory and Control Engineering from the Nanjing University of Science and Technology (NUST), Nanjing, China, in 1999; and his Ph.D. degree in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics, in 2003. In 2004, he joined the Faculty of Electrical Engineering, School of Automation, Nanjing University of Science and Technology. In 2010, he became an Associate Professor at NUST, where he has been engaged in teaching and research in the field of power electronics. His current research interests include power factor correction converters, renewable energy generation systems and electric traction systems for rail vehicles.

Fuyun Wu was born in Jiangsu province, China, in 1988. She received her B.S. and M.S. degrees in Electrical Engineering and Automation from the Nanjing University of Science and Technology (NUST), Nanjing, China, in 2012 and 2015 respectively. In 2015, she joined the College of Electrical and Automatic Engineering, Sanjiang University, Nanjing, China, where she has been engaged in teaching and research in the field of power electronics. Her current research interests include the modeling and control of power converters, and renewable energy generation systems.



Kai Yao was born in Jiangsu province, China, in 1980. He received his B.S. degree in Industrial Automation from Nantong University, Nantong, China, in 2002; his M.S. degree in Mechanical Design and Theory, and his Ph.D. degree in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2005 and 2010, respectively. In 2011, he joined the Faculty of Electrical Engineering, School of Automation, Nanjing University of Science and Technology (NJUST), Nanjing, China, where he has been engaged in teaching and research in the field of power electronics. His current research interests include power factor correction converters, renewable energy generation systems and power supplies for LEDs.

Junji Wu was born in Henan Province, China, in 1955. He received his M.S. degree from the Nanjing University of Science and Technology (NUST), Nanjing, China, in 1990. In 1970, he joined in Nanjing University of Science and Technology. He became a professor at NUST, in 2000, where he has been engaged in teaching and research in the field of control science and engineering. His current research interests include the modeling and control of electrical systems, modern data acquisition technology, renewable energy generation systems and electric traction systems for rail vehicles.