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A Modified Single-Phase Transformerless Z-Source Photovoltaic Grid-Connected Inverter

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Abstract

In a grid-connected photovoltaic (PV) system, the traditional Z-source inverter uses a low frequency transformer to ensure galvanic isolation between the grid and the PV system. In order to combine the advantages of both Z-source inverters and transformerless PV inverters, this paper presents a modified single-phase transformerless Z-source PV grid-connected inverter and a corresponding PWM strategy to eliminate the ground leakage current. By utilizing two reversed-biased diodes, the path for the leakage current is blocked during the shoot-through state. Meanwhile, by turning off an additional switch, the PV array is decoupled from the grid during the freewheeling state. In this paper, the operation principle, PWM strategy and common-mode (CM) characteristic of the modified transformerless Z-source inverter are illustrated. Furthermore, the influence of the junction capacitances of the power switches is analyzed in detail. The total losses of the main electrical components are evaluated and compared. Finally, a theoretical analysis is presented and corroborated by experimental results from a 1-kW laboratory prototype.

Key words: Common-mode voltage, Leakage current, Photovoltaic power system, Power loss, Pulse width modulation, Z-source inverter

I. INTRODUCTION

For PV grid-connected systems, two types of inverters are usually used. One is a dc/ac inverter with a line-frequency transformer and the other is a dc/ac inverter with a dc/dc converter. This line-frequency transformer can boost the voltage after the dc/ac inverter and guarantee galvanic isolation between the grid and the PV system [1]. However, because of its low frequency (50–60Hz), this transformer is big, heavy and expensive [2]. Therefore, a high frequency dc-dc converter with a high-frequency transformer is used to boost the voltage to reach a constant value [3], [4]. Unfortunately, the high-frequency transformer and switches in the dc/dc converter will cause additional power loss. As a result, the interest in single-stage transformerless conversion topologies has grown.

In single-stage topologies, the Z-source inverter is one of the best choices to realize inversion and boost functions in a single stage [5]-[7]. It has some advantages such as a simple structure, high reliability of the inverter to avoid the influence of shoot-through due to EMI, and little output waveform distortion. However, the isolation capability has to be considered carefully because of the removal of the transformer. The traditional Z-source inverter topology with its PWM techniques can generate a high-frequency three-level CM voltage, whose peak value is equal to the Z-source capacitor voltage stress. Because of the capacitance between the PV panel and the ground, the high-frequency potential difference can cause undesirable leakage currents in transformerless PV systems [8]. The additional leakage currents can increase the grid current ripples, system losses, and (conducted and radiated) electromagnetic interferences [9]-[11]. Thus, a novel transformerless Z-source inverter topology and a particular PWM strategy should be researched to reduce leakage current in order to meet the strict grid codes established by authorities. For example, a 300mA threshold level is stated in the DIN VDE 0216 standard [12].

Recently many research works have been proposed to eliminate the leakage current to meet this standard. These leakage current reduction techniques can be mainly divided into two groups. One is a group of galvanic isolation techniques, and the other is a group of CM voltage clamping techniques.

The galvanic isolation topologies introduce dc-decoupling and ac-decoupling methods to disconnect PV systems and the

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grid during zero states [13]. H5 and H6 belong to the dc-decoupling topology family. The H5 topology, which is used in SMA (SMA Solar Technology AG) commercial converters, adds only one switch when compared to full-bridge (FB) inverters [14]. The H6 topology, which is proposed in [15], symmetrically adds two additional switches to the FB inverter. The H6 topology equally distributes the device's efforts and balances the thermal distribution. In [16], a novel H6 topology is proposed, which constructs a new direct power passing path in a half cycle to reduce the conduction loss. The highly efficient reliable inverter concept (HERIC) topology applies a bidirectional switch to realize the disconnection of the converter and the grid during zero-voltage vectors [17]. Due to the reduction of switches, the ac-decoupling method can provide lower power losses in the conduction path. Although the topologies mentioned above have a simple circuit structure, the galvanic isolation cannot completely eliminate the leakage current due to the influence of switches' junction capacitances and the parasitic parameters of the leakage current loop [15].

To completely eliminate the leakage current, the CM voltage should be clamped to half of the input voltage during the zero state, which can keep the CM voltage constant for all of the switching modes. This clamping technique has been used in the oH5 [18], modified H6 topologies [19], HB-ZVR [20] and HBZVR-D [21]. By connecting one pole of a PV cell directly to the neutral line of the grid, the leakage current can be eliminated. In [22], the negative pole of a PV array is directly connected to the neutral line of grid. In [23], the positive terminal of a PV array is connected to the phase output during the positive half-wave and to the neutral terminal during the negative half-wave. In addition, the neutral point clamp (NPC) inverter [24] connects the midpoint of a PV array to the neutral of a grid, which achieves three or more output levels. However, the NPC inverter, like the half-bridge inverter, demands a higher input voltage.

In this paper, a modified single-phase transformerless Z-source inverter (ZSI-TL) with one decoupling switch and two fast-recovery diodes is presented to eliminate the ground leakage current. In addition, a special PWM strategy is proposed to avoid zero states with the two lower switches conduction. Furthermore, it can ensure that each phase leg switches on and off once per switching cycle, and it can make the shoot-through zero states evenly allocated into each phase. Moreover, it is analyzed that the junction capacitances of the switches can influence the CV voltage, and a corresponding paralleled capacitor of the switch is designed. Hence, the path for the leakage current can be blocked by two reverse-biased diodes during the shoot-through state, while the CM voltage remains constant during the non-shoot-through state. Therefore, the leakage current is eliminated.

The paper is organized as follows. Section II introduces the ZSI-TL, its PWM strategy and the corresponding operation mode. Section III illustrates the leakage current reduction principle, while Section IV analyzes the system losses. Section V shows some experimental results, and Section VI draws some conclusions.

II. Operation Principles of the Modified Topology

A. Structure of the Modified ZSI-TL

Fig. 1 shows the ZSI-TL by using the dc-decoupling method. When compared with the traditional single-phase Z-source grid-connected inverter, the ZSI-TL adds one additional switch (S_5) and one fast-recovery diode (D_2). S_5 is used to electrically decouple the PV array from the grid during the zero state, while D_1 and D_2 are used to block the path of the leakage current during the shoot-through state.

B. Modified PWM Strategy

The PWM strategy is one of the key factors that affects the leakage current. To achieve the aim of eliminating the leakage current of the ZSI-TL, the modulation strategy of the traditional single-phase Z-source inverter needs to be modified. For Z-source inverter modulation, the shoot-through states are added to the null intervals to keep the active interval constant. In order to ensure that only one single device is switched during every state transition, the shoot-through states are added adjacent to the instants of the state transitions of a conventional voltage-source inverter. According to the ZSI-TL topology structure, the zero states where S_2 or S_4 conducts must be forbidden to eliminate the leakage current in the modified PWM strategy. Therefore, to achieve the aim of boosting the dc-link voltage, the shoot-through states should be added between the active sates and the zero states where S_1 or S_3 conducts.

As an illustration, Fig. 2 shows the switching patterns of the ZSI-TL. Here, S_1 is ON and S_2 is OFF during the positive half cycle. Sinusoidal reference signals are used to modulate S_3. S_4 and S_5, with additional shoot-through time intervals added, commutate complementarily to S_3. Similarly, during the negative half cycle, S_3 is ON and S_4 is OFF. S_1 commutates at the switching frequency. S_2 and S_5, with additional shoot-through time intervals added, commutate complementarily to S_1. It should be noted that each phase leg continues to switch on and off once per switching cycle. Without changing the total zero-state time interval, the shoot-through zero states are evenly allocated into each phase.

Assuming that the inductors L_{Z1} and L_{Z2} have the same inductance (L) and that the capacitors C_{Z1} and C_{Z2} have the same capacitance (C), the Z-source network becomes symmetrical. As a result, the following formula can be obtained as:

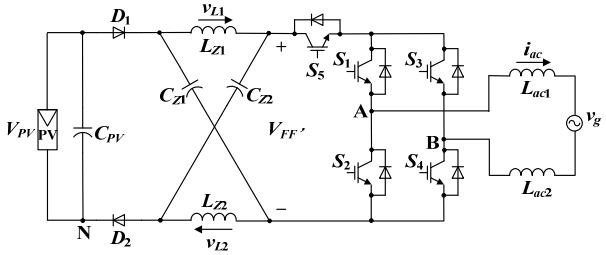


Fig. 1. Single-phase transformerless Z-source grid-connected PV inverter.

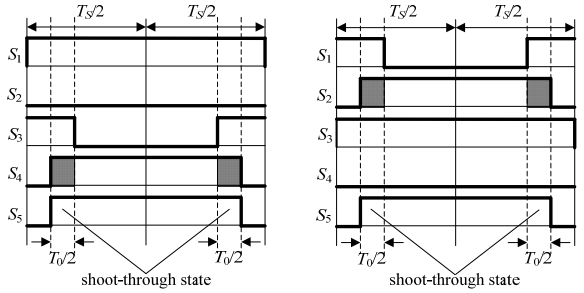


Fig. 2. Modulation strategy of ZSI-TL. (a) During the positive half cycle. (b) During the negative half cycle.

$$V_{C1} = V_{C2} = V_C \quad \text{and} \quad v_{L1} = v_{L2} = v_L . \tag{1}$$

According to the modified PWM strategy, the shoot-through duty ratio d_0 should be limited to 1-M.

Therefore, the output peak voltage of the inverter can be expressed as:

$$\hat{v}_{ab} = \hat{V}_{FF'} M = \frac{T_S}{T_1 - T_0} V_{PV} M = \frac{M}{1 - 2d_0} V_{PV} = BMV_{PV} \tag{2}$$

where $\hat{V}_{FF'}$ is the peak dc-link voltage, V_{PV} is the output voltage of the PV panel, M is the modulation index, and T_0, T_1 and T_S are the shoot-through time interval, the non-shoot-through time interval and the switching cycle, respectively. Equation (2) shows that the output voltage can be stepped up or down by choosing an appropriate boost factor, G,

$$G = BM . \tag{3}$$

If M=1-d_0, the relation between M and the maximum value for G can be obtained as:

$$G_{\max} = \frac{M}{2M - 1} . \tag{4}$$

Thus, to boost the output voltage, M ranges from 0.5 to 1.

C. Operation Mode Analysis

Fig. 3 shows the operation modes of the ZVI-TL.

1) Mode 1 is the freewheeling mode during the positive half cycle of the grid voltage. S_1 and S_3 are ON while S_2, S_4 and S_5 are OFF. The diodes D_1 and D_2 are conducting and the Z-source inductor current decreases linearly. The anti-parallel diode of S_3 conducts. Therefore, u_{AB}=0V and the output current decreases through the switch S_1 and the anti-parallel diode of S_3.

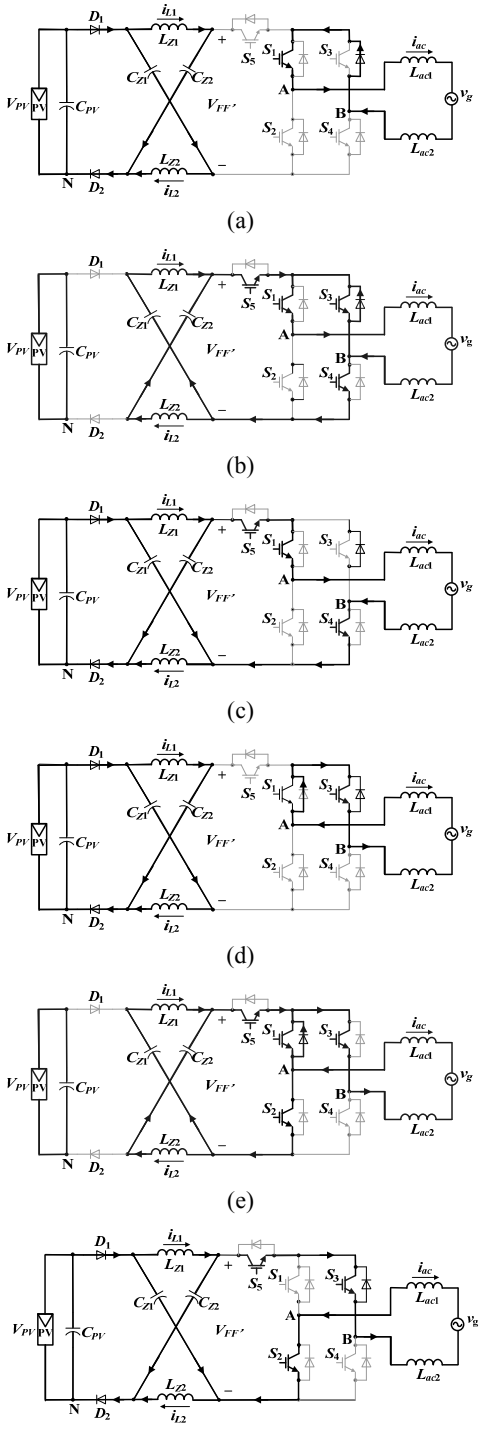


Fig. 3. Six operation modes of ZVI-TL. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

2) Mode 2 is the shoot-through mode during the positive half cycle of the grid voltage. S_1, S_3, S_4 and S_5 are ON while S_2 is OFF. The sum of the Z-source capacitors voltage is greater than the dc source voltage ($V_{C1} + V_{C2} > V_{PV}$), the diodes D_1 and D_2 are reverse-biased, and the Z-source capacitors charge the Z-source inductors.

The Z-source inductor current increases linearly, while the output current i_{ac} decreases.

3) Mode 3 is the active mode during the positive half cycle of the grid voltage. S_1, S_4 and S_5 are ON while S_2 and S_3 are OFF. The output current increases through the switches S_5, S_1 and S_4.

4) Mode 4 is the freewheeling mode during the negative half cycle of the grid voltage. S_1 and S_3 are ON while S_2, S_4 and S_5 are OFF. The diodes D_1 and D_2 are conducting. The Z-source inductor current decreases linearly. Therefore, u_{AB}=0V and the output current decreases through the switch S_3 and the anti-parallel diode of S_1.

5) Mode 5 is the shoot-through mode during the negative half cycle of the grid voltage. S_1, S_2, S_3 and S_5 are ON while S_4 is OFF. The diodes D_1 and D_2 are reversed-biased, and the Z-source capacitors charge the Z-source inductors. The Z-source inductor current increases linearly, while the output current decreases.

6) Mode 6 is the active mode during the negative half cycle of the grid voltage. S_2, S_3 and S_5 are ON while S_1 and S_4 are OFF. The output current increases through the switches S_5, S_3 and S_2.

From the above analysis, it can be seen that the shoot-through states are evenly inserted between the active states and the traditional zero states. The zero states freewheel only through S_1 and S_3.

III. Leakage Current Analysis of the ZSI-TL

A. Model of the CM Voltage

Fig. 4(a) shows the CM model for the ZSI-TL including the most significant stray elements. The most important stray elements that influence the leakage current dynamics include the stray capacitance between the PV array and the ground C_{PVg} and the series impedance between the ground connection points of the inverter and the grid Z_{pg}. The leakage current i_{cm} flows through the closed-loop path consisting of C_{PVg}, the Z-source network, the bridge, the filters (L_{ac1} and L_{ac2}), the utility grid, and Z_{pg}. Without Z_{pg} considered, the total CM voltage v_{tcm} is defined as:

$$v_{tcm} = \frac{v_{AN} + v_{BN}}{2} + \frac{L_{ac2} - L_{ac1}}{2(L_{ac2} + L_{ac1})}(v_{AN} - v_{BN}) \tag{5}$$

where v_{AN} represents the voltage between terminal (A) and terminal (N), and v_{BN} represents the voltage between terminal (B) and terminal (N).

From (5), if L_{ac1} = L_{ac2}, the total CM voltage is only relevant to v_{AN} and v_{BN}. The CM voltage v_{cm} can be given by the following:

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2}. \tag{6}$$

v_{AN} and v_{BN} are determined by the PWM strategy of the ZSI-TL. Therefore, v_{AN} and v_{BN} can be regarded as the controlled-voltage sources connected to the negative terminal

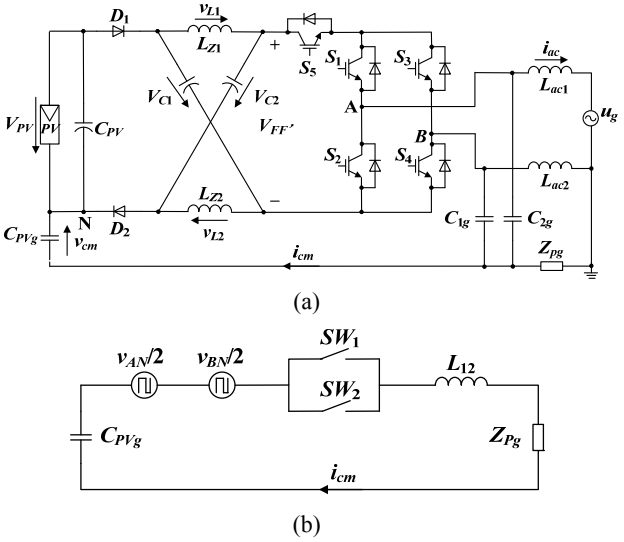


Fig. 4. Common-mode model for ZSI-TL. (a) Full model. (b) Simplified model.

of the PV array, namely a square-wave voltage sources with a switching frequency. The simplified circuit of Fig. 4(b) is finally obtained. SW_1 and SW_2 represent the diodes of the ZSI-TL. SW_1 and SW_2 are ON during the non-shoot-through states, and they are OFF during the shoot-through states. L_{12} is obtained by the following:

$$L_{12} = \frac{L_{ac1}L_{ac2}}{L_{ac1} + L_{ac2}}. \tag{7}$$

In the active modes (Mode 3 and Mode 6), the CM voltage can be expressed as:

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} = \frac{V_C + V_{PV} - V_C}{2} = \frac{V_{PV}}{2} \tag{8}$$

where $v_{AN} = V_C$ and $v_{BN} = V_{PV} - V_C$ (Taking Mode 3 as an example.).

In the freewheeling modes (Mode 1 and Mode 4), the CM voltage can be obtained as:

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} = \frac{\frac{V_{PV}}{2} + \frac{V_{PV}}{2}}{2} = \frac{V_{PV}}{2} \tag{9}$$

where $v_{AN} = v_{BN} = \frac{v_{FF'}}{2} + v_L = \frac{2V_C - V_{PV}}{2} + V_{PV} - V_C = \frac{V_{PV}}{2}$.

In the shoot-through modes (Mode 2 and Mode 5), the sum of the two Z-source capacitors' voltage is greater than the output voltage of the PV panel. Therefore, the diodes D_1 and D_2 are reverse biased. SW_1 and SW_2 are OFF so that the path for the leakage current is blocked.

According to the above analysis, because the CM voltage is kept constant during the non-shoot-through states and the discharge path of the CM voltage is blocked during the shoot-through states, the leakage current is avoided.

B. Influence of the Junction Capacitances

In the active mode, the dc and ac sides of the inverter are directly connected by the filter inductors. The operation states

and the common-mode voltage are not affected by the junction capacitance of the switches. In the freewheeling mode, the PV panel is disconnected from the grid by S_5, and the CM voltage is affected by the junction capacitances of the switches. In the shoot-through mode, because the path of the leakage current is blocked, the influence of the junction capacitances will not be considered. Therefore, when the inverter commutates from the shoot-through mode to the freewheeling mode, the slope of the voltages v_{AN} and v_{BN} depends on the junction capacitance of the switches, and the CM voltage v_{cm} is accordingly affected.

Taking the commutation from Mode 2 to Mode 1 as an example, there are two stages. The other commutation, from Mode 5 to Mode 4, is similar due to the symmetry of the operation modes.

Stage I: Fig. 5 shows the transient circuit of the commutation from Mode 2 to Mode 1, where C_{D1} and C_{D2} represent the junction capacitances of the diodes D_1 and D_2, C_1~C_5 represent the junction capacitors of the switches S_1~S_5 and D_3 represents the anti-parallel freewheeling diode of S_3. When S_4 and S_5 are turned OFF, the two charging or discharging circuits are composed of the junction capacitors C_2, C_4 and C_5. According to Kirchhof's current law, the following current equations can be obtained:

$$i_1 = i_{C5} + i_{D3} \tag{10}$$

$$i_2 = i_{C4} + i_{D3} \tag{11}$$

$$i_{C2} = i_1 - i_2 \tag{12}$$

where i_1 and i_2 represent the currents of the two charging or discharging circuits; i_{D3} is the current of D_3; and i_{C2} , i_{C4} and i_{C5} are the currents of C_2, C_4 and C_5, respectively.

From (10) to (12), the formula can be derived as follows:

$$i_{C5} = i_{C2} + i_{C4}\,. \tag{13}$$

Assuming that the acquired charge of C_{D2} is equal to the discharged charge of C_{D1}, an equivalent circuit model for the transient state can be obtained in Fig. 5(b), where the initial potentials in stage 1 are indicated in the brackets (the node N' is used as a reference potential). It is obvious that the junction capacitors C_2 and C_4 are charged by C_5 in parallel through the filter inductors L_{ac1} and L_{ac2}. Thus, the voltages v_{AN} and v_{BN} rises until their values are equal to $V_{PV}/2$, and the transient process on Stage 1 ends. Fig. 5(c) shows an equivalent circuit model at the end of Stage 1. Based on the charge conservation, it can be found that:

$$\left(V_C - \frac{V_{PV}}{2}\right)C_5 = \left[\frac{V_{PV}}{2} - \left(V_{PV} - V_C\right)\right]\left(C_2 + C_4\right). \tag{14}$$

As a result, the relation of the junction capacitors can be obtained as:

$$C_5 = C_2 + C_4\,. \tag{15}$$

Stage II: Fig. 6 shows a potential resonant circuit in Mode 1 according to (15). The voltages v_{AN} and v_{BN} become $V_{PV}/2$ synchronously only if C_5= C_2+C_4 at the end of transient state I. Therefore, the CM voltage can still remain $V_{PV}/2$. The

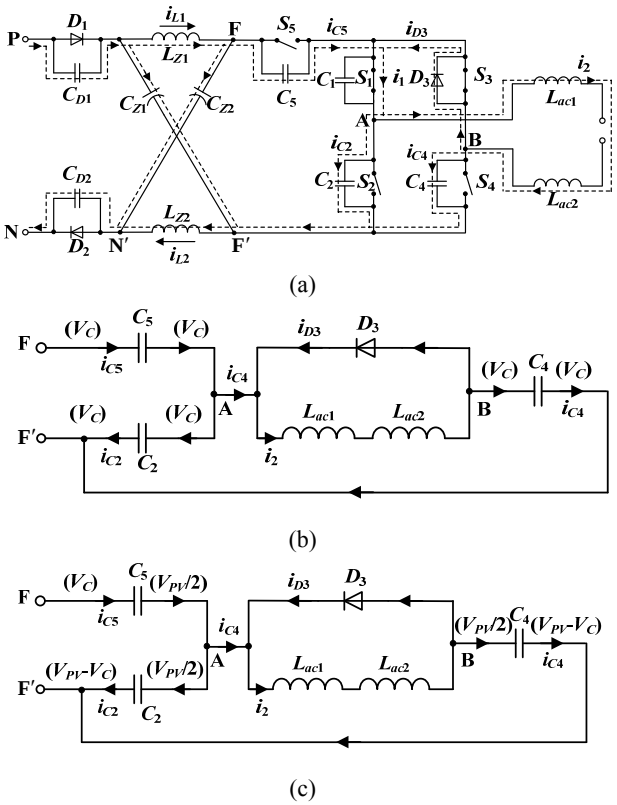


Fig. 5. Transient circuit of commutation from Mode 2 to Mode 1. (a) Transient circuit. (b) Equivalent circuit from Mode 2 to Mode 1. (c) Equivalent circuit at the end of Stage 1.

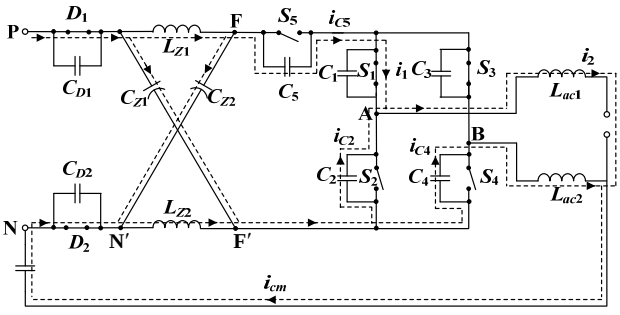


Fig. 6. Potential resonant circuit in Mode 1.

modified inverter can operate normally in Mode 1, and the condition for eliminating the leakage current is met as analyzed earlier.

IV. Power Loss Calculation and Analysis

A. Conduction Losses Analysis

Assuming that the output current is sinusoidal:

$$i_{ac} = I_{CM} \sin\alpha\,. \tag{16}$$

where i_{ac} is the output current, and I_{CM} is the peak value of the output current.

The conduction losses of S_1 can be obtained in the positive half cycle as:

$$P_{S1\_con}=\frac{1}{2\pi}I_{CM}\int_0^{\pi}\left(\frac{V_{CEN}-V_{CEO}}{I_{CN}}I_{CM}\sin^2\alpha+V_{CEO}\sin\alpha\right)d\alpha$$
$$=\frac{1}{4}\frac{V_{CEN}-V_{CEO}}{I_{CN}}I_{CM}^2+\frac{1}{\pi}V_{CEO}I_{CM} \quad (17)$$

where V_{CEO} is the saturation voltage drop, I_{CN} is the rated current, and V_{CEN} is the collector-to-emitter voltage at the rated current. This implies a threshold voltage plus a resistance drop.

In the negative half cycle, the conduction losses of S_1 during the shoot-through time interval are:

$$P_{S1\_SH}=\frac{1}{2\pi}\int_0^{\pi}\left(\frac{V_{CEN}-V_{CEO}}{I_{CN}}\times 2I_L+V_{CEO}\right)2I_L d_0 d\alpha \quad (18)$$
$$=\left(2\frac{V_{CEN}-V_{CEO}}{I_{CN}}I_L+V_{CEO}\right)I_L d_0$$

where I_L is the Z-source inductor current.

Another part of the conduction losses of S_1 is induced by the conduction of the body diode in the negative half cycle.

$$P_{S1\_D1}=\frac{1}{2\pi}\int_0^{\pi}(1-M\sin\alpha)\left(\frac{V_{FN}-V_{FO}}{I_{CN}}i_{ac}+V_{FO}\right)i_{ac}d\alpha \quad (19)$$
$$=\left(\frac{1}{4}-\frac{2M}{3\pi}\right)\frac{V_{FN}-V_{FO}}{I_{CN}}I_{CM}^2+\left(\frac{1}{\pi}-\frac{M}{4}\right)V_{FO}I_{CM}$$

where V_{FO} is the saturation voltage drop, and V_{FN} is the diode voltage drop at the rated current.

Thus, the average conduction losses of S_1 are:

$$P_{S1\_all}=P_{S1\_con}+P_{S1\_D1}+P_{S1\_SH}. \quad (20)$$

In a similar way, the average conduction losses of S_2 can be given as:

$$P_{S2\_all}=P_{S2\_con}+P_{S2\_SH} \quad (21)$$

where:

$$P_{S2\_con}=\frac{1}{2\pi}MI_{CM}\int_0^{\pi}\left(\frac{V_{CEN}-V_{CEO}}{I_{CN}}I_{CM}\sin^2\alpha+V_{CEO}\sin\alpha\right)\sin\alpha d\alpha,$$
$$=\frac{2M}{3\pi}\frac{V_{CEN}-V_{CEO}}{I_{CN}}I_{CM}^2+\frac{M}{4}V_{CEO}I_{CM}$$
$$P_{S2\_SH}=\frac{1}{2\pi}\int_0^{\pi}\left(\frac{V_{CEN}-V_{CEO}}{I_{CN}}\times 2I_L+V_{CEO}\right)2I_L d_0 d\alpha.$$
$$=\left(2\frac{V_{CEN}-V_{CEO}}{I_{CN}}I_L+V_{CEO}\right)I_L d_0$$

According to Fig. 2, the conduction losses of S_3 are equal to those of S_1, and the conduction losses of S_4 are equal to those of S_2. In addition, the conduction losses of S_5 are the sum of S_2 and S_4. Therefore, the conduction losses of the switches are:

$$P_{all}=P_{S1\_all}+P_{S2\_all}+P_{S3\_all}+P_{S4\_all}+P_{S5\_all}. \quad (22)$$
$$=2P_{S1\_all}+4P_{S2\_all}$$

B. Switching Losses Analysis

The turn-on losses, turn-off losses and recovery power losses of S_1 can be calculated from (23) to (25), respectively.

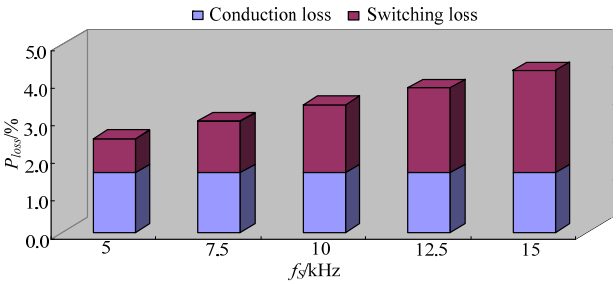


Fig. 7. Power switches loss distribution for ZSI-TL.

$$P_{S1\_ON(AV)}=\frac{(2V_C-V_{PV})I_L^2 t_{rN}}{I_{CN}}f_S \quad (23)$$

$$P_{S1\_OFF(AV)}=\frac{1}{3}(2V_C-V_{PV})I_L\left(1+\frac{I_L}{I_{CN}}\right)t_{fN}f_S \quad (24)$$

$$P_{S1\_rr}=\frac{1}{2}(2V_C-V_{PV})t_{rrN}f_S\left(0.8+0.4\frac{I_L}{I_{CN}}\right) \quad (25)$$
$$\times\left(0.35I_{rrN}+0.3\frac{I_L}{I_{CN}}I_{rrN}+2I_L\right)$$

where f_S is the switching frequency, and t_{rN} and t_{fN} are the rise and fall times of the switch at a rated current, respectively. t_{rrN} is the diodes reverse recovery time, and I_{rrN} is the peak reverse recovery current.

Thus, the switching losses of S_1 can be expressed as follows:

$$P_{S1\_S\_all}=P_{S1\_ON(AV)}+P_{S1\_OFF(AV)}+P_{S1\_rr}. \quad (26)$$

In a similar way, the average switching losses of S_2 can be given as:

$$P_{S2\_S\_all}=\frac{1}{3}P_{S1\_S\_all}. \quad (27)$$

The switching losses of S_3 are equal to those of S_1, and the switching losses of S_4 are equal to those of S_2. In addition, the switch state of S_5 is the same as that of S_4 in the positive cycle and it is also the same as that of S_2 in the negative cycle. However, the voltage across S_5 is doubled when compared with S_2 or S_4. As a result, the switching losses of S_5 are quadrupled when compared with S_2. The total switching losses of the switches are:

$$P_{S\_all(AV)}=2P_{S1\_S\_all}+6P_{S2\_S\_all}=4P_{S1\_S\_all}. \quad (28)$$

By substituting the parameters from the datasheets of an IRGP4062DPbF [25], the total losses with the change of the switching frequency are calculated. The efficiency evaluation of the ZVI-TL is shown in Fig. 7. The output power of the PV inverter is 1kW. V_{PV}=320V, V_g=220V, M=0.775, and d_0=0.1. When the switching frequency is low, the switching losses are not the main source of the power losses. However, as the switching frequency increases, the distribution of the switching losses increases gradually and becomes the main source of power losses. A lower switching frequency leads to a high total harmonic distortion (THD) of the output current. Therefore, in view of the quality of the output current and the

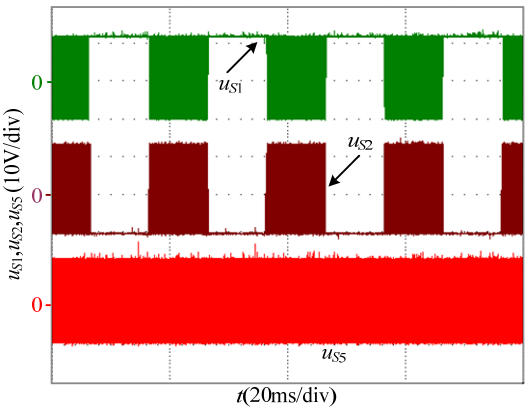
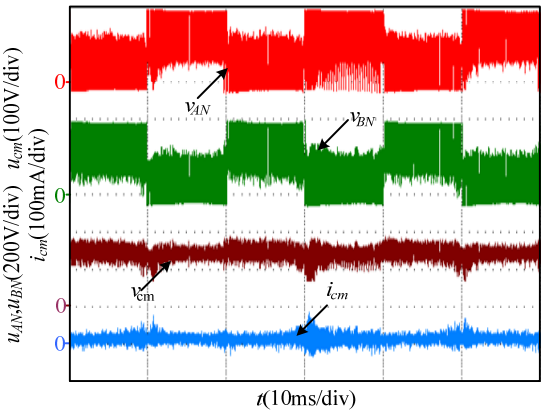
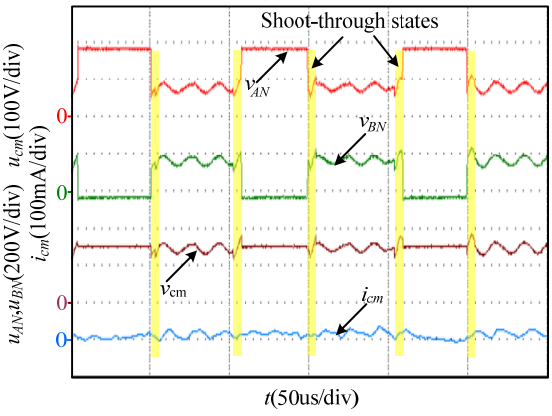


Fig. 8. Gating signals of switches.



(a)



(b)

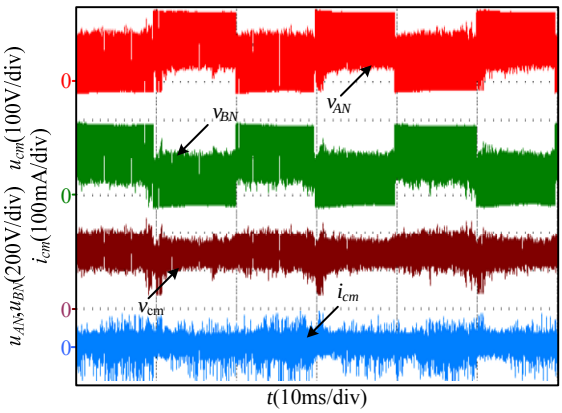
Fig. 9. Experimental waveforms of CM voltage and leakage current with paralleled capacitor. (a) Experimental waveforms in the grid cycle. (b) Experimental waveforms in the PWM cycle.

switching losses, a compromised switching frequency of 10kHz is selected in this paper.

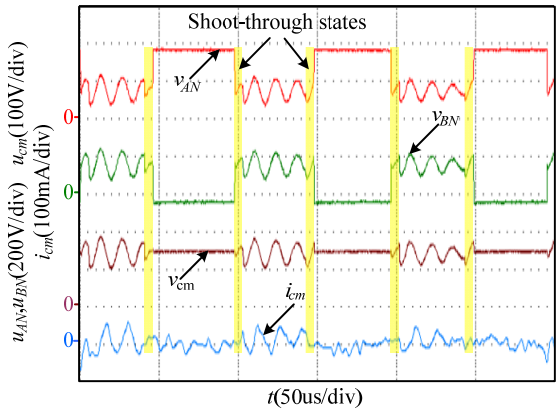
V. Experimental Results

A 1kW prototype circuit has been designed and tested to verify the performance of the proposed ZVS-TL topology.

The detailed components and parameters are as follows: input voltage, V_{PV}=320V; Z-source capacitor voltage, V_C=360V; Z-source capacitor, C_{Z1}=C_{Z2}=940μF; Z-source



(a)



(b)

Fig. 10. Experimental waveforms of CM voltage and leakage current without paralleled capacitor. (a) Experimental waveforms in the grid cycle. (b) Experimental waveforms in the PWM cycle.

inductor, L_{Z1}=L_{Z2}=4mH; filter inductor, L_{ac1}=L_{ac2}=4.5mH; grid voltage, V_g =220Vac; grid frequency, f_g=50Hz; switching frequency, f_S=10kHz; parasitic capacitor, C_{PVg}=0.1μF; power switches, S_1–S_5= IRGP4062DPbF; and junction capacitors of the switches, C_1–C_5=84pF.

The experimental gating signals in a grid cycle are shown in Fig. 8. It can be seen that the experimental gating signals u_{s1}, u_{s2} and u_{s5} agree with the analysis results of the PWM scheme, and that the gating signals of u_{s2} and u_{s5} are synchronized well in the negative half cycle.

According to the principle of the junction capacitors, one additional capacitor with a value of 84pF should be paralleled to S_5. In addition, a capacitor with a values of 82pF is applied in this prototype circuit. Because Z_{pg} is very small, it is not considered. The CM voltage and the leakage current waveforms of the ZVI-TL with a paralleled capacitor in the grid-cycle and in the PWM cycle are shown in Fig. 9(a) and Fig. 9(b). The yellow highlighted sections represent the shoot-through states. From (8) and (9), v_{AN}=360V, v_{BN}= -40V in Mode 3, and v_{AN}=v_{BN}=160V in mode 1. By choosing a reasonable value for the paralleled capacitor, 82pF, v_{AN}=v_{BN}=0.5V_{PV} is obtained at the ending point of the transient process from the shoot-through mode to the freewheeling

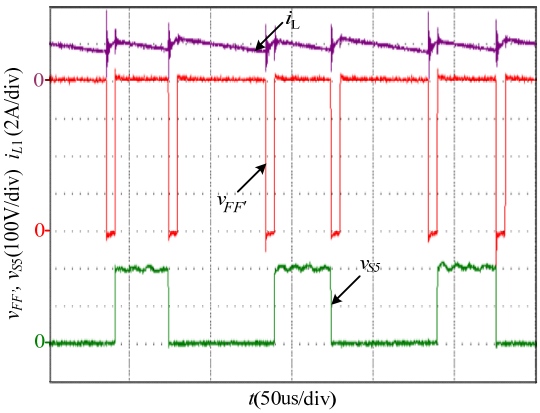


Fig. 11. Experimental waveforms of $v_{FF'}$, v_{S5} and i_L.

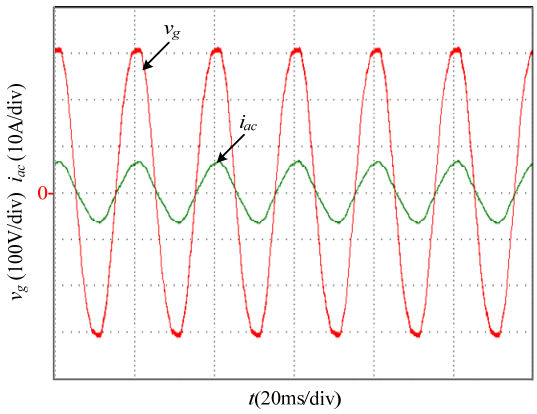


Fig. 12. Experimental waveforms of v_g and i_{ac}.

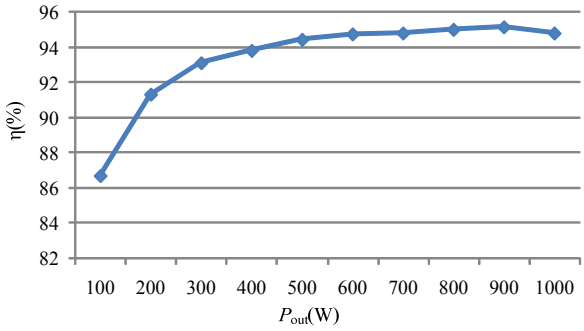


Fig. 13. Measured efficiency of ZVI-TL.

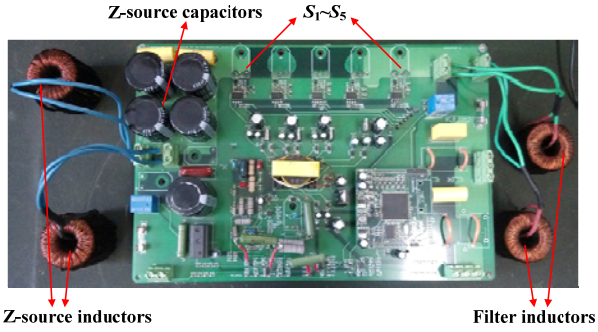


Fig. 14. Photograph of the proposed inverter.

mode. Thus, v_{cm} is maintained at approximately $V_{PV}/2$. The leakage current i_{cm} is successfully limited to a very small value that is less than 70mA for the peak value and less than 50mA for the rms value. This complies with the DIN V VDE V 0126-1-1 standard.

Fig.10 shows the CM voltage and the leakage current waveforms of the ZVI-TL without a paralleled capacitor. It can be seen that the leakage current with a paralleled capacitor is less than that without a paralleled capacitor.

Fig. 11 shows the dc-link voltage $v_{FF'}$, the collector-emitter voltage v_{S5} of S_5, and the Z–source inductor current i_L waveforms. It is clear that i_L increases in the shoot-through mode and decreases in the non-shoot-through mode. In the freewheeling modes, S_5 is OFF and v_{S5} is equal to 200V.

Fig. 12 shows the grid current and voltage waveforms. The grid-connected current is highly sinusoidal and synchronized with the grid voltage. The experimental efficiency of the Z-source PV grid-connected inverter is shown in Fig. 13. The maximum efficiency is 95.15%, including the main circuit, control board, and auxiliary power. Fig. 14 shows a photograph of the proposed inverter.

VI. Conclusion

A modified transformerless Z-source PV grid-connected inverter has been proposed in this paper. The proposed inverter has the following characteristics: (i) a decoupling switch and two reversed-biased diodes are used to eliminate the leakage current, (ii) a modified PWM strategy is implemented, which ensures a single power device switching per state transition, and retain all of the harmonic benefits of conventional modulation strategies, (iii) no shoot-through issue leads to a greatly enhanced reliability, and (iv) a low ac output current distortion can be achieved because there is no dead time. These factors make the modified Z-source inverter suitable for high efficiency and low leakage current transformerless PV grid-connected applications. Finally, experimental results obtained with a 1 kW hardware prototype verify the effectiveness of the proposed inverter.

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