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Power Conditioning for a Small-Scale PV System with Charge-Balancing Integrated Micro-Inverter

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Abstract

The photovoltaic (PV) power conditioning system for small-scale applications has gained significant interest in the past few decades. However, the standalone mode of operation has been rarely approached. This paper presents a two-stage multi-level micro-inverter topology that considers the different operation modes. A multi-output flyback converter provides both the DC-Link voltage balancing for the multi-level inverter side and maximum power point tracking control in grid connection mode in the PV stage. A modified H-bridge multi-level inverter topology is included for the AC output stage. The multi-level inverter lowers the total harmonic distortion and overall ratings of the power semiconductor switches. The proposed micro-inverter topology can help to decrease the size and cost of the PV system. Transient analysis and controller design of this micro-inverter have been proposed for stand-alone and grid-connected modes. Finally, the system performance was verified using a 120 W hardware prototype.

Key words: Micro-inverter, Multi-level inverter, Multi-output flyback converter, Total harmonic distortion

I. INTRODUCTION

Traditional large-scale power-generating stations connected to a central grid have several shortcomings because of the ever increasing demand for electrical power and its resulting complexity. Distributed Generation (DG) provides a solution for this problem because of its quick installation time unlike large-scale power stations and the added flexibility it provides to the system. DG also increases in the generation and transmission efficiency because it is located closer to consumers. Most research efforts in DG systems have mainly focused on sources with the least carbon footprints given that it has become an essential criterion for electrical power generation systems to minimize greenhouse gas emission levels. Photovoltaic (PV) solar power, wind turbine power, and fuel-cell power generation systems have become the essential research topics in this area because they have literally zero-carbon footprint [1], [2]. PV systems have higher longevity and lower operational costs among these sources because of the lack of mechanical movements and being devoid of fuel costs. Given the rapid growth in the PV system capacity and decrease in the PV panel prices, small-scale PV systems are obtaining a larger share in the market [3]-[7]. Although the PV panel costs have been largely decreased, the size and cost of the power conditioning system (PCS) that interfaces with the PV panels with the load/grid remains relatively high [7]-[10]. This work attempts to decrease the PCS size and cost used for the PV panels without compromising the IEEE standards.

The PCS for grid-connected PV systems are traditionally classified into three groups: centralized type, string type, and micro-inverters or module-integrated converters (MIC). Although the centralized and string types are suitable for large-scale PV systems, operating in optimal operating conditions during partially-shaded conditions is difficult. MIC systems are connected to each PV module separately, which allow them to achieve better energy conversion efficiency during partially-shaded conditions. These systems also have inherent advantages of manufacturing and installation costs from modularity unlike other types [11], [12]. PV micro-inverter systems can be divided into groups based on the number of converters used, such as single-stage, two-stage, or sometimes three-stage systems. A single-stage has only one converter that connects the PV module to the grid as the name suggests. Two-stage micro-inverter systems are generally preferred because of the wide range of PV voltage and reduction in the value of the power decoupling capacitor

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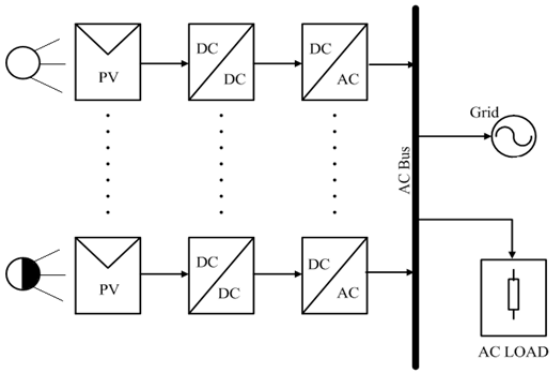


Fig. 1. Configuration of a PV system with parallel MIC modules connected to the grid and residential loads.

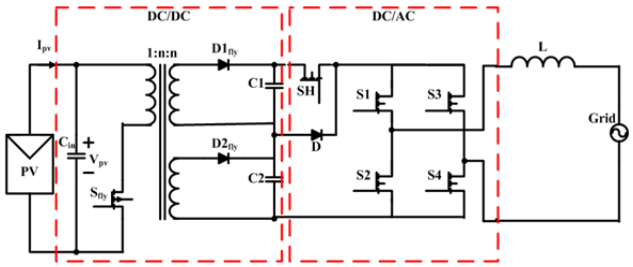


Fig. 2. Complete circuit diagram of the proposed two-stage multi-level PCS.

compared with single-stage systems [13]. However, the operation and control of micro-inverter-based systems in the standalone mode was rarely approached in literature. The PV system is stably connected to the grid under normal operating conditions. However, the standalone mode is sometimes necessary when a fault occurs in the grid and the local load should remain working (Fig. 1). In this case, one of the micro-inverter modules should maintain the AC bus stable in the normal range, whereas the other modules work in the grid-connection mode. This paper presents a small-scale PCS that uses a multi-level inverter with an integrated cell-balancer and analyzes it in both grid-connected and stand-alone operating modes. The controllers for both modes are then derived.

The operating principles of the newly suggested PV system architecture of the abovementioned multi-level inverter and flyback converter are explained in Section II. Consequently, the derivation and validation of the state-space averaged linear transfer functions for the converter stages that use small-signal modeling is shown in Section III. Section IV discusses the design procedure of the digital controller used for the stable operation of the system in stand-alone and grid-connected modes. The experimental setup and results of the hardware prototype are shown Section V. Section VI concludes this paper.

II. Proposed Small-Scale PCS

A two-stage PCS generally consists of a DC–DC converter to boost the PV and an inverter that converts the boosted DC to an AC output connected to the grid or local loads. Figure 2 shows the schematic of the proposed small-scale PCS in a grid connection.

A. Multi-Output Flyback Converter

One of the main purposes of a pre-stage DC–DC converter is to boost the PV module voltage up to the DC-link so that the inverter can provide the AC output with the desired specifications. The DC–DC converter used for boosting the PV voltage can employ either an isolated or non-isolated converter. Given that the voltage should be balanced between the two input capacitors (C1 and C2) of the multi-level inverter, an active voltage balancing circuit becomes mandatory in this study. Active balancing circuits have been extensively used in electric vehicles to balance the voltage of individual batteries. They can be divided into two major groups, namely, magnetic-coupling and capacitive-coupling balancing methods. Among these circuits, the multi-output flyback converter has been selected for this two-stage converter scheme (Fig. 2). Flyback-based converter schemes have received positive reviews because of the fewer components and potential low cost [14]-[16]. The multi-winding transformer in the flyback provides not just isolation and energy transfer but also performs accurate voltage balancing.

The voltage balancing strategy becomes simple in the case of a multi-output flyback converter. By the same turns-ratio for the secondary and tertiary outputs in the transformer, the rectified voltage should balance each other regardless of the switch duty cycle. Fig. 2 shows that the secondary and tertiary windings balance the top capacitor (C1) and bottom capacitor (C2), respectively. This inductive-coupling multiple-secondary scheme helps to minimize the required components, which lowers the cost and size of the proposed small-scale PCS. Additionally, the maximum power point tracking (MPPT) for the PV module can be achieved using the multi-output flyback converter in grid-connected systems. The DC-link voltage for the inverter can be balanced from the inverter stage in grid-connected systems, which allows the application of the MPPT scheme through the multi-output flyback converter.

B. Multi-Level Inverter

Multi-level inverters are traditionally used in high-power industrial applications. However, they are increasingly used in renewable energy systems because of their inherent advantages over conventional two-level inverters [17–20]. Multi-level inverters produce a staircase output waveform with low distortion, so it aids in decreasing electromagnetic (EM) compatibility problems. It also draws the input current with low distortion and decreases the *dv/dt* stresses [21]. They can be operated in either fundamental frequency or high switching frequency pulse width modulation (PWM). A clear disadvantage of multi-level inverters is the utilization of a

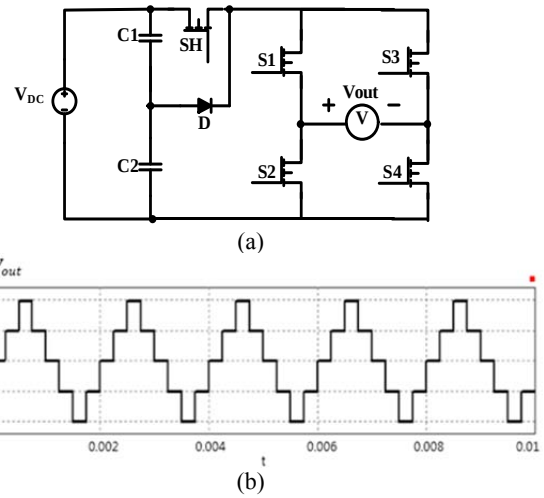


Fig. 3. Low-power multi-level inverter topology and output. (a) Modified H-bridge topology. (b) 5-level output voltage waveform.

TABLE I
COMPARISON OF THE NUMBER OF SWITCHING COMPONENTS IN DIFFERENT MULTI-LEVEL INVERTER TOPOLOGIES

Topology type	Switches	Diode	Capacitor
Cascaded	8	0	2
Modified	5	1	2
FCAH	6	0	2

higher number of power switches compared with conventional H-bridge inverters. Although the voltage ratings are lower, the large number of switches increases the complexity of the gate driver circuit. Therefore, current multi-level studies have attempted to tackle this problem by proposing new multi-level inverter topologies. The current work selects a recently proposed multi-level inverter topology, which is a modified H-bridge topology with a 5-level output [22]. Unlike well-known multi-level topologies such as cascaded H-bridge and flying capacitor asymmetric H-bridge (FCAH), the selected topology is ideally suited for small-scale PCS. In contrast, previous topologies are designed for high-power applications that share the power transfer between the cascaded H-bridge modules. Fig. 3 shows a circuit diagram of the selected multi-level inverter with its output waveform. This topology has fewer switching components compared with conventional multi-level inverters with a 5-level output. This feature helps to lower the overall system cost and complexity of the gate driver circuit and controllers. Table I shows the comparison of the component number in each circuit. However, a drawback of the inverter topology is that because the average and instantaneous currents of SH and D are completely different, a reliable external voltage balancing circuit is necessary to maintain each of the capacitor voltages.

Several modulation techniques have been used for the multi-level topologies such as space vector modulation,

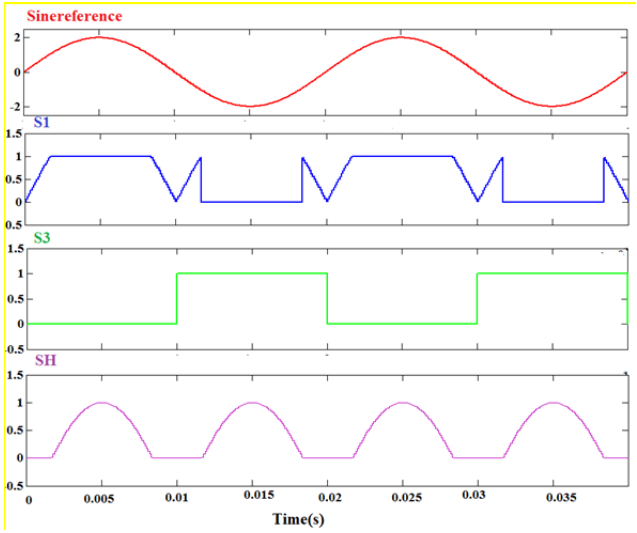


Fig. 4. Reference signals used in the PWM generation of S1, S3, and SH.

TABLE II
SWITCHING STATES OF THE INDIVIDUAL SWITCHES ACCORDING TO THE OUTPUT VOLTAGE LEVELS (1 = ON, 0 = OFF)

Output Voltage	S1	S2	S3	S4	SH
V_{DC}	1	0	0	1	1
$V_{DC/2}$	1	0	0	1	0
0	0	1	0	1	0
$-V_{DC/2}$	0	1	1	0	0
$-V_{DC}$	0	1	1	0	1

selective harmonic elimination, and sinusoidal PWM (SPWM). Among these, SPWM is one of the most simple and widely used modulation techniques. Instead of using the rudimentary form of SPWM technique, a technique combined with a modified unipolar switching strategy has been employed in this study [23]. An advantage of such a strategy is that one of the legs that contain two switches always operates at the fundamental frequency of the output, whereas the remaining three switches operate under the switching frequency (f_{sw}). Fig. 4 shows each of the reference signals used in the PWM generation for individual switches. Each signal is derived from the fundamental sinusoidal waveform reference. The reference signals for switches S2 and S4 are inherently the complementary signals of S1 and S3, respectively. Notably, the frequency of PWM outputs for switches S3 and S4 is the fundamental frequency of the output. Thus, the leg (S3 and S4) always operates under the fundamental frequency of the output. This modulation effectively helps lower the switching losses that occur in the inverter and high-frequency EM interference (EMI) noises. The frequency modulation ratio (m_f) was selected as an odd integer to lower the even-order harmonics in this strategy. Table II shows the switch state of all the individual switches that correspond to the output voltage levels.

III. System Modelling

A. Grid-Connected Multi-Level Inverter Modeling

The grid-connected inverter is regulated by a two-loop control, such as an inner loop of the inductor current and outer loop of the DC-link voltage. The corresponding transfer functions should be first derived for the controller design. The state equations of the grid-connected modified H-bridge inverter can be obtained by examining the equivalent circuit in each operating mode. Fig. 5 depicts the current flow path and switching operation under different voltage levels. When the output voltage is zero, switches S2 and S4 are turned ON (mode 1). When the output voltage is $V_{DC/2}$, the diode is forward biased and switches S1 and S4 are turned ON (mode 2). Similarly, when the output voltage is V_{DC}, switches SH, S1, and S4 are turned ON (mode 3).

From each of the above diagrams, the state equations of the inductor current under different voltage levels are derived as follows:

$$L\frac{di_L}{dt} = -V_o \quad \text{(mode 1)}$$

$$L\frac{di_L}{dt} = \frac{1}{2}V_{DC} - V_o \quad \text{(mode 2)}$$

$$L\frac{di_L}{dt} = V_{DC} - V_o \quad \text{(mode 3)} \qquad (1)$$

When switch S1 is turned ON and the state-space averaging technique is applied, the control-to-inductor current transfer function is derived as follows:

$$\frac{\hat{i}_L}{\hat{d}_1} = \frac{V_{DC}}{2sL} \qquad (2)$$

where d_1 is the duty applied to switch S1. Similarly, when the top switch SH is turned ON, the control-to-inductor current transfer function is derived as follows:

$$\frac{\hat{i}_L}{\hat{d}_2} = \frac{V_{DC}}{2sL} \qquad (3)$$

where d_2 is the duty applied to switch SH. Eqs. (2) and (3) show that the input voltage V_{DC} has a significant influence on the inductor current, but the inverter has a large capacitor at the input. Thus, we can assume that the voltage is constant.

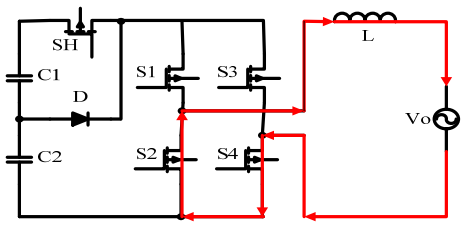
The control-to-v_{DC} should be derived for the outer loop controller design. The output power equals the input power in the case of an ideal inverter.

$$v_{DC} \cdot i_{DC} = v_o \cdot i_o \qquad (4)$$

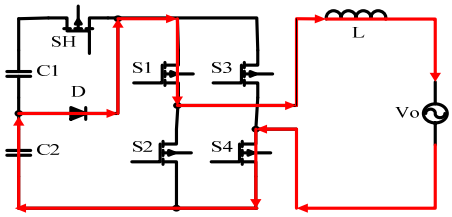
The input quantities v_{DC} and i_{DC} are the DC-link parameters, whereas the output quantities v_o and i_o are rms values. The controllers are designed in such a way that the inner loop controller is always much faster than the outer loop controller. We assume that the output current tracks its reference without any error. Therefore, the output current is assumed to be the multiplication of the phase-lock-loop (PLL) output and control voltage.

$$i_o = \frac{v_o}{k} v_{con} \qquad (5)$$

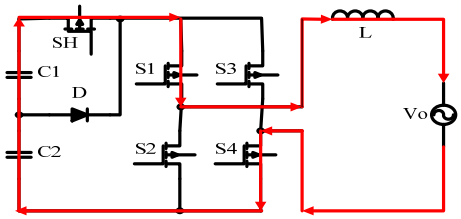
where k is the scaling factor, and v_{con} is the control voltage from the outer loop controller. Eq. (6) is obtained using Eqs. (4) and (5).



(a) Mode 1.



(b) Mode 2.



(c) Mode 3.

Fig. 5. Current flow according to the output voltage levels. (a) Mode 1(Vo = 0). (b) Mode 2 (Vo = $V_{DC/2}$). (c) Mode 3 (Vo = V_{DC}).

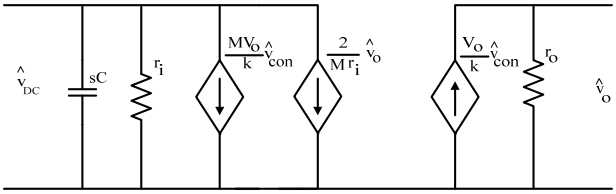


Fig. 6. Small-signal circuit diagram of the inverter.

$$\frac{v_o^2}{k} v_{con} = V_{DC} \cdot i_{DC} \qquad (6)$$

The value of the modulation index M of the modified H-bridge inverter can be derived as follows:

$$M = \frac{V_{DC}}{V_o} = \sqrt{\frac{k}{(v_{con} r_i)}} \qquad (7)$$

where r_i is the small-signal resistance of the input. Introducing the perturbation to the above Eqs. (5), (6), and (7), we can obtain Eqs. (8) and (9):

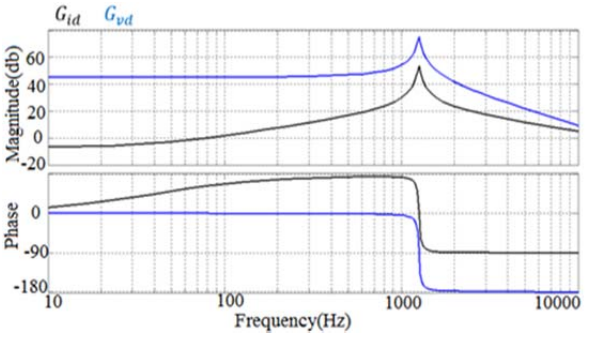
$$\hat{i}_1 = \frac{2}{M r_i}\hat{v}_o + \frac{M v_o}{k}\hat{v_{con}} - \frac{1}{r_i}\hat{v_{DC}} \qquad (8)$$

$$\hat{i}_o = \frac{V_o}{k}\hat{v_{con}} + \frac{1}{M^2 r_i}\hat{v}_o \qquad (9)$$

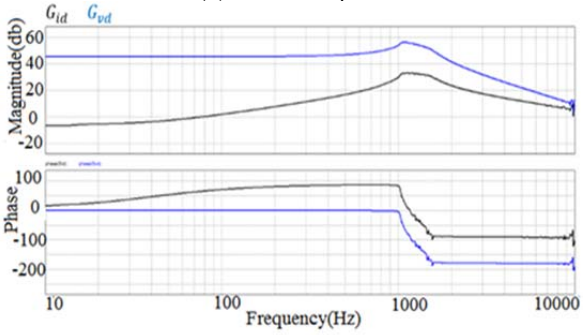
The small-signal model can be obtained from Eqs. (8) and (9) as shown in Fig. 6. The output small-signal resistance (r_o) is given by the following:

$$r_o = -r_i M^2 \qquad (10)$$

The small-signal circuit model shows that the expression for the control control-to-DC-link voltage (V_{DC}) transfer function can be derived as Eq. (11):

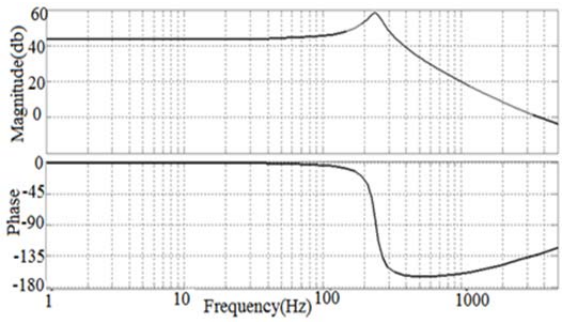


(a) MATLAB plot.

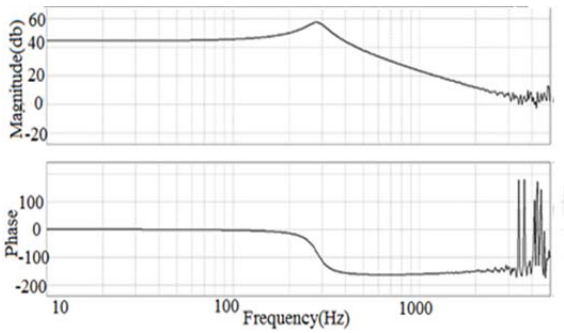


(b) PSIM plot.

Fig. 7. Bode plots of G_{vd} and G_{id}. (a) Derived transfer function with MATLAB. (b) Numerical simulation PSIM.



(a) Analytical model.



(b) Numerical simulation.

Fig. 8. Bode plot of G_{vd}. (a) Derived transfer function with MATLAB. (b) Numerical simulation by PSIM.

$$\frac{\widehat{v_{DC}}}{\widehat{v_c}} = \frac{MV_o}{k}\left[\frac{r_i}{2+sCr_i}\right] \quad (11)$$

B. Multi-Level Inverter Modelling under Standalone Mode

In the standalone operating condition, the flyback converter starts to regulate the DC-link voltage instead of the MPPT control. The following inverter also starts to generate the output AC voltage. The state equations of the modified H-bridge topology at each of the output levels are provided below.

$$L\frac{di_L}{dt} = -v_c \qquad C\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \qquad \text{(mode 1)}$$

$$L\frac{di_L}{dt} = \frac{1}{2}v_{DC} - v_o \qquad C\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \qquad \text{(mode 2)}$$

$$L\frac{di_L}{dt} = v_{DC} - v_o \qquad C\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \qquad \text{(mode 3)} \quad (12)$$

The transfer functions of the control-to-output and control-to-inductor current are derived using the state-space averaging technique as shown in Eqs. (13) and (14), respectively.

$$\frac{\widehat{v_o}}{\hat{d}} = \frac{V_{DC}}{2+2sLC^2+2\frac{sL}{R_o}} \quad (13)$$

$$\frac{\widehat{i_L}}{\hat{d}} = \frac{\frac{1}{2}V_{DC}}{sL+\frac{1}{sC+1/R_o}} \quad (14)$$

The derived transfer functions can be validated by comparing them with the exact models in PSIM as shown in Fig. 7.

C. Multi-Output Flyback Converter Modeling under Grid Connection

Similar to the modified H-bridge topology, the state equations of the multi-output flyback converter can be obtained by examining the current flow during switch ON and OFF conditions. The state equations when the switch is turned ON are shown in Eq. (15) as follows:

$$C\frac{dv_{pv}}{dt} = i_{sa} - i_i = \frac{(v_i - v_{pv})}{R_{sa}} - i_i$$

$$L\frac{di_L}{dt} = v_{pv} \quad (15)$$

The state equations when the switch is turned OFF are shown in Eq. (16):

$$C\frac{dv_{pv}}{dt} = i_{sa} = \frac{(v_i - v_{pv})}{R_{sa}}$$

$$L\frac{di_L}{dt} = \frac{v_{DC}}{n} \quad (16)$$

where V_{DC} is the flyback converter output voltage. Using the state-space averaging technique, the linearized transfer function for the control-to-input voltage is derived as Eq. (17):

$$G_{vd} = \frac{\widehat{v_{pv}}}{\hat{d}} = \frac{-I_L - \frac{(V_{DC}D+\frac{V_oD}{n})}{sL}}{sC+\frac{1}{R_{sa}}+\frac{D^2}{sL}} \quad (17)$$

The derived linearized transfer function can be verified by comparing it with the bode plot of the exact model in PSIM. Fig. 8 shows the bode plots of the averaged model and exact model, which matching each other.

D. Flyback Converter Modeling under Standalone Operation

In the case of standalone operation, the function of the DC–DC converter is to provide a fixed DC-Link voltage to the multi-level inverter. The characteristics of the control-to-output voltage should be analyzed to develop the controller. Fig. 9 shows the equivalent circuit of the flyback converter

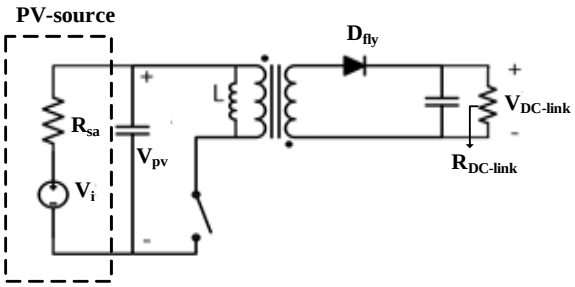


Fig. 9. Equivalent circuit diagram of the flyback converter with a PV source in standalone mode.

TABLE III
STATE EQUATIONS OF THE FLYBACK CONVERTER

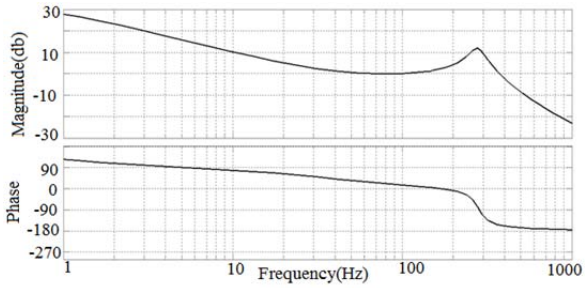
	Switch ON	Switch OFF
Input Voltage	$C\frac{dV_{pv}}{dt} = i_{sa} - i_L = \frac{(V_i - V_{pv})}{R_{sa}} - i_L$	$C\frac{dV_{pv}}{dt} = i_{sa} = \frac{(V_i - V_{pv})}{R_{sa}}$
Transformer Current	$L\frac{di_L}{dt} = V_{pv}$	$L\frac{di_L}{dt} = -\frac{V_{DC}}{n}$
Output Voltage	$C\frac{dV_{DC}}{dt} = \frac{V_{DC}}{R_{DC}}$	$C\frac{dV_{DC}}{dt} = \frac{i_L}{n} - \frac{V_{DC}}{R_{DC}}$

with a single output in the standalone operation. The state equations can be derived from the equivalent circuit diagram as shown in Table III. The control-to-output transfer function is derived for the flyback converter shown in Eq. (18). The derived transfer function can be validated by comparing them with the averaged model plot in MATLAB and exact model plot in PSIM as shown in Fig. 10.

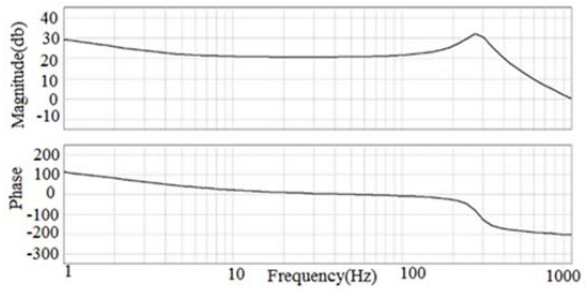
$$\frac{\widehat{v_{pv}}}{\hat{d}} = \left(\frac{I_L}{n} + \frac{(1-D)}{n}\frac{(v_{DC}+\frac{v_{DC}}{n}-\frac{DI_L}{sC_o+\frac{1}{R_{sa}}})}{(sL+\frac{D^2}{sC_o+\frac{1}{R_{sa}}})}\right)\Bigg/\left(sC_o + \frac{1}{R_{DC}} + \frac{\frac{(1-D)^2}{n^2}}{(sL+\frac{D^2}{sC_o+\frac{1}{R_{sa}}})}\right) \quad (18)$$

IV. CONTROLLER DESIGN

This section present the design process of the digital controllers used for the stable operation of the converter in standalone and grid-connected modes. The high-frequency PWM (f_{sw}) was set at 20 kHz for both the flyback converter and multi-level inverter switches. The value of the input capacitor of the flyback converter was set as 300 µF to ensure that the PV module ripple voltage was less than 1%. The turn-ratio of the multi-output transformer was 1:3:3. The magnetizing inductance was twice the boundary value at 600 µH to ensure the CCM mode of operation in the flyback converter. The capacitor used for the DC-link voltage should lower the 120 Hz ripple to less than 5% of the DC-link voltage. The value of 600 µF was selected for both of the DC-link capacitors. Given that the output voltage of the multi-level inverter is a 5-level staircase waveform, the low



(a) Analytical model.



(b) Numerical model.

Fig. 10. Bode plot of G_{vd}. (a) Derived transfer function with MATLAB. (b) Numerical simulation by PSIM.

values of 1.3 mH and 2 µF are sufficient for the inverter LC filters. The validated transfer functions derived in the previous sections are utilized to design the feedback controllers. The controller function *H(s)* is presented in continuous domain in Eq. (19). The bilinear transformation is applied to the controller function to obtain the digital form of the controllers shown in Eq. (20).

$$H(s) = K_p + \frac{K_i}{s} \quad (19)$$

$$Y(n) = \left(\frac{2K_p + K_i T_s}{2}\right)X(n) + \left(\frac{K_i T_s - 2K_p}{2}\right)X(n-1) + Y(n-1) \quad (20)$$

A. Standalone Mode

In the case of standalone operation, the flyback converter should provide a constant DC-link voltage independent from the operation of the multi-level inverter stage. This condition is achieved using a voltage loop PI controller. The DC-link voltage is fed back to the controller, and then the PI controller is used to eliminate the error voltage by varying the duty-cycle given to the switch of the flyback converter. The cut-off frequency of the controller was set at 50 Hz. The K_p and K_i values of the designed controller are 4396330.77 and 33817.751, respectively. Fig. 11 shows the closed loop performance of the designed controller. The control dynamics indicate the characteristics of the open-loop transfer function and designed controller, respectively. The red line indicates the closed loop performance of the flyback converter in standalone operation. The figure shows that the controller provides a 110° phase margin that guarantees the stability.

In standalone mode, the multi-level inverter is controlled using a two-loop controller, inner-loop that controls the inductor current, and outer loop that controls the output

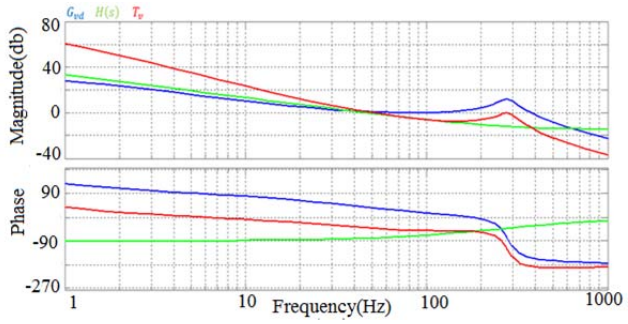


Fig. 11. Bode plot of the dynamic characteristics of the closed loop flyback converter. G_{vd}: control-to-output, H(s): Controller, T_v: Loop-gain.

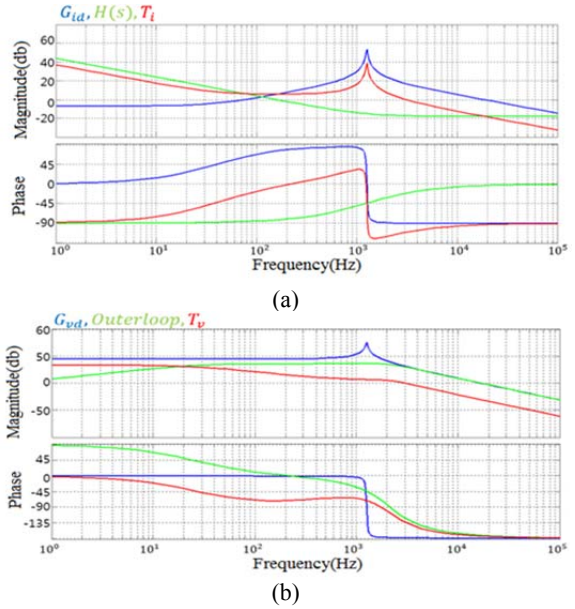


Fig. 12. Bode plot of the designed feedback loop. (a) G_{id}: control-to-inductor current, $H_i(s)$: Inner loop controller, T_i: Inner loop-gain. (b) G_{vd}: control-to-output voltage, Outer loop controller, T_v: Outer loop-gain.

voltage. The cut-off frequency of both the control loops was set at 3 kHz. Given that the digital controllers decrease the phase margin by the sample and hold effect, an excessive phase margin of 70 degrees was selected.

The designed PI control values for the inner and outer loops are K_p = 480000, K_i = 96000, and K_p = 768230, K_i = 2926242.6, respectively. Figs. 12(a) and 12(b) show the Bode plots of the inner and outer loop characteristics, respectively.

Three PWM signals are generated to control the inverter switches using the modified unipolar strategy in Table II. Fig. 13 shows the complete circuit diagram of the power stages with the digital controller in standalone mode.

The controller was simulated in PSIM software to test its functionality. A reference of 110 V_{AC} was selected for the load, whereas the DC-link reference was set at 200 V. The results show that the designed controllers successfully track each of the references as shown in Fig. 14. The flyback capacitors also have an equivalent voltage level (V_{DC1}, V_{DC2}), although the multi-level inverter draws the input current in imbalance between the switch (SH) and diode (D).

B. Grid-Connected Mode

The focal point of the controller moves to the MPPT operation in case of a grid-connected operation. The DC-link voltage is fixed by the inverter stage in this mode. The MPPT algorithm is perturb-and-observe (P&O). PV-voltage control is used to track the reference provided by the P&O algorithm. The coefficients of the PI controller K_p and K_i were calculated as 224545.5 and 102066.12, respectively. Fig. 15 shows the closed-loop characteristics of the designed controller with a sufficient phase margin of 70° that guarantee the system stability. Fig. 16 shows the circuit diagram of the PCS with its controller scheme under grid connection. The parameters V_{pv} and I_{pv} are used to calculate the V_{ref} in the P&O MPPT algorithm.

The controller of the inverter part includes a PLL, an outer voltage loop that regulates the DC-Link voltage, and an inner current loop for the output current control. Eqs. (3) and (11) show that design of the PI controllers for the voltage and current loops. The bode plots of both loops are shown in Fig. 17. The cut-off frequency of the current loop was set at 600 Hz, whereas the cut-off frequency of 5 Hz was selected for the voltage loop. The simulation results that verify the feasibility of the control design is presented in Fig. 18. The MPP voltage was located at 38 V, and 110 V is the grid voltage.

V. Experimental Results

A 120 W hardware prototype was realized to verify the proposed charge-balancer integrated multi-level PV-PCS. The selected specifications for the hardware prototype are provided in Table IV. The inductance L_o is 1.3 mH, which is relatively smaller than that of conventional 2-level or 3-level inverters. Texas Instruments DSC TMS320F28335 was used to execute the designed controllers in the hardware prototype. Fig. 19 shows the 5-level inverter output voltage waveform. The step of the voltage level is even because of the flyback charge balancer. Fig. 20 shows a closed-loop result of the PCS under standalone operation with a 200 V DC-Link voltage and 110 V reference. The experimental data was collected from the oscilloscope and used to accurately calculate the THD value in the MATLAB FFT scope. Fig. 21 shows the measured THDs of the output voltage at 4.43%.

A dual PV-array simulator (TerraSAS ELGAR) was used to emulate a real PV module (100W SM100-24). The module and array parameters, as well as the external conditions such as the solar radiation and temperatures, are all represented in the simulator. The simulator is remotely controlled by a desktop computer, whereas data acquisition is provided by the simulation software.

The PV system is tested under a changeable weather

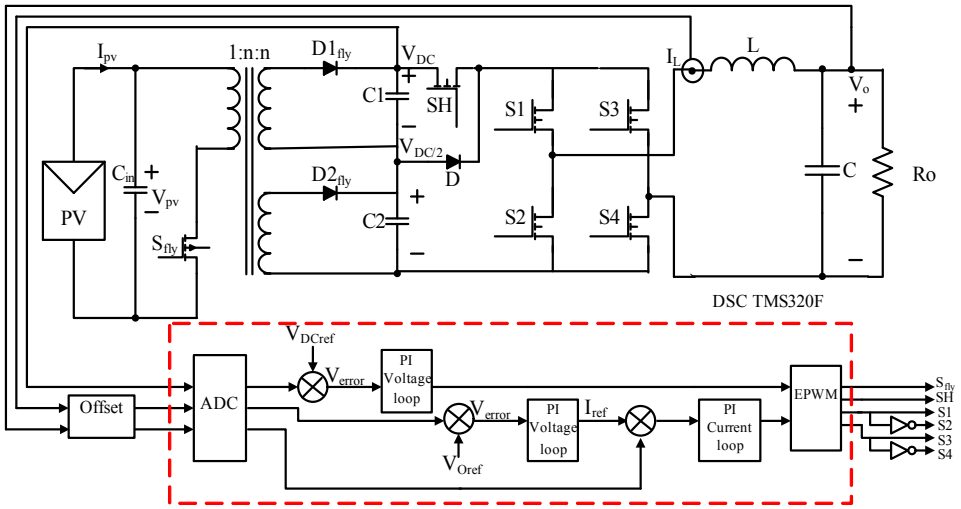


Fig. 13. Circuit and controller diagram of the proposed two-stage multi-level inverter closed-loop PCS under standalone mode.

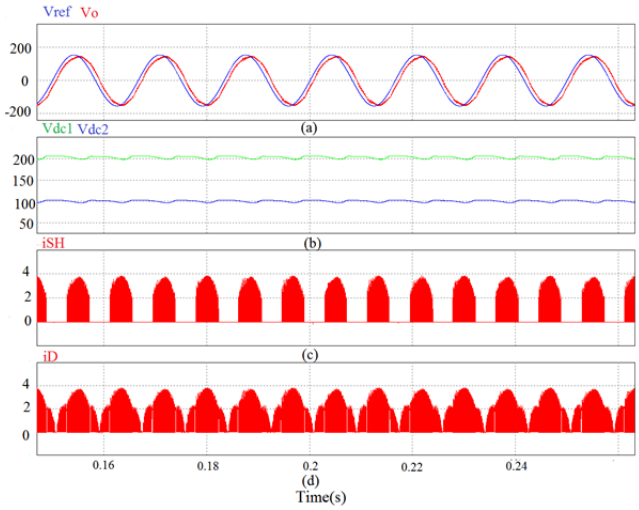


Fig. 14. Simulation result for the standalone control scheme. (a) 110 V_{AC} reference vs. load voltage. (b) 200 V DC-Link voltage. (c) Top switch (SH) current. (d) Diode current.

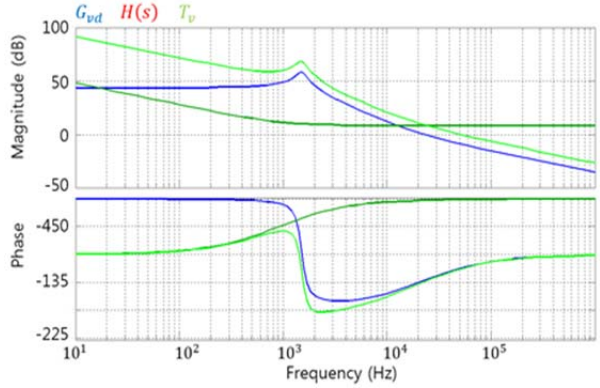


Fig. 15. Bode plot for the closed loop operation of the voltage loop PI controller for MPPT. G_{vd}: control-to-input voltage, H(s): Voltage controller, T_v: Loop-gain.

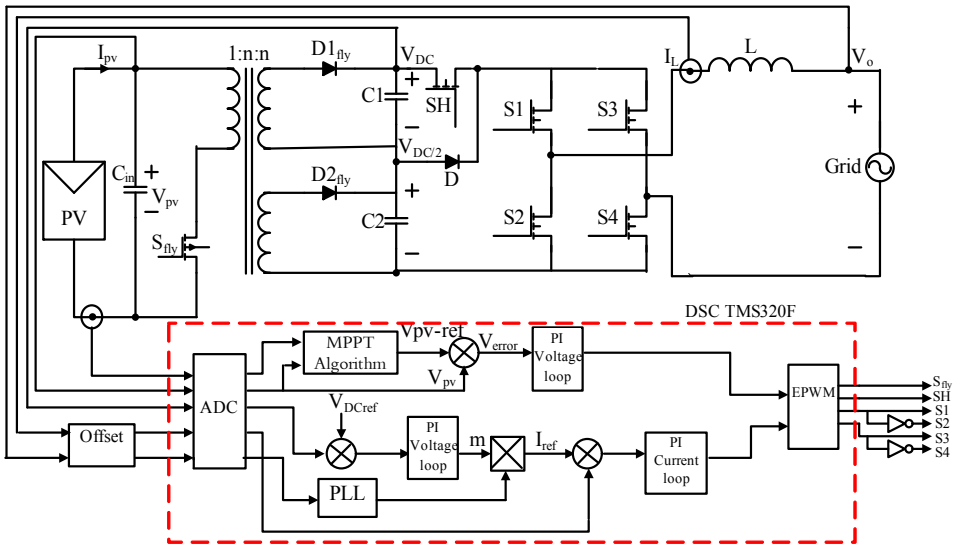
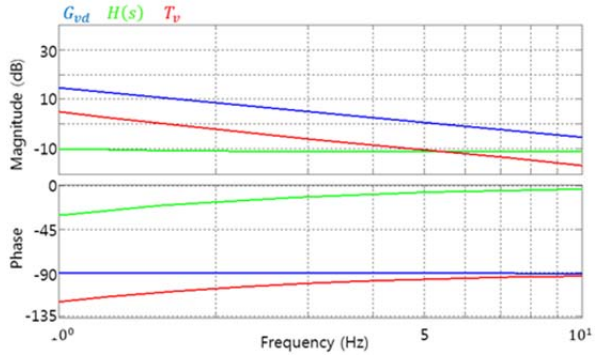
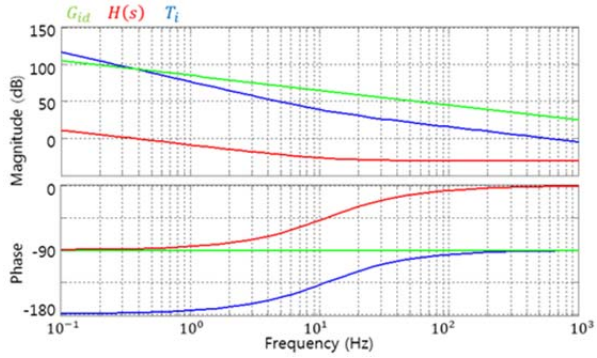


Fig. 16. Circuit and controller diagram of the closed-loop PCS in grid-connected mode with MPPT operation.



(a)



(b)

Fig. 17. Bode plots of the designed feedback loop gain. (a) Voltage loop G_{vd}: control-to-DC-link voltage, H(s)-Outer loop controller, T_v: Outer loop gain. (b) Current loop G_{id}: control-to-inductor current, H(s)- Inner loop controller, T_i: Inner loop gain.

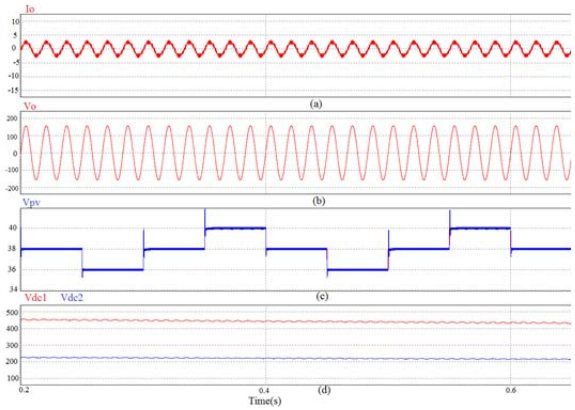


Fig. 18. Simulation results for the grid-connected control scheme. (a) Grid current, (b) grid voltage, (c) PV-source voltage (V_{pv}), MPP (38 V), and (d) balanced DC-Link capacitor voltages.

TABLE IV
SPECIFICATIONS AND DESIGN OF THE HARDWARE PROTOTYPE

Parameters	Values
Solar array voltage [$V_{pv(mpp)}$]	34 V
Solar array current [$I_{sa(mpp)}$]	3 A
Switching frequency [f_{sw}]	20 kHz
Magnetizing inductance (L_{fly})	600 uH
Turns ratio	1:3:3

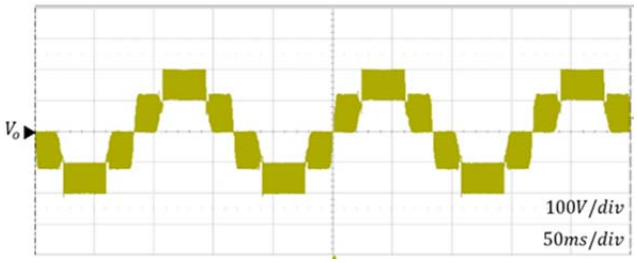


Fig. 19. 5-level inverter output voltage.

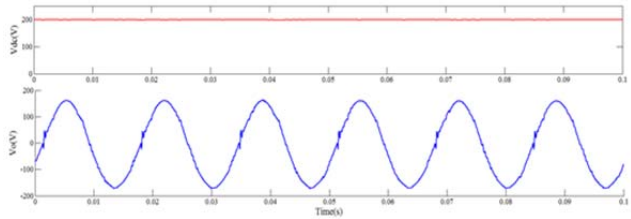


Fig. 20. DC-link voltage (V_{DC}) and load voltage (V_o) during the standalone operation.

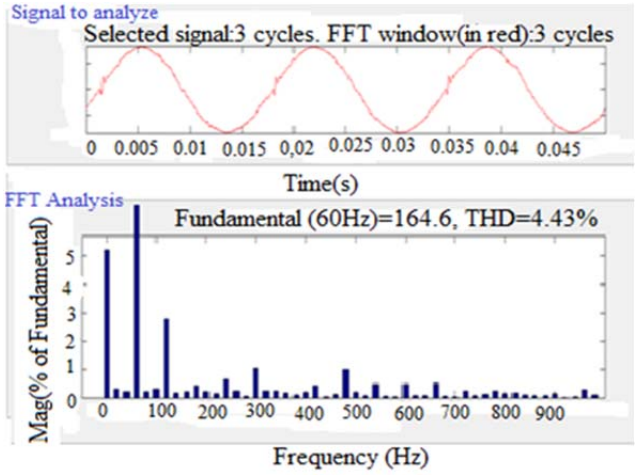


Fig. 21. Calculation of the inverter hardware output voltage THD (4.43%) using MATLAB FFT scope.

condition of constantly varying temperature and irradiance profiles to evaluate the MPPT and charge-balancing performance. Fig. 22 shows the variation of a cloudy dayprofile, including a time period from points (a) to (b), applied to test the hardware prototype. The time and voltage steps of the P&O algorithm were set as 0.1 sec and 2 V, respectively. The results in Fig. 23(a) show that the controller unit tracks the varying maximum power point rapidly and accurately, even under the fast-changing conditions of solar radiation and temperature over a period of 2 hours. Fig. 23(b) shows the short-time (250 seconds) variation of the PV voltage and current to check the MPPT performance of the controller that responds to the varying atmospheric conditions. The MPPT efficiency is almost 100% and at least 90%. Finally, Fig. 24 shows that the capacitor voltages share the partial DC-link voltage evenly.

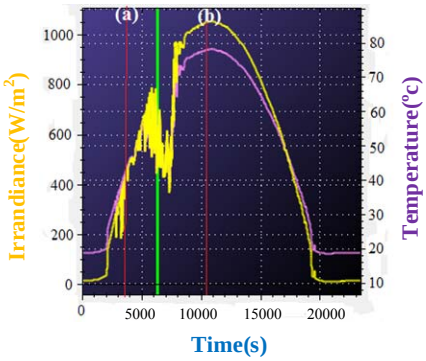
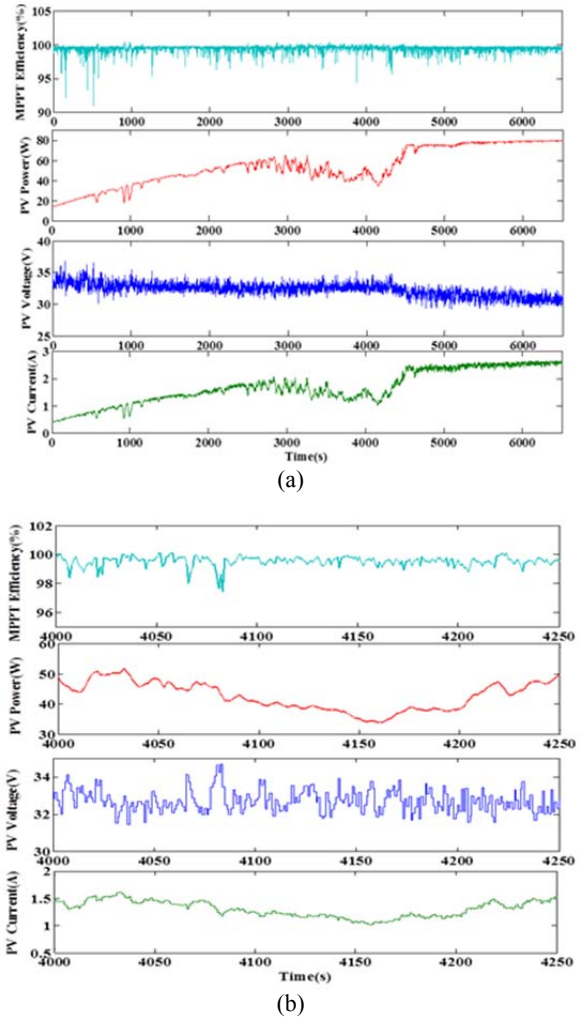


Fig. 22. Temperature and irradiance parameters in the cloudy day profile.



(a)

(b)

Fig. 23. Experimental results of the MPPT controller during the cloudy day profile test. (a) Entire 2-hour period from (a) to (b) in Fig. 22. (b) Zoom-in waveforms in Fig. 23(a).

VI. CONCLUSION

This paper presents a two-stage micro-inverter system using an active voltage balancing circuit and recently proposed 5-level inverter topologies. The multi-output flyback converter lowers the cost and performs the MPPT control by confirming the voltage balancing operation of the DC-link capacitor voltages for the following multi-level inverter. The modified H-bridge topology uses fewer components compared with conventional topologies, which decreases the size and cost of the PCS. The staircase waveform from the multi-level inverter output helps in decreasing the values of the output filter components and mitigates high-frequency EMI.

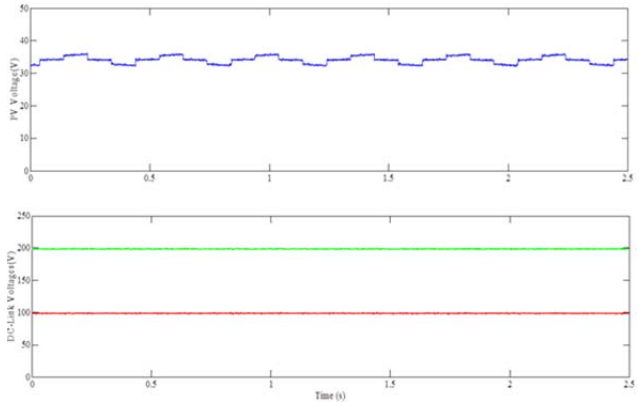


Fig. 24. Experimental results of the PV voltage and DC-Link voltage during the MPPT operation. The voltages V_{DC1} (200 V) and V_{DC2} (100 V) are well balanced during every step operation change in the PV voltage.

The analysis and controller design for the proposed PCS scheme has been presented. The proposed scheme and derived controllers were verified using a 120 W hardware prototype. The MPPT operation for the grid-connected systems was verified by testing the prototype under a cloudy-day profile using a TerraSAS PV simulator. The MPPT efficiency remained above 95% in most of the testing times during the varying irradiance conditions. The designed controllers for standalone mode were also tested for the 120 W output. The DC-link capacitor voltages for the inverter stage were well balanced, and the AC output voltage waveform with 4.43% THD was achieved.

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REFERENCES

[1] A. Ahmed, L. Ran, S. Moon, and J.-H. Park, "A fast PV power tracking algorithm with reduced power mode," *IEEE Trans. Energy Convers.*, Vol. 28, No. 3, pp. 565-575, Sep. 2013.

[2] A. Ahmed, Li Ran, and J. Bumby, "New constant electrical power soft-stalling control for small-scale VAWT's, " *IEEE*

Trans. Energy Convers., Vol. 25, No.4, pp. 1152-1161, Apr.2010.
[3] Economist. (2012). Sunny Uplands: Alternative energy will no longer be alternative (June 2nd, 2012 ed). Available: http://www.economist.com/blogs/graphicdetail/2012/12/daily-chart-19
[4] D. M. Scholten, N. ertugrul, and W. L. Soong, "Micro-inverters in small scale PV systems: A review and future directions," *Australian Universities Power Engineering Conference, AUPEC 2013*, 2013.
[5] D. Sera, L. Mathe, T. Kerekes, and R. Teodorescu, "On the perturb-and-observe and incremental conductance MPPT methods for PV systems, "*IEEE Journal of Photovolt.*, Vol. 3, No. 3, pp. 1070- 1078, Jul.2013.
[6] B. Subudhi and R. Pradhan, "A comparative study on maximum power point tracking techniques for photovoltaic power systems," *IEEE Trans. Sustain. Energy*, Vol. 4, No. 1, pp. 89- 98, Jan.2013.
[7] J. von Appen, T. Stetz, M. Braun, and A. Schmiegel, "Local voltage control strategies for PV storage systems in distribution grids," *IEEE Trans. Smart Grid*, Vol. 5, No. 2, pp. 1002-1009, Mar. 2014.
[8] M. Z. S. El-Dein, M. Kazerani, and M. M. A. Salama, "Optimal photovoltaic array reconfiguration to reduce partial shading losses," *IEEE Trans. Sustain. Energy*, Vol. 4, No. 1, pp. 145-153, Jan. 2013.
[9] T. Wang, H. Kamanth, and S. Willard, "Control and optimization of grid-tied photovoltaic storage systems using model predictive control," *IEEE Trans. Smart Grid*, Vol. 5, No. 2, pp. 1010-1017, Mar. 2014.
[10] M. S. Agamy, S. Chi, A. Elasser, and Yan Jiang, "A high-power-density DC-DC converter for distributed PV architectures," *IEEE Trans. Sustain. Energy*, Vol. 3, No. 2, pp. 791-798, Apr. 2013.
[11] L. Quan and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, Vol. 23, No. 3, pp. 1320-1333, May 2008.
[12] M. E.-S. Ahmed, M. Orabi, and O. M. AbdelRahim, "Two-stage micro-grid inverter with high-voltage gain for photovoltaic applications," *IET Power Electron.*, Vol. 6, No. 9, pp-1812-1821, Nov. 2013.
[13] H. Hu, S. Harb, N. Kutkut, and I. Bataresh, "Power decoupling techniques for micro-inverters in PV systems- a review" *Energy Conversion Congress and Exposition (ECCE)*, pp- 3235-3240, 2010.
[14] A. C. Kyritsis, E. C. Tatakis, and N. P. Papanikolaou, "Optimum design of the current-source flyback inverter for decentralized grid-connected photovoltaic systems," *IEEE Trans. Energy Convers.*, Vol. 23, No. 1, pp. 281-293, Mar. 2008.
[15] Y. Li and R. Oruganti, "A low cost flyback CCM inverter for AC module application," *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1295-1303, Mar. 2012.
[16] Y. Xue, L. Chang, and S. B. Kjaer, "Topologies of single-phase inverters for small distributed power generators: An overview," *IEEE Trans. Power Electron.*, Vol. 19, No. 5, pp. 1305-1314, Sep. 2004.
[17] Md. D. Islam, C. M. F. S. Reza, and S, Mekhilef, "Modeling and experimental validation of 5-level hybrid H-bridge multilevel inverter fed DTC-IM drive," *Journal of Electrical Engineering & Technology*, Vol. 10, No. 2, pp. 574-585, Mar. 2015.
[18] S. A. Alexander and M. Thathan, "Optimal harmonic stepped waveform technique for solar fed cascaded multilevel inverter," *Journal of Electrical Engineering & Technology*, Vol. 10, No. 1, pp. 261-270, Jan. 2015.
[19] P. Alemi and D.-C. Lee, "A generalized loss analysis algorithm of power semiconductor devices in multilevel NPC inverters," *Journal of Electrical Engineering & Technology*, Vol. 9, No. 6, pp. 2168-2180, Nov. 2014.
[20] M. R. Banaei, B. Nayeri, and E. Salary, "Single input multi output DC/DC converter : An approach to voltage balancing in multilevel inverter," *Journal of Electrical Engineering & Technology*, Vol. 9, No. 5, pp. 1537-1543, Sep. 2014.
[21] I. D. Pharne and Y. N. Bhosale, "A review on multilevel inverter topology," *Conference on Power, Energy and Control (ICPEC)*, pp. 700-703, 2013.
[22] J. Choi, K. Kim, and F. Kang, "Five-level PWM inverter using a single DC input source," *Power Electronics Annual Conference on Korean Institute of Power Electronics*, pp. 433-434, 2013.
[23] M. F. N. Tajuddin, N. H. Ghazali, and T. C. Siong, "Modelling and simulation of modified unipolar PWM scheme on a single phase DC-AC converter using PSIM," *Proceedings of Student Conference on Research and Development (SCOReD)*, pp. 328-331, 2009.

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