JPE 15-6-10

http://dx.doi.org/10.6113/JPE.2015.15.6.1508
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Cascaded Multi-Level Inverter Based IPT Systems for High Power Applications

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Abstract

A single phase H-bridge inverter is employed in conventional Inductive Power Transfer (IPT) systems as the primary side power supply. These systems may not be suitable for some high power applications, due to the constraints of the power electronic devices and the cost. A high-frequency cascaded multi-level inverter employed in IPT systems, which is suitable for high power applications, is presented in this paper. The Phase Shift Pulse Width Modulation (PS-PWM) method is proposed to realize power regulation and selective harmonic elimination. Explicit solutions against phase shift angle and pulse width are given according to the constraints of the selective harmonic elimination equation and the required voltage to avoid solving non-linear transcendental equations. The validity of the proposed control approach is verified by the experimental results obtained with a 2kW prototype system. This approach is expected to be useful for high power IPT applications, and the output power of each H-bridge unit is identical by the proposed approach.

Key words: Cascaded multi-level inverter, Harmonic elimination, Inductive Power Transfer (IPT), Power regulation

NOMENCLATURE

Q_1 - Q_8 : power MOSFETs.
D_1 - D_8 : MOSFET antiparallel diodes.
L_p : equivalent primary coil inductance.
L_s : equivalent secondary coil inductance.
C_p : resonant compensation capacitance for the primary circuit.
C_s : resonant compensation capacitance for the secondary circuit.
M : mutual inductance between the primary and secondary coils.
R_L : equivalent load resistance.
E : DC source voltage.
u_{H1} : output voltage of the first H-bridge unit.
u_{H2} : output voltage of the second H-bridge unit.
u_0 : synthesized voltage of the cascaded multilevel inverter.
i_p : AC current in the primary transmitting coil.
T_s : period of the fundamental period.
Z_s : reflection impedance of the secondary circuit.
$(\mathbf{A})^*$: conjugate operation of **A**.
Re(**A**) : real component operation of **A**.

Manuscript received Jan. 20, 2015; accepted Jun. 12, 2015
Recommended for publication by Associate Editor Younghoon Cho.
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I. INTRODUCTION

Inductive Power Transfer (IPT) technology can deliver power from a power source to a load with no physical contact [1] in order to enhance systems' flexibility. This technology adopts high-frequency electromagnetic coupling [2], [3], resonant inverters [4], power regulation [5] and control theory [6]. With IPT technology, devices can be applied in contaminated environments to avoid the influences of ice, dirt, moisture and other chemicals. In addition, IPT systems have been used in numerous applications including the wireless charging of biomedical implants [7], mining applications [8], under-water power supply [9] and electric vehicles [10]-[13].

For IPT systems, the resonant inverter is one of the most important components, which operates at relatively high

frequency (5-100 kHz) compared to 50/60Hz. It generates and maintains a high-frequency resonant current in the primary coil, creating a strong magnetic field, which inductively generates an AC voltage of the same frequency in the secondary pick-up. Both the secondary and primary circuits are tuned at the resonant inverter's operating frequency using compensation capacitors. However, the output power capacity of the single phase H-bridge resonant inverter [14] employed in conventional IPT systems is limited by the constraints of the power electronic devices and the cost. Therefore, it may not be able to meet some high-power application requirements, such as electric vehicles and rail transit systems.

Multi-level technology has advantages in terms of reducing the voltage stress of switching devices, limiting the changing rate of voltage (du/dt), degrading the harmonic density of output voltage, and increasing the output power capacity. Cascaded H-bridge multi-level inverters are much easier to implement modularization and they have the merits of increased flexibility and fewer electronic devices needed than diode-clamped and flying-capacitor multi-level inverters. Compared to a single H-bridge inverter, cascaded multi-level inverters have the following advantages: 1) the cascaded structure uses low-voltage and low-cost power semiconductor devices to enhance a high power output; 2) the cascaded inverters can be built with modularized components which helps to reduce the manufacture cost; 3) the limitation of a single H-bridge inverter power supply can be removed in aspects like heat dissipation, short time overload; and 4) the Total Harmonic Distortion (THD) of the output voltage of the inverter is lower than that of conventional single H-bridge inverter. Therefore, a cascaded H-bridge multi-level inverter is adopted in this paper as the high-frequency source for IPT systems.

The output power of a cascaded inverter can be directly regulated by altering the switching angle with no need for additional DC-DC devices. Furthermore, Selective Harmonic Elimination (SHE) methods can be applied in cascaded inverters to eliminate selective harmonic components of the output voltage. However, SHE equations are nonlinear, transcendental equations, so that no solution can be accomplished [15]. Homotopy and continuation theory based SHE methods are proposed to solve transcendental equations [16]-[18]. However, these approaches need preliminary off-line computation of the switching angles, and real time applications fetch the switching angles from pre-calculated lookup tables stored in the microcontroller's internal memory.

Multi-level technology has been adopted in IPT systems in [19], [20]. A high frequency multi-level IPT system suitable for high power application was described in [19]. However, harmonic distortion, power losses, power factor and efficiency were analyzed in detail without consideration of the power regulation or/and selective harmonic elimination. Recently, a MOSFET-IGBT multi-level converter, which can reduce the overall costs and the number of harmonic components [20], was proposed for IPT based high frequency fast chargers. This converter needs to solve transcendental equations instead of providing explicit solutions for the SHE equation. A novel modulation strategy and a phase shift modulation algorithm for the multi-level inverters supplying IPT systems were proposed to minimize the switching loss and coil loss [21]. However, they ignored the power regulation.

In order to enhance the output power capacity of IPT systems, this paper employs a cascaded multi-level inverter instead of the conventional single H-bridge for supplying IPT systems. The Phase Shift Pulse Width Modulation (PS-PWM) method employed in cascaded multi-level inverters is proposed to realize both power regulation and selective harmonic elimination. Explicit solutions against phase shift angle and pulse width are given according to the constraints of the selective harmonic elimination equation and the required voltage avoiding solving nonlinear transcendental equations. Thus, the proposed method is suitable for real-time applications. The active output power of each H-bridge unit is analyzed. They are identical with the proposed approach.

This paper is organized as follows. In Section II, a detailed description of the structure design and the principle analysis of an IPT system based on a cascaded multilevel inverter are given. Section III describes the self-balancing output power of each H-bridge. The selective harmonic elimination and power regulation method for cascaded multi-level inverters supplying IPT systems is analyzed in detail in Section IV. Then, Section V shows the steady-state results of simulation and experimental systems operating at 2kW. The conclusion is finally drawn in Section VI.

II. Structure Design and Principle Analysis of an IPT System Based on a Cascaded Inverter

A. Structure Design and Principle Analysis of an IPT System Based on Cascaded Inverters

It is well-known that the larger the number of cascaded multilevel H-bridge inverters employed, the better the power quality of the IPT output voltage becomes. To enhance the quality of the voltage waveform and the output power in a cost-effective way, this paper aims to investigate a five-level inverter with two cascaded H-bridges instead of more H-bridges. This will be used as an example to demonstrate the findings of this study while considering the cost of the whole system. The structure of an IPT system based on a cascaded multilevel inverter with an S-S (series-series) tuned circuit is shown in Fig. 1. Each H-bridge inverter is connected with an isolated DC voltage source whose voltage may differ from one another. However, they are set to be the same as E in this paper. The DC voltage sources can be batteries or rectified voltages according to the required voltage and power.

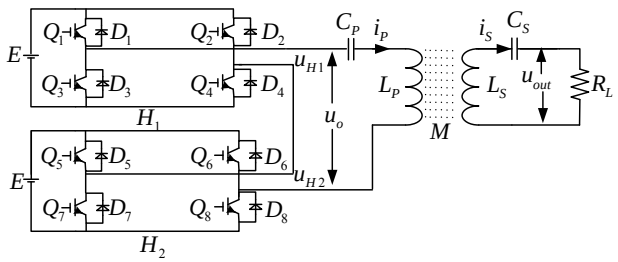


Fig. 1. The schematic of IPT system based on a cascaded multi-level inverter.

Suppose that the series resonant tank on the primary and secondary pick-up sides are both tuned to the operating angular frequency ω of the H-bridges, then:

$$\omega^2 = \frac{1}{L_P C_P} = \frac{1}{L_S C_S} \tag{1}$$

In this situation, the reflection impedance Z_s of the secondary circuit becomes purely resistive.

$$Z_S = \frac{\omega^2 M^2}{R_L} \tag{2}$$

B. Staircase Waveform Synthesis with PS-PWM

The output of the cascaded multi-level inverter is synthesized by superimposing two identical staircases with different phase shift angles. The synthesized voltage (u_0) can be continuously regulated by Phase Shift Pulse Width Modulation (PS-PWM) of the two H-bridge units' voltages (u_{H1} and u_{H2}) in order to meet various power requirements.

To simplify the analysis, a coordinate is established as shown in Fig.2. Line x is the symmetrical center line of the positive pulse width of the synthesized voltage. The origin is the joint of line x and the horizontal axis (ωt), while the fundamental angular frequency is (ω), and the fundamental period is (T_s). Consequently, the pulse width of u_{H1} can be expressed by $2\theta_L$, measured in radians. The angular difference between the center of u_0 and the center of u_{H1} is θ_Δ . The phase shift angle is denoted by $2\theta_\Delta$.

The synthesized voltage u_0 of the cascaded inverter is the superposition of u_{H1} and u_{H2} . Therefore, the synthesized voltage can be described mathematically as:

$$u_o(t) = u_{H1}(t) + u_{H2}(t) \tag{3}$$

The output voltage of each H-bridge $u_{Hi}(t)(i = 1, 2)$ is defined by:

$$u_{Hi}(t) = \begin{cases} E, & \omega t \in [-\theta_L + (-1)^i \theta_\Delta, \theta_L + (-1)^i \theta_\Delta] \\ -E, & \omega t \in [\pi - \theta_L + (-1)^i \theta_\Delta, \pi + \theta_L + (-1)^i \theta_\Delta] \\ 0, & otherwise. \end{cases} \tag{4}$$

When synthesizing two identical staircases with different phase shift angles, there will be two possible situations: (a) $\theta_\Delta + \theta_L \le \pi/2$ and (b) $\pi/2 \le \theta_\Delta + \theta_L$.

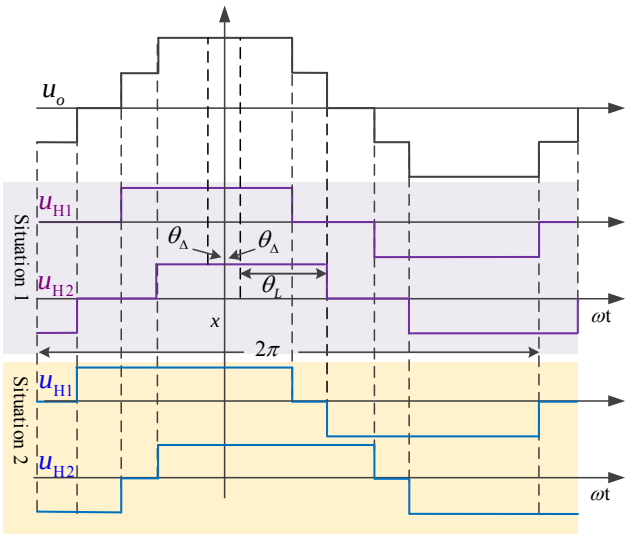


Fig. 2. Schematic of staircase synthesis method.

In the first situation ($\theta_\Delta + \theta_L \le \pi/2$), one switching cycle operation of the cascaded inverter is divided into eight submodes as follows. The driving signals of the MOSFETs are shown in Fig. 3. The switch-mode transitions and the resonant current pathways in the proposed cascaded inverter are illustrated in Fig. 4.

[**Mode 1**]: Q_2 , Q_6 , and Q_7 switch on, and D_1 is naturally forward biased. The synthesized voltage of the inverter turns to be $-E$.

[**Mode 2**]: Before the current commutation (mode 2(a)), Q_2 and Q_6 switch on, and D_1 and D_5 are naturally forward biased. After the current commutation (mode 2(b)), Q_1 and Q_5 switch on, and D_2 and D_6 are naturally forward biased. The synthesized voltage turns to be zero.

[**Mode 3**]: Q_1 , Q_4 , and Q_5 switch on, and D_6 is naturally forward biased. The synthesized voltage becomes E .

[**Mode 4**]: Q_1 , Q_4 , Q_5 , and Q_8 switch on, and the synthesized voltage turns to be $2E$.

[**Mode 5**]: Q_4 , Q_5 , and Q_8 switch on, and D_3 is naturally forward biased. The synthesized voltage becomes E .

[**Mode 6**]: Before the current commutation (mode 6(a)), Q_4 and Q_8 switch on, and D_3 and D_7 are naturally forward biased. After the current commutation (mode 6(b)), Q_3 and Q_7 switch on, and D_4 and D_8 are naturally forward biased. The synthesized voltage becomes zero.

[**Mode 7**]: Q_2 , Q_3 , and Q_7 switch on, and D_8 is naturally forward biased. The synthesized voltage becomes $-E$;

[**Mode 8**]: Q_2 , Q_3 , Q_6 , and Q_7 switch on. The synthesized voltage becomes $-2E$.

C. Staircase Waveform Synthesis with PS-PWM

In the second situation ($\pi/2 \le \theta_\Delta + \theta_L$), the zero voltage is produced by synthesizing the two voltages of the two

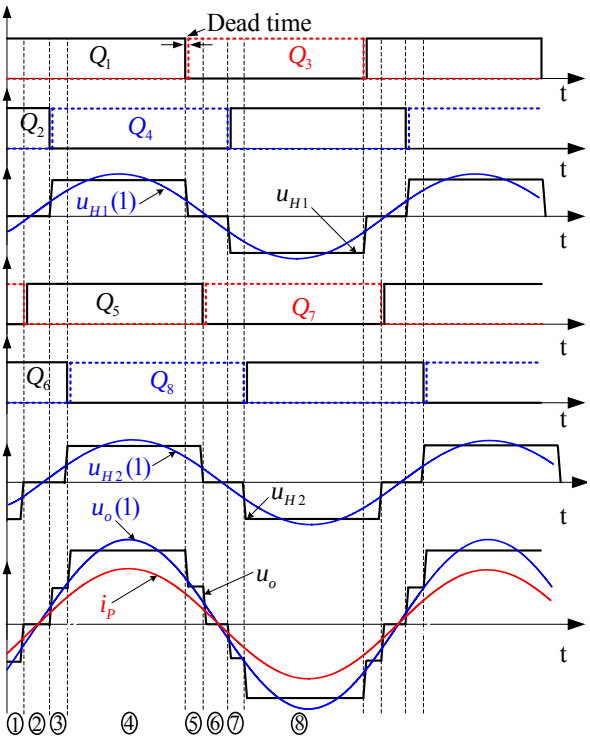


Fig. 3. Relevant voltage and current operating waveforms.

opposite voltage levels produced by two H-bridge units (H_1 and H_2) as shown in the blue line of Fig. 2. In this case, one H-bridge unit will charge the other H-bridge unit, and the reverse situation will occur in the second half period. This phenomenon influences the stability of the synthesized voltage and will probably damage the DC sources of each H-bridge unit.

One switching cycle operation of the second situation can also be divided into eight submodes, in which Modes 1, 3, 5, 7, and 8 are exactly the same as those of the first situation. However, there are two different modes between the first and the second situation. A detailed analysis is given below:

[**Mode 2**]: Before the current commutation (Fig. 5(a)), the DC source of H_2 charges the DC source of H_1 through D_1, D_4, Q_6, and Q_7. After the current commutation (Fig. 5(b)), the DC source of H_1 charges the DC source of H_2 through Q_1, Q_4, D_5, and D_7. The voltages of the two H-bridges cancel each other out and the synthesized voltage becomes zero.

[**Mode 6**]: Before the current commutation (Fig. 5(c)), the DC source of H_1 charges the DC source of H_2 through D_2, D_3, Q_5, and Q_8. After the current commutation (Fig. 5(d)), the DC source of H_2 charges the DC source of H_1 through Q_2, Q_3, D_5, and D_8. The voltages of the two H-bridge cancel each other out and the synthesized voltage becomes zero.

To avoid the aforementioned drawbacks, θ_L and θ_Δ should satisfy the following constraint:

$$\theta_\Delta+\theta_L \le \frac{\pi}{2} \tag{5}$$

III. Analysis of the Self-Balancing Output Power

After applying a Fourier Transformation to $u_{Hi}(t)$, the phasor of the k[th] order harmonic is in the form of:

$$\dot{U}_{Hi}(k)=\frac{\sqrt{2}}{T_S}\left(\int_{\frac{-\theta_L+(-1)^i\theta_\Delta}{2\pi}\cdot T_S}^{\frac{\theta_L+(-1)^i\theta_\Delta}{2\pi}\cdot T_S} E\cdot e^{\frac{-j2\pi kx}{T_S}}dx+\int_{\frac{-\theta_L+(-1)^i\theta_\Delta}{2\pi}\cdot T_S+\frac{T_S}{2}}^{\frac{\theta_L+(-1)^i\theta_\Delta}{2\pi}\cdot T_S+\frac{T_S}{2}} -E\cdot e^{\frac{-j2\pi kx}{T_S}}dx\right)$$
$$=\begin{cases}\dfrac{2\sqrt{2}E\sin(k\theta_L)\cdot e^{-jk(-1)^i\theta_\Delta}}{k\pi} & (k \text{ is an } odd \text{ } number)\\ 0 & (k \text{ is an } even \text{ } number)\end{cases} \tag{6}$$

According to (3) and (6), the phasor of the k[th] order harmonic is provided by:

$$\dot{U}_o(k)=\dot{U}_{H1}(k)+\dot{U}_{H2}(k)$$
$$=\frac{4\sqrt{2}E\cdot\cos(k\theta_\Delta)\cdot\sin(k\theta_L)}{k\pi} \tag{7}$$

The current of the primary coil can be derived by:

$$i_P=\frac{u_0}{Z_S}=\frac{u_0R_L}{\omega^2M^2} \tag{8}$$

i_P will be in phase with the fundamental synthesized voltage ($u_0(1)$) when the circuit is tuned at the resonant frequency. The active power of the fundamental output of H-bridge unit H_1 can be obtained by:

$$P_{H1}=\mathrm{Re}\left[\dot{U}_{H1}(1)\cdot\left(\dot{I}_P\right)^*\right]$$
$$=\frac{2\sqrt{2}E\cdot\sin\theta_L\cos\theta_\Delta}{\pi}\cdot I_P \tag{9}$$

where $\dot{I}_P$ and I_P denote the phasor and Root Mean Square (RMS) of the converter output current.

Similarly, the active power of the fundamental output of H_2 can be expressed in terms of θ_L and θ_Δ as:

$$P_{H2}=\frac{2\sqrt{2}E\cdot\sin\theta_L\cos(-\theta_\Delta)}{\pi}\cdot I_P \tag{10}$$

Comparing (9) and (10), it is obvious that $P_{H1}=P_{H2}$, which means that the active output power of each H-bridge unit is identical. That is to say, the output power of each H-bridge is self-balanced.

IV. Harmonic Elimination and Power Regulation Method (HEPRM)

A. Selective Harmonic Elimination

When the k[th] order harmonic of $u_o(t)$ is selected to be eliminated, the harmonic elimination equation is provided according to (7) by:

$$\frac{4\sqrt{2}E\cdot\cos(k\theta_\Delta)\cdot\sin(k\theta_L)}{k\pi}=0 \tag{11}$$

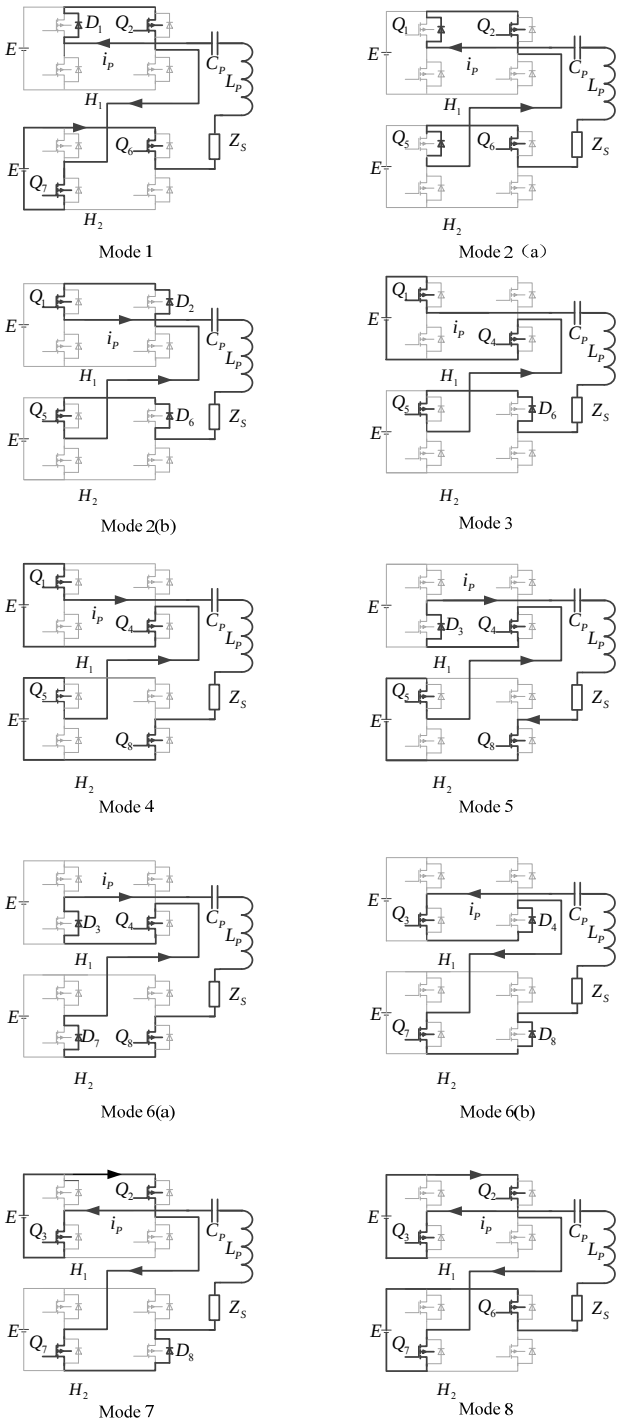


Fig. 4. Mode transitions during one switching cycle.

The solutions of (11) are given by:

$$\theta_\Delta = (0.5+n)\pi/k \quad n \in \mathrm{N} \tag{12}$$

$$\theta_L = n\pi/k \quad n \in \mathrm{N} \tag{13}$$

Considering the odd multiples of the k[th] order harmonic and according to (12) and(13), the following are obtained:

$$\cos[(2K+1)k\theta_\Delta] = 0 \quad K \in \mathrm{N} \tag{14}$$

$$\sin[(2K+1)k\theta_L] = 0 \quad K \in \mathrm{N} \tag{15}$$

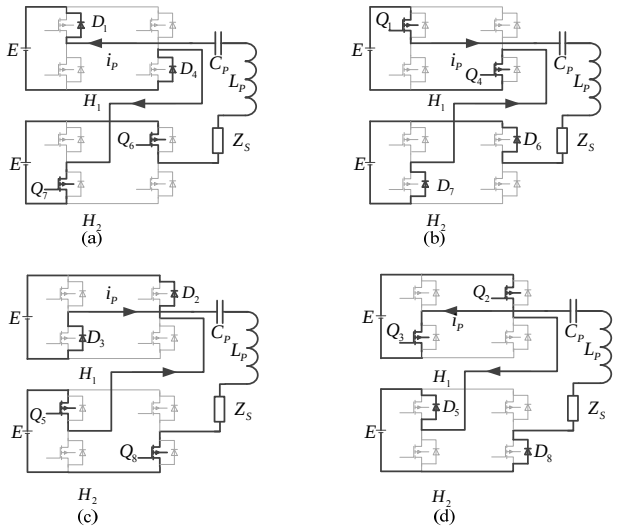


Fig. 5. Operating modes of the switching devices.

The two equations above satisfy (11), which eliminates the k[th] order harmonic and the odd multiples of the k[th] order harmonic. Taking the 3[rd] order harmonic elimination as an example, the corresponding 9[th], 15[th], etc. order harmonics can be eliminated.

As the lower harmonic components have more influence than the higher harmonic components in some applications, the 3[rd] harmonic component is selected to be eliminated in this paper. Consequently, the following is obtained:

$$\dot{U}_o(3) = \frac{4\sqrt{2}E \cdot \cos 3\theta_\Delta \cdot \sin 3\theta_L}{3\pi} = 0 \tag{16}$$

By solving (16) with the constraint of (5), the formula yields $\theta_\Delta = \pi/6$ or $\theta_L = \pi/3$. When $\theta_\Delta = \pi/6$ or $\theta_L = \pi/3$, the 3[rd] order harmonic and the odd triplen harmonics are eliminated.

B. Power Regulation with the HEPRM

The IPT output power can be described as a function of $U_o(1)$ as follows:

$$P_{out} = \frac{U_o(1)^2 R_L}{\omega^2 M^2} \tag{17}$$

Therefore, the output power can be regulated by changing the fundamental RMS $U_o(1)$ of the synthesized voltage. Thus, $U_o(1)$ can be derived from (7):

$$U_o(1) = \frac{4\sqrt{2}E \cdot \cos\theta_\Delta \cdot \sin\theta_L}{\pi} \tag{18}$$

Substitute $\theta_\Delta = \pi/6$ into (18). Then $U_o(1)$ can be expressed by:

$$U_o(1) = \frac{2\sqrt{6}E \cdot \sin\theta_L}{\pi} \tag{19}$$

With the restriction of (5):

$$0 \le \theta_L \le \frac{\pi}{3} \tag{20}$$

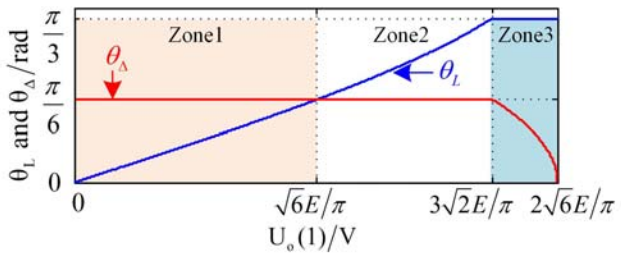


Fig. 6. θ_L and θ_Δ against the RMS of the fundamental voltage.

TABLE I

THE CONFIGURATION OF THE IPT SYSTEM

Parameters	Value
DC voltage of the H-bridge unit *E/V*	50
Inverter frequency *f/kHz*	20
Inductance of the primary coil L_P / μH	83.34
Resonant compensation capacitance of primary circuit C_P / μF	0.751
Mutual inductance of the primary and secondary coils M / μH	26.07
Inductance of the secondary coil L_S / μH	36.2
Resonant compensation capacitance of secondary circuit C_S / μF	1.749
Equivalent resistance of the load R_L / Ω	3.7

In this case, $0 \le U_o(1) \le 3\sqrt{2}E/\pi$.

Similarly, when $\theta_L = \pi/3$, $U_o(1)$ can be expressed by:

$$U_o(1) = \frac{2\sqrt{6}E \cdot \cos\theta_\Delta}{\pi} \tag{21}$$

With the restriction of (5), there is:

$$0 \le \theta_\Delta \le \frac{\pi}{6} \tag{22}$$

Thus, $U_o(1)$ ranges over $3\sqrt{2}E/\pi \le U_o(1) \le 2\sqrt{6}E/\pi$.

In a word, the fundamental RMS of the synthesized voltage can be regulated continuously from 0 to $2\sqrt{6}E/\pi$ with the elimination of the 3rd harmonic as shown in Fig. 6. It is worth noting that this synthesized voltage will degrade to a three-level staircase when the required synthesized voltage drops below $\sqrt{6}E/\pi$ ($\theta_\Delta = \pi/6, \theta_L \le \pi/6$). Consequently, the synthesized voltage can be divided into 3 zones according to aforementioned discussion.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

The performance of the proposed control method is firstly verified via MATLAB/SIMULINK and then realized and tested in an experimental setting. To be consistent, all of the parameters in both the simulation and the experiment are the same as those given in Table I.

A. Simulation Results

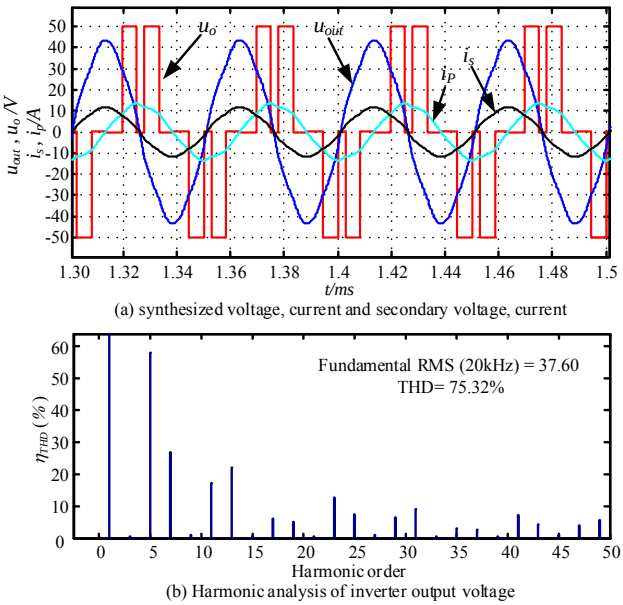


Fig. 7. The simulation waveform of voltage and current of primary side and secondary side, synthesized voltage harmonic analysis when $\theta_\Delta = \pi/6$, $\theta_L = \pi/9$.

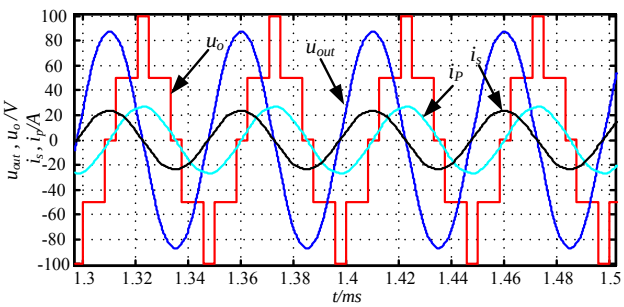


Fig. 8. The simulation waveform of voltage and current of the cascaded inverter when $\theta_\Delta = \pi/6, \theta_L = \pi/4$.

To verify the validity of the proposed control method, a simulation model of the cascaded two-H-bridge inverter was constructed in Matlab/Simulink. Detailed configuration information is given in TABLE I.

Zone 1 ($\theta_\Delta = \pi/6, 0 \le \theta_L \le \pi/6$): the inverter outputs a synthesized voltage over $0 \le U_o(1) \le \sqrt{6}E/\pi$, and appears as a three-level voltage waveform as shown in Fig. 7(a). The 3rd order harmonic and the odd triplen harmonics have been completely eliminated, and its fundamental RMS complies with (14) (the experimental values are slightly smaller than the theoretical ones, because there are internal resistances in the power switches). The Total Harmonic Distortion (THD) is rather high (up to 75.32%) under such an operating condition.

Zone 2 ($\theta_\Delta = \pi/6, \pi/6 \le \theta_L \le \pi/3$): the amplitude of the synthesized voltage ranges over $\sqrt{6}E/\pi \le U_o(1) \le 3\sqrt{2}E/\pi$, and is a five-level staircase waveform. In such an operating condition, the THD is relatively low (up to 33.12%) as shown in Fig. 10.

Zone 3 ($0 \le \theta_\Delta \le \pi/6, \theta_L = \pi/3$): the synthesized voltage is

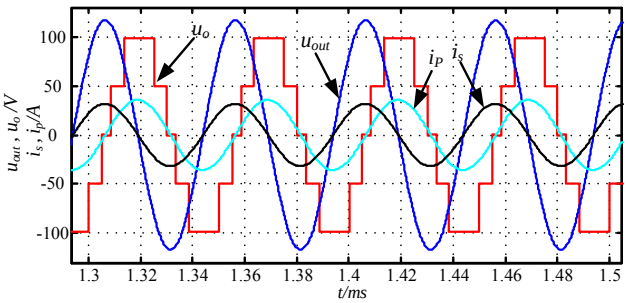


Fig. 9. The simulation waveform of voltage and current of the cascaded inverter when $\theta_\Delta = \pi/10$, $\theta_L = \pi/3$.

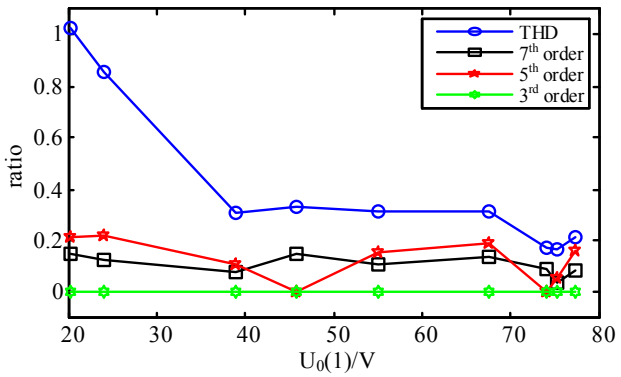


Fig. 10. Harmonic density against the synthesized voltage. Input voltage is 50V dc.

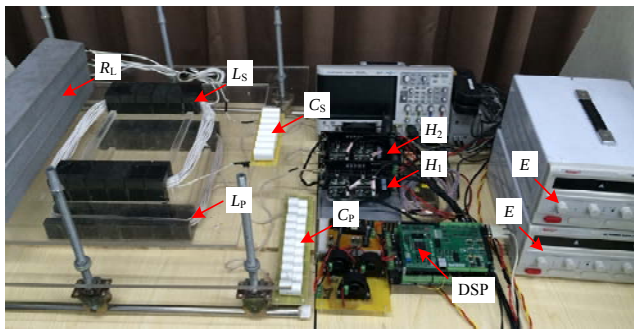
a five-level staircase ranging in the segment of $3\sqrt{2}E/\pi \le U_o(1) \le 2\sqrt{6}E/\pi$. In such a case, the THD is rather low (up to 16.73%) as shown in Fig. 10.

The THD of the 3rd, 5th and 7th harmonics against $U_o(1)$ are shown in Fig. 10. The THD is low if $U_o(1)$ is relatively high. However, the THD becomes relatively high if $U_o(1)$ decreases to a relatively low level. In addition, the 3rd order harmonic remains at a low level when the synthesized voltage varies.

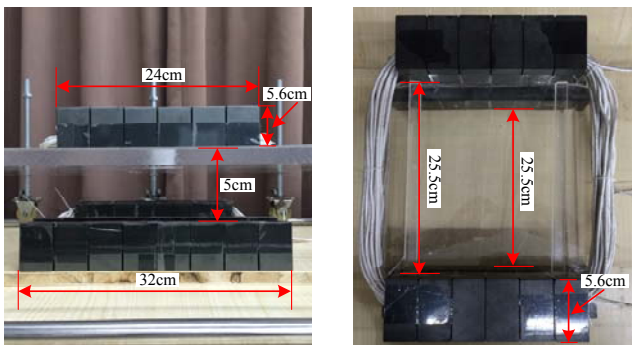
B. Experimental Results

Applying the system configuration in Table I, an IPT system is established based on a cascaded multilevel inverter with a TMS320F28335 as the controller and an IRF3710 as the power switch. The primary and secondary coils are wound with Litz wire and the distance between the two coils is set to be 50mm. The experimentation setup is shown in Fig. 11. Because of the limited capacity of the MOSFET, the maximum output power of the IPT system is around 2kW. Correspondingly, the rated power of each H-bridge unit is approximately 1kW.

In Fig. 12, the inverter output degrades to a three-level staircase. The 3rd order harmonic and its odd triplen harmonics have been completely eliminated. However, the 5th and 7th order harmonic distortions remain high (up to 25% and 15%, respectively), and $U_o(1)$ is rather low (24V). The inverter output power is approximately 180W (each of the



(a)



(b) (c)

Fig. 11. The experimentation setup of a 2 kW IPT system. (a)Experimental setup. (b)Lateral view of the coils. (c)Top view of the coils.

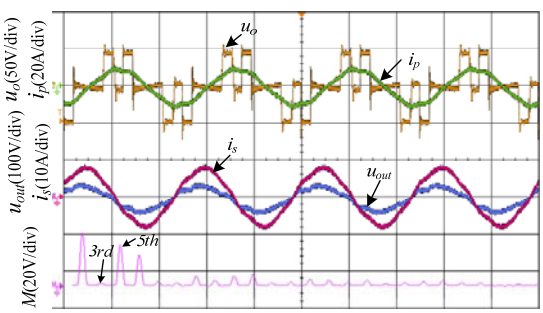


Fig. 12. The waveform of voltage and current of primary and secondary sides, synthesized voltage harmonic analysis when $\theta_\Delta = \pi/6$, $\theta_L = \pi/10$.

H-bridge units, H_1 and H_2, has an output power of 90W). The load of the secondary circuit consumes about 120W and the IPT system has an efficiency of around 75%. In Fig. 13 and Fig. 14, the synthesized voltages appear to be five-level staircases, and the 3rd order harmonic and their odd triplen harmonics are also eliminated with a low THD (35% and 16.91%, respectively). In the two cases, the values of $U_o(1)$ are set to be 43V and 70V, respectively. Correspondingly, the inverter output powers are 600W (the output power of both H-bridge units, H_1 and H_2, are approximately 300W) and 1600W (800W for each H-bridge unit). The power consumption of the secondary loads are 480W and 1400W, which yield efficiencies of 80% and 87.5%, respectively.

In this experiment, various values of θ_Δ and θ_L are

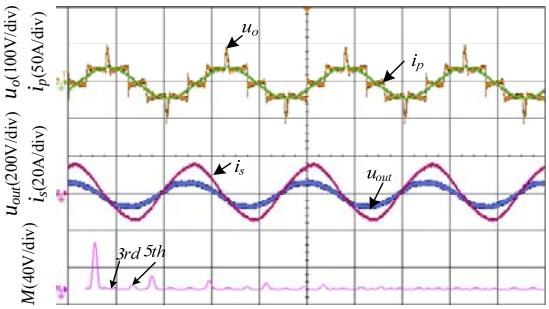


Fig. 13. The waveform of voltage and current of primary and secondary sides, synthesized voltage harmonic analysis when $\theta_\Delta = \pi/6, \theta_L = \pi/5$.

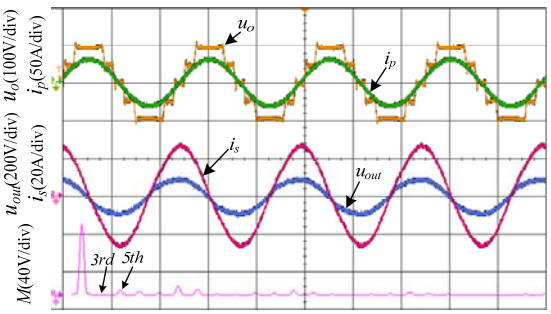


Fig. 14. The waveform of voltage and current of primary side and secondary side, output voltage harmonic analysis when $\theta_\Delta = \pi/12$, $\theta_L = \pi/3$.

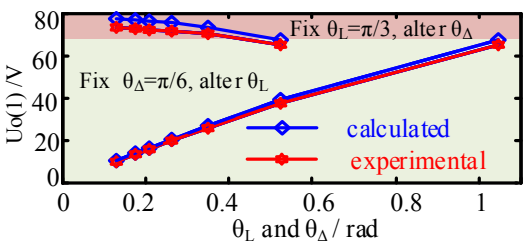


Fig. 15. The curve of experimentation and theoretical value of the fundamental voltage's RMS against θ_Δ and θ_L .

adopted to verify the performance of the HEPRM. A comparison of the RMS of the experimental and theoretical synthesized voltages is shown in Fig. 15. The trends of the changes in the experimental and theoretical values are similar. However, the theoretical values are slightly smaller than the experimental ones because of the internal resistance of the power switches and the equivalent circuit resistance. When the synthesized voltage increases (the current also increases), the experimental values differ greater from the theoretical values.

VI. Conclusion

This paper proposed a HEPRM method for IPT systems to enhance the power capacity of these systems, eliminate selective order harmonics, and simultaneously regulate the IPT output power. This is achieved by changing the phase shift angle and pulse width according to the explicit relation of the two quantities. In this analysis, a five-level two-H-bridge inverter is taken as an example to provide the explicit expression of the phase shift angle and pulse width. The proposed method is verified with simulation and experimental results. These results allow some conclusions to be made. When compared with traditional IPT systems based on a single phase H-bridge inverter, the system has the following characteristics:

1) The proposed system enhances the IPT output power when using the switches with the same capacity.

2) The system employs the staircase synthesis method instead of high-frequency modulation. Thus, it is applicable to the high-frequency inverters employed in IPT systems, and each cascaded H-bridge unit has the power self-balancing characteristic.

3) The system can eliminate selective order harmonics of the output voltage. The explicit expression of the phase shift angle and pulse width can be obtained without solving higher transcendental equations. As a result, the computational complexity is reduced and real-time control is facilitated.

4) The system eliminates the 3rd order harmonic and the odd triplen harmonics. It also continuously regulates the output power without an additional DC-DC converter.

5) The system's synthesized voltage appears to be a three-level staircase with a low fundamental RMS and a high THD. Meanwhile, the synthesized voltage appears to be a five-level staircase with a large fundamental RMS and a low THD. This means that the characteristics of the proposed method are suitable for high power applications.

Acknowledgment

This work was supported by Scientific R&D Program of China Railway Corporation (2014J013-B) and National Natural Science Foundation of China (Grant No. 51507147).

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