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Compensation of Current Offset Error in Half-Bridge PWM Inverter for Linear Compressor

Dong-Youn Kim*, Won-Sang Im**, Seon-Hwan Hwang***, and Jang-Mok Kim†

*,†Department of Electrical Engineering, Pusan National University, Busan, Korea
**Department of Electrical Computer Engineering, Lehigh University, Bethlehem, PA, USA
***Department of Electrical Engineering, Kyungnam University, Changwon, Korea

Abstract

This paper proposes a novel compensation algorithm of current offset error for single-phase linear compressor in home appliances. In a half-bridge inverter, current offset error may cause unbalanced DC-link voltage when the DC-link is comprised of two serially connected capacitors. To compensate the current measurement error, the synchronous reference frame transformation is used for detecting the measurement error. When an offset error occurs in the output current of the half-bridge inverter, the d-axis current has a ripple with frequency equal to the fundamental frequency. With the use of a proportional-resonant controller, the ripple component can be removed, and offset error can be compensated. The proposed compensation method can easily be implemented without much computation and additional hardware circuit. The validity of the proposed algorithm is verified through experimental results.

Key words: Current offset error, Half-Bridge inverter, Linear compressor, PR controller, Single phase, Unbalanced voltage

I. INTRODUCTION

In recent years, effort has been exerted to improve the efficiency of home aapliance systems. However, considerable effort is needed to reduce the power consumption of the refrigerators, which covers 20%–40% of the power consumption of home appliances. Of total the power consumed by the refrigerator, 80% is utilized by the compressor. The use of a linear compressor can improve the efficiency and minimize the volume of the refrigerator compared with a conventional crank-driven compressor [1]-[3].

Furthermore, the topology of the power converter is also important to increase the efficiency of the refrigerator. The satisfactory operation of power converter in home appliances requires the following conditions:

- Power factor control must be available for low harmonic distortion.
- The switch loss and conduction loss must be considered.
- Boost control of DC-link is needed to improve the system efficiency.

Among the several power converter topologies, the single-phase back-to-back converter is suitable for controlling the linear compressor [4]-[6]. In particular, the half-bridge converter is the simplest topology, yet it has a large current ripple. The other topology for the linear compressor is the full-bridge converter, which reduces current ripple and the size of inductor used for filtering. Despite those advantages, the linear compressor needs eight switching devices for rectification and inverting operations, which consequently, results in much switching loss.

This paper proposes a system with a full-bridge converter and a half-bridge inverter to drive the linear compressor, as shown in Fig. 1. The full-bridge converter at the rectifier side of this topology gives an advantage of reducing the current ripple and the voltage rating of switching element. In addition, the half-bridge inverter reduces the number of switching elements, switching loss, cost, and volume of the system.

However, current ripple on the inverter side may be an issue in case of the half-bridge inverter. Nevertheless, because of the large inductance of the linear compressor, the ripple of the inverter current is negligible in this topology. The remarkable feature of the proposed power converter is the DC-link, and this DC-link consists of two serially

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Recommended for publication by Associate Editor Bon-gwan Gu.
†Corresponding Author: jmok@pusan.ac.kr
Tel: +82-51-510-2366, Fax: +82-51-513-0212, Pusan Nat'l University
*Dept. of Electrical Eng., Pusan National University, Korea
**Dept. of Electrical Computer Eng., Lehigh University, USA
***Dept. of Electrical Engineering, Kyungnam University, Korea

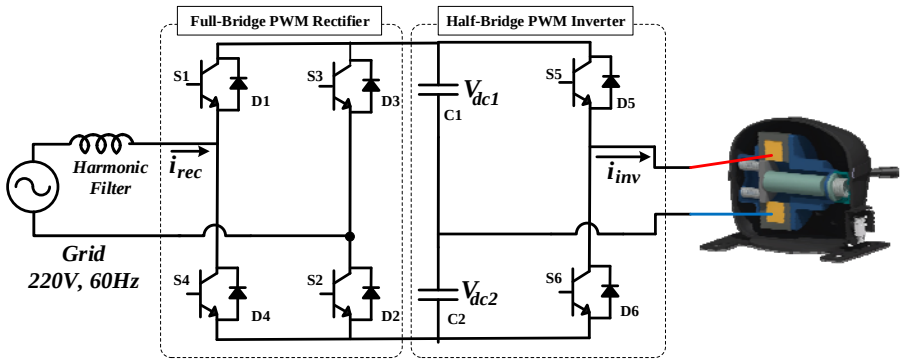

Fig. 1. Proposed single-phase Pulse Width Modulation(PWM) converter for linear compressor.

connected capacitors. In an ideal inverter operation of this topology, the two capacitors are charging and discharging complementarily according to the current direction, and the average energy of charging and discharging is always equal. However, if offset error exists in the current sensor, the upper and lower capacitors cause DC-link imbalance. Thus, the compensation algorithm is needed for safe operation.

This paper analyzes the components of the offset error on the basis of the synchronous reference frame and analyzes the voltage imbalance on DC-link caused by the offset error of the current sensor. In addition, this paper proposes the offset compensation method. The proposed offset compensation method can remove the offset error and compensate the DC-link imbalance. The proposed compensation method is verified through experimental results.

II. CONTROL STRATEGY FOR THE PROPOSED TOPOLOGY

The controller of the proposed topology can be divided into two parts, as shown in Fig. 2. The converter side controller controls the DC voltage and input current [7]. The single-phase PLL method with imaginary axis made by all pass filter and synchronous reference frame transformation is used to estimate the phase of the grid system [8]. In addition, the PR controller for controlling the current is utilized [9]. The current controller reference signal is determined by the product of the outputs of voltage controller and grid phase estimation circuits. As a result, the power factor control is possible. Fig. 2(b) shows the inverter side controller. Fixed frequency current control is needed to control the linear compressor. Thus, the PR current controller is adopted because it is best suited for constant frequency control.

III. EFFECT OF CURRENT MEASUREMENT ERROR

Two types of current measurement errors exist: offset and scale errors. However, the single-phase system using a proportional-resonant (PR) controller in a stationary reference frame cannot recognize the measurement errors. In this chapter, the synchronous transformation is used to investigate the effect of each measurement error. In addition, the

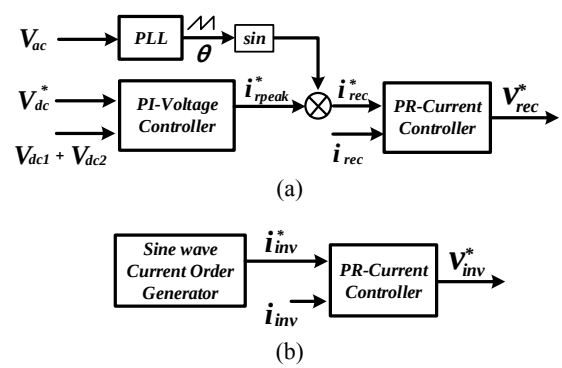

Fig. 2. Control system of the proposed topology. (a) Controller for the single-phase power converter. (b) Controller for the single-phase inverter.

unbalanced DC-link voltage caused by the offset error is analyzed.

Fig. 3 presents the block diagram of the current control system in consideration of the measurement error of the current sensor in the half-bridge inverter. The reference of the current controller is expressed as

$$i_{inv}^{*} = -I_m \sin \omega t \ . \tag{1}$$

The current is controlled by the PR controller, as expressed in the following:

$$G_c(s) = K_{pc} + \frac{2K_{rc}\omega_c s}{s^2 + 2\omega_c s + \omega^2} \ . \tag{2}$$

The measured current is expressed as

$$i_{\alpha\_m} = i_{inv} + \Delta I_{inv} \tag{3}$$

and

$$i_{\alpha\_m} = K_{inv} \cdot i_{inv} \tag{4}$$

where i_{inv}, ΔI_{inv}, and K_{inv} are the real current, the offset error, and the scale error, respectively. Equation (3) considers only the offset error, whereas equation (4) considers the scale error.

Such measurement error can be estimated by synchronous d–q reference frame transformation. The measured current is defined as d-axis current, and imaginary q-axis current can be generated by an all-pass filter for synchronous d–q reference transformation [9].

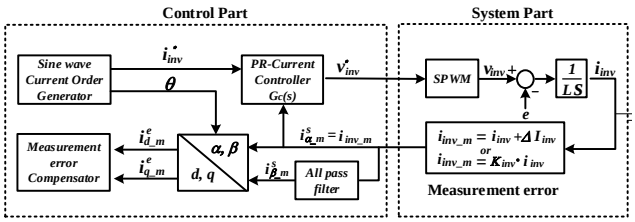

Fig. 3. Block diagram of the control system in consideration of measurement errors of the current sensor in the half-bridge inverter.

A. Effect of Offset Error

Offset error, which may be caused by a potential imbalance of current sensors and measurement path or other problems, is inevitable in current measurement. Current offset errors are commonly compensated by reading the A/D converter repeatedly without current flowing in the wire before the operation of inverter. However, completely compensating for the effects of the thermal drift of the analog devices and the switching noise when the system is actually running is impossible [10]-[12].

In this paper, the synchronous reference frame transformation is used to estimate the offset error. For the synchronous d–q reference transform, imaginary current with a phase shift of 90° is generated from Equation (3) through the all pass filter, as shown in

$$\begin{bmatrix} i^s_{\alpha\_m} \\ i^s_{\beta\_m} \end{bmatrix} = \begin{bmatrix} i_{inv} + \Delta I_{inv} \\ i_{inv+90^\circ} + \Delta I_{inv} \end{bmatrix} . \tag{5}$$

After the all-pass filter, DC offset component ΔI_{inv} still remains the same, despite the phase shift of 90°.

DC offset components ΔI^e_d and ΔI^e_q in synchronous reference frame can be obtained as follows:

$$\begin{bmatrix} i^e_{d\_m} \\ i^e_{q\_m} \end{bmatrix} = \begin{bmatrix} i^e_d + \Delta I^e_d \\ i^e_q + \Delta I^e_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i^s_{\alpha\_m} \\ i^s_{\beta\_m} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} i^e_d + \Delta I^e_d \\ i^e_q + \Delta I^e_q \end{bmatrix} = \begin{bmatrix} 0 + \sqrt{2}\Delta I_{inv}\sin(\theta + 45^\circ) \\ I_m - \sqrt{2}\Delta I_{inv}\sin(\theta - 45^\circ) \end{bmatrix} \tag{7}$$

and

$$\begin{bmatrix} \Delta I^e_d \\ \Delta I^e_q \end{bmatrix} = \begin{bmatrix} \sqrt{2}\Delta I_{inv}\sin(\theta + 45^\circ) \\ -\sqrt{2}\Delta I_{inv}\sin(\theta - 45^\circ) \end{bmatrix} \tag{8}$$

As shown in Equations (6)-(8), measured current in synchronous reference frame is composed of the offset error and the real current. The offset error has a ripple with a fundamental frequency of the inverter current. This offset component can be detected only in a synchronous reference frame.

B. Effect of Scale Error

The scale error may be caused by the nonlinearity of the current sensor itself, matching circuit between the current sensor and A/D input, and the nonlinearity of an A/D converter [10], [13]. The scale error can be expressed by the following equation when the measured current of the inverter contains the error:

$$\begin{bmatrix} i^s_{\alpha\_m} \\ i^s_{\beta\_m} \end{bmatrix} = \begin{bmatrix} K_{inv} \cdot i_{inv} \\ K_{inv} \cdot i_{inv} \end{bmatrix} . \tag{9}$$

From Equation (9), the d–q currents in synchronous reference frame can be derived as follows:

$$\begin{bmatrix} I^e_{d\_m} \\ I^e_{q\_m} \end{bmatrix} = \begin{bmatrix} 0 \\ K_{inv} \cdot I_m \end{bmatrix} \tag{10}$$

As shown in Equation (10), the scale error remains with the q-axis current component after the synchronous transformation.

The scale error causes energy efficiency reduction in the linear compressor. However, the scale error cannot be compensated without the information on scale error factor K_{inv} in this system. As a result, compensation of the scale error is not considered in this paper.

C. Effect of Offset Error on DC-Link Voltage

Fig. 4 shows the unbalanced DC-link voltage when the current sensor has the offset measurement error. V_{dc1} and V_{dc2} are the voltages on the upper capacitor (C_1) and the lower capacitors (C_2), respectively. ΔV_{dc1} and ΔV_{dc2} are the voltage variations on C_1 and C_2 in one period, respectively.

If the current sensor has an offset error, the measured current is different from the real inverter current. However, the current control performance of the digital processor relies on the measured current. If the current controller operates well, the reference current will be equal to the measured current, as shown in Fig. 4. However, the real current is different from the reference current.

As shown in Fig. 4, if the measured current includes a positive offset error, the real supply power is lower than the power of the reference current during the positive half cycle, whereas the real supply power is higher than the reference current for the negative half cycle. In addition, the discharging time of C_1 decreases in the positive current period, and charging time of C_1 increases in the negative current period. As a result, the voltage of C_1 increases. On the other hand, the voltage of C_2 decreases, and in the end, the DC-link finally goes into an unbalanced condition.

The voltage difference of each capacitor in one period can

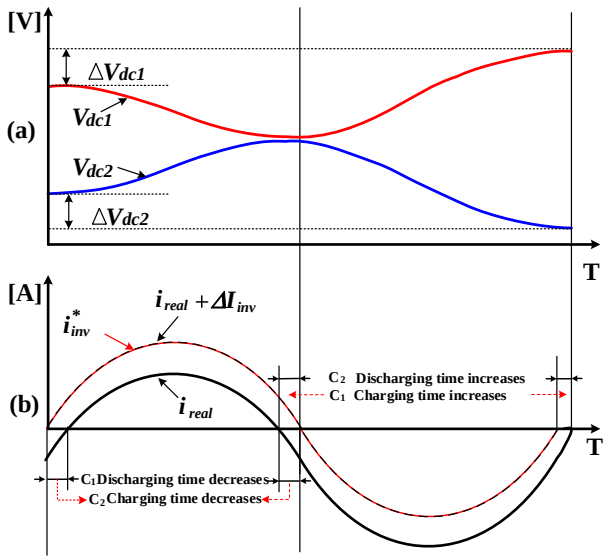

Fig. 4. Effect of the offset error on the DC-link. (a) Voltage variation of the DC-link. (b) Effect of the offset error between the control current and the real current.

be derived by calculating the average power supplied from the DC-link. The inverter output voltage is given by the following equation at the steady state:

$$v_{inv} = L_s \frac{di_{inv}}{dt} = -\omega L_s I_m \cos\omega t \,. \tag{11}$$

If no power loss occurs in the inverter, the power supplied from the DC-link to the inverter is similar to the effective power of the inverter. In addition, the source of the DC power is different according to the direction of the output current. For example, the upper capacitor supplies the power in the positive period of the output current. Thus, supply power can be obtained in two regions as follows:

1) Negative Output Current ($i_{inv} < 0$):

$$\begin{aligned} P_{dc1} &= I_{eff} \cdot V_{eff} \\ &= \sqrt{\frac{2}{T}\int_0^{\frac{T}{2}} (-I_m \sin\omega t - \Delta I_{inv})^2 dt} \cdot \sqrt{\frac{2}{T}\int_0^{\frac{T}{2}} (-\omega L_s I_m \cos\omega t)^2 dt} \\ &= \frac{\omega L_s I_m}{\sqrt{2}} \cdot \sqrt{\frac{I_m^2}{2} + (\Delta I_{inv})^2 + \frac{8\Delta I_{inv} I_m}{T\omega}} \end{aligned} \tag{12}$$

2) Positive Output Current ($i_{inv} \geq 0$):

$$\begin{aligned} P_{dc2} &= I_{eff} \cdot V_{eff} \\ &= \sqrt{\frac{2}{T}\int_{\frac{T}{2}}^{T} (-I_m \sin\omega t - \Delta I_{inv})^2 dt} \cdot \sqrt{\frac{2}{T}\int_{\frac{T}{2}}^{T} (-\omega L_s I_m \cos\omega t)^2 dt} \\ &= \frac{\omega L_s I_m}{\sqrt{2}} \cdot \sqrt{\frac{I_m^2}{2} + (\Delta I_{inv})^2 - \frac{8\Delta I_{inv} I_m}{T\omega}} \end{aligned} \tag{13}$$

The voltage variation of each DC-link capacitor in one period can be derived as follows:

$$\begin{aligned} \Delta V_{dc1} &= \sqrt{\frac{TC}{4}(P_{dc1} - P_{dc2}) + V_{dc1}^2} - V_{dc1} \\ \Delta V_{dc2} &= \sqrt{\frac{TC}{4}(P_{dc2} - P_{dc1}) + V_{dc2}^2} - V_{dc2} \end{aligned} \tag{14}$$

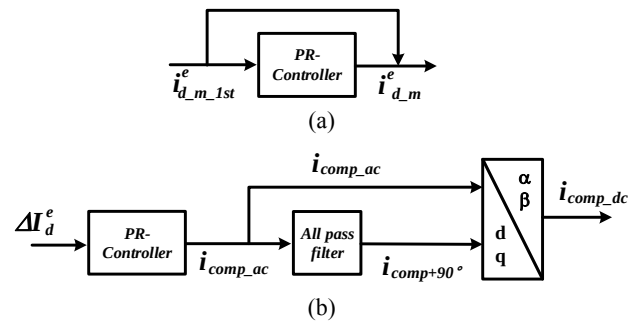

Fig. 5. (a) Conventional use of the PR controller. (b) Proposed compensation method.

IV. PROPOSED CURRENT OFFSET ERROR COMPENSATION METHOD

The conventional method [10], [11] can compensate the offset error by using the integration term of the d-axis current of the synchronous reference frame. However, this method needs one period of the integration time. Thus, it needs much compensation time.

On the other hand, this paper proposes the PR controller to compensate the offset error. The PR controller has high gain at the resonant frequency. It is specialized in the AC system [9]. As shown in previous equations (7) and (8), the ripple component of the d-axis current has a specific frequency. The generalized PR controller shown in Fig. 5(a) can eliminate the ripple component [14]. However, the unbalanced DC-link voltage cannot be compensated by the PR controller. Thus, the compensation component should be injected to the measured current to simultaneously compensate both the offset error and the unbalanced DC-link voltage.

Fig. 5(b) shows the proposed compensation method. The PR controller for the compensation is used in the same way as the PR-current controller in the following equation, and the input of PR controller is ΔI_d^e, as in Equation (8):

$$G_{comp}(s) = K_{pc} + \frac{2K_{rc}\omega_c s}{s^2 + 2\omega_c s + \omega^2} \,. \tag{15}$$

i_{comp_ac} is the AC component, which is not suitable to compensate the DC component of the offset error. Thus, the synchronous reference transformation is again used to change i_{comp_ac} to the DC value. i_{comp_dc} is derived as Equations (16) and (17):

$$\begin{bmatrix} i_{comp\_dc} \\ i_{comp\_dc+90°} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \Delta I_{off} \sin(\theta + 45°) \\ -\Delta I_{off} \cos(\theta + 45°) \end{bmatrix} \tag{16}$$

and

$$\begin{bmatrix} i_{comp\_dc} \\ i_{comp\_dc+90°} \end{bmatrix} = \begin{bmatrix} \Delta I_{off}^{'} \\ -\Delta I_{off}^{'} \end{bmatrix} . \tag{17}$$

Finally, compensating current i_{comp_dc} is injected to the measured current by using the PI-controller. The overall

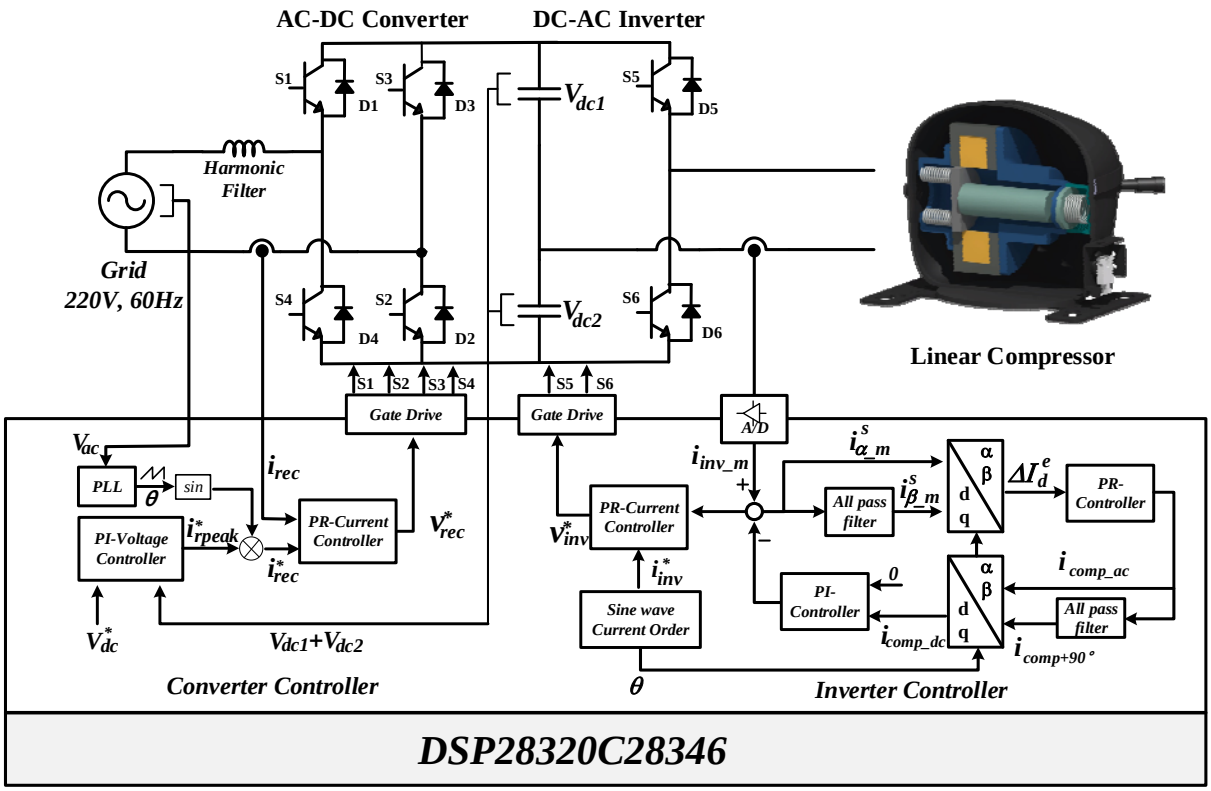

Fig. 6. Block diagram of the proposed compensation scheme.

block diagram of the proposed compensation system is shown in Fig. 6.

V. EXPERIMENTAL RESULTS

The experiment is conducted by simultaneously operating the converter control and inverter control systems. The converter controls the DC-link voltage at 400 V, and the inverter uses fixed frequency control, keeping the linear compressor current at 1 A. The control parameters and system parameters used for the experiment are shown in Table I. The offset error is injected by software on the measured current of the inverter. The linear compressor is operated in a no-load condition.

Fig. 7 shows the unbalanced DC-link voltage when the offset error is injected to the measured current, where i_{inv_m} is the measured current, and i_{inv} is the real current sensed by the current probe. As shown in Fig. 7(a), a 26-V voltage difference occurs between the two capacitors when an offset error of 0.1 A is injected to the measured current. On the other hand, Fig. 7(b) shows the 52-V voltage difference between the upper and lower capacitors when -0.1 A of the offset error is injected. This difference between Figs. 7(a) and (b) occurs because of the internal offset error produced during the current measurement prior to the injection of experimental offset signal. Finally, Fig. 7(c) shows the balanced DC-link voltages and current after compensation is made for an injected offset current of 0.1 A.

TABLE I
CONTROL PARAMETERS

Parameter of Power Converter	Grid Voltage	220 V	Grid Frequency	60 Hz
	DC-Link Capacitor	4,700 uF	Filter Inductor	5 mH
	Switching Frequency	10 kHz	DC Voltage Order	400 V
Parameter of Power Inverter	Switching Frequency	10 kHz	Current Order	1 A
			Injected Offset Error	±0.1 A
Parameter of Linear Compressor	Rate Power	750 W	Rate Frequency	60 Hz
	Inductance	350 mH	Register	10 Ω

Fig. 8 shows the d-axis current of the synchronous reference frame and its FFT result when the offset error is injected. The injected offset is 0.1 and –0.1 A in Figs. 8(a) and 8(b), respectively. The FFT result in Fig. 8 shows the magnitude of ΔI_{inv} in the d-axis current. Ideally, this value must be similar for both 0.1 and -0.1 A offset injection. The difference in the two values appears because of the real offset

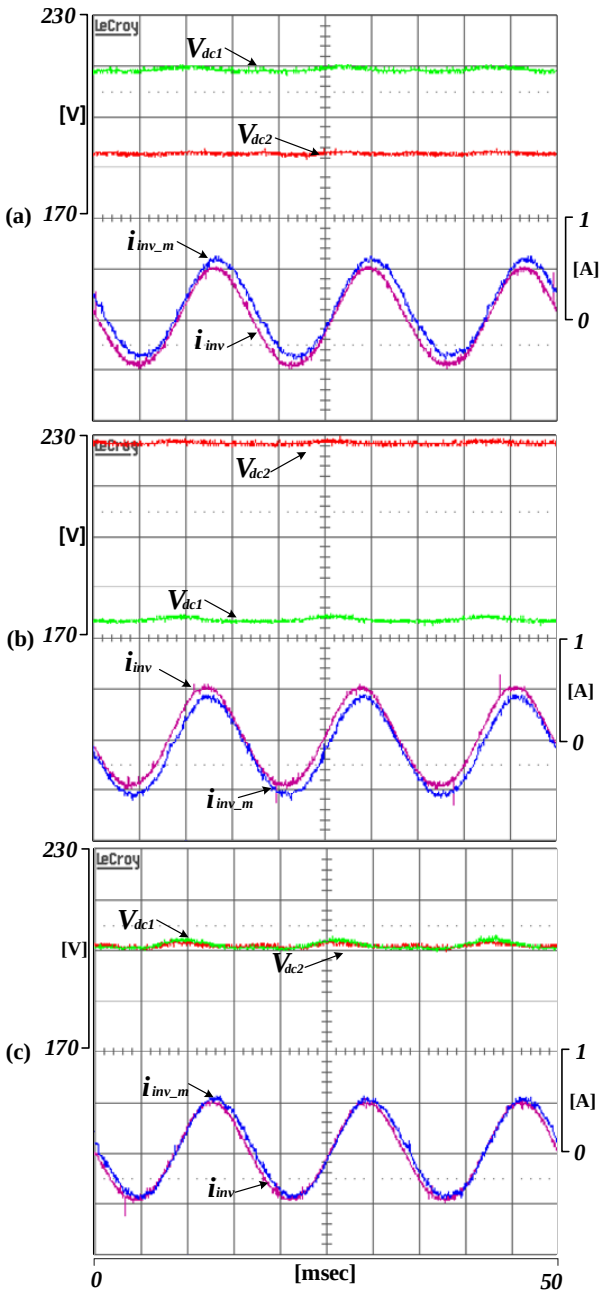

Fig. 7. Unbalance voltage of the DC-link, the real current, and the measured current. (a) 0.1 A of offset error is injected. (b) -0.1 A of offset error is injected. (c) DC voltage after compensating the offset error.

error caused by the current sensing path prior to the injection of the offset current. Finally, Fig. 8(c) shows the balanced DC link voltage after the compensation when the injected offset error is 0.1 A.

Fig. 9 shows the output value of the compensator and the DC-link voltages when the injected offset error is 0.1 A. The compensation starting time is 0.25 s, and the steady-state value of the compensation signal is 0.075 A. A difference of -0.025 value with injected offset error appears because the system has an internal offset error.

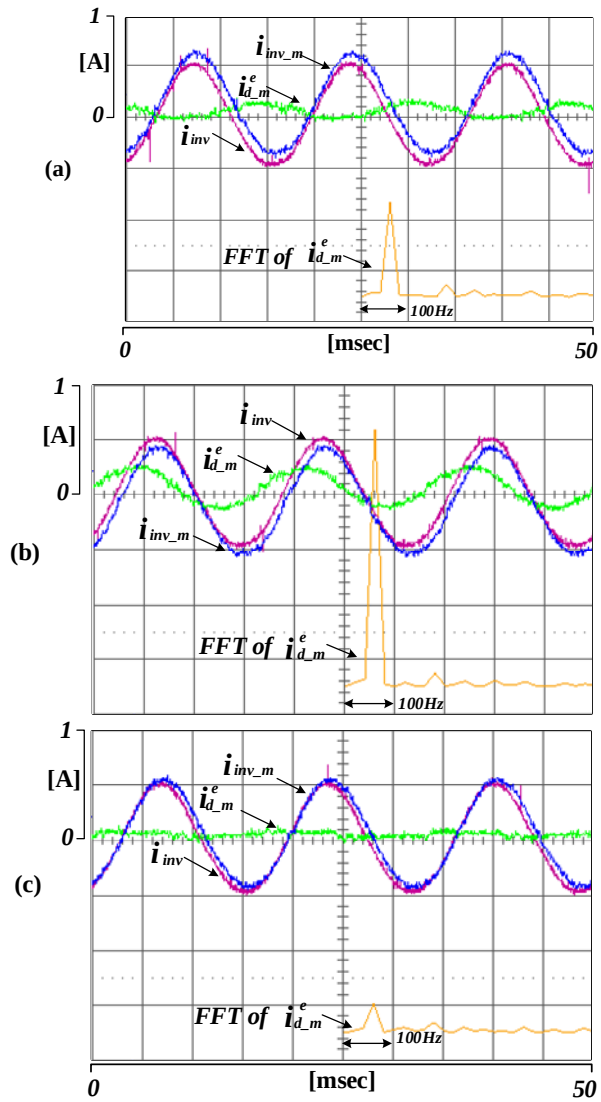

Fig. 8. d-axis current and FFT result with offset error. (a) 0.1 A of offset error is injected. (b) -0.1 A of offset error is injected. (c) DC voltage after compensating the offset error.

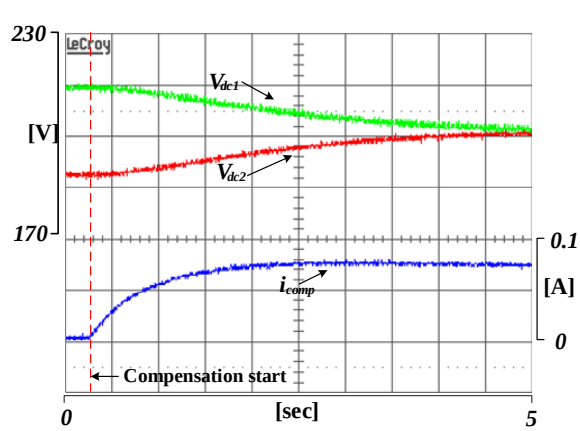

Fig. 9. Characteristic of compensation.

VI. CONCLUSION

This paper has proposed a suitable topology to control the linear compressor. The series-connected capacitor of the DC-link is the feature of the proposed topology. When an offset error exists in the half-bridge inverter, an imbalance will occur in the DC-link. This paper has proposed a compensation method to solve the offset error. The synchronous reference transformation and the PR controller are used to compensate the offset error. The proposed compensation method ensures safe operation of the compressor system by protecting the switching elements and the DC-link from breakdown. In addition, the proposed method is simple to implement. The feasibility and effectiveness of the proposed compensation method were verified through experimentation.

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Dong-Youn Kim was born in Ulsan, Korea, in 1983. He received the B.S. and M.S. degrees in Electrical Engineering from Pusan National University, Busan, Korea, in 2011 and 2013, respectively, where he is currently working toward the Ph.D. degree. His research interests include power conversion, electric machine drives, and electrical vehicle propulsion.

Won-Sang Im was born in Busan, Korea, in 1981. He received the B.S., M.S and Ph.D. degrees in Electrical Engineering from Pusan National University, Busan, in 2007, 2009, and 2013, respectively. He is currently a Postdoctoral researcher in Lehigh University, Bethlehem, PA, USA. His research interests include power conversion, electric machine drives, and their diagnosis and fault tolerance.

Seon-Hwan Hwang was born in Chungnam, Korea, in 1978. He received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Pusan National University, Busan, Korea, in 2004, 2006, and 2011, respectively. From 2011 to 2012, he was with the Center for Advanced Power Systems (CAPS), Florida State University, Tallahassee, FL, USA. In 2012, he joined the Department of Electrical Engineering, Kyungnam University, Changwon, Korea. His current research interests include control of electrical machines, power electronics, and wind power generation systems.

Jang-Mok Kim received the B.S. from Pusan National University (PNU), Korea, in 1988, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Seoul National University, Seoul, Korea, in 1991 and 1996, respectively. From 1997 to 2000, he was a Senior Research Engineer with Korea Electrical Power Research Institute (KEPRI). Since 2001, he has been with the School of Electrical Engineering, PNU, where he is currently a Research Member of the Research Institute of Computer Information and Communication, a Faculty Member, and a head of LG electronics Smart Control Center. He joined the Center for Advanced Power Systems (CAPS), Florida State University, Tallahassee, FL, USA, as a Visiting Scholar in 2007. His current interests include the control of electric machines, electric vehicle propulsion, and power quality.