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# An Improved Carrier-based SVPWM Method By the Redistribution of Carrier-wave Using Leg Voltage Redundancies in Generalized Cascaded Multilevel Inverter

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## ABSTRACT

The carrier-based space vector pulse width modulation (SVPWM), which is considered as highly simple and efficient PWM technology, can be also used in multilevel inverters The method was originally designed for the two-level inverter and developed to the diode clamped multilevel inverter structure However it may be noted that it also cause bad switch utilization in cascaded multilevel inverter This paper introduces an improved carrier-based SVPWM scheme, which is fully suitable for cascaded multilevel inverter topologies because it can achieve the optimized switch utilization through the redistribution of the triangular carrier waves considering leg voltage redundancies while having the advantages of the conventional carrier-based SVPWM Using simulation and experimental results, the superior performance of new PWM method is shown

**Key Words** : carrier based SVPWM, switch utilization, switch redundancy, cascaded multilevel inverter

## 1. Introduction

In recent years, multilevel inverters have been focused on and selected as high power and high voltage ones. These multilevel inverters, in case of N-level, can increase the capacity by (N-1) times than that of two-level inverter through the series connection of power semiconductor devices without additional circuit in order to have uniform voltage sharing

Comparing with two-level inverter system having the same capacity, multilevel inverters have the advantages that the harmonic components of line-to-line voltages fed to motor, switching frequency of the devices and EMI problem could be much decreased. Due to those merits, many studies about multilevel inverters have been performed since Nabae proposed neutral-point-clamped inverter called as three-level inverter [1]

Up to now, the multilevel topologies are classified into three categories: diode clamped inverter, flying capacitor inverter, and cascaded inverter. In the three-phase inverter system, the number of main switches of each topology is equal Comparing with the number of other components, for example, clamping diodes and DC-link capacitors having the same capacity per unit, diode clamped inverter has the least number of capacitors among the three types but requires the additional clamping diodes Flying capacitor inverter needs the most number of capacitors But cascaded inverter is considered as having the simplest structure [2]

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Diode clamped inverter, particularly the three-level one, has taken much interest in motor drive applications because it needs only one common voltage source and many simple and efficient PWM algorithms have been developed, even if it has inherent unbalanced DC-link capacitor voltage problem[3]-[5] However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering DC-link balancing and much number of clamping diodes.

Cascaded inverter has structurally no problem of DC-link voltage unbalancing but has a problem to require many separated DC sources in motor drive applications So the cascaded inverter has been largely studied and used in fields of SVCs (static VAR compensators), power line conditioner, voltage stabilizer and so on[6]-[9]. It may be noted that due to another advantages of the modularized circuit layout and package, the cascaded inverter could be a good choice in motor drive applications with higher voltage as well as pre-mentioned branches.

The studies to improve the switch utilization for the cascaded inverter have been performed in various methods. Marchesoni presented a PWM method using two clock pointers in single-phase three-level cascaded inverter [10] The method has the feature that all the switch components operate at the same switching frequency with very similar duty cycles in both high and low modulation index But this PWM strategy is very difficult to be applied to the three-phase and higher-level cascaded inverter Peng contributed several papers related to cascaded inverter for the utility and the motor applications[9], [11], [12] In the methods, the switches are turned on and off once per modulation cycle considering reactive power compensation and switching utilization in three-phase eleven-level cascaded inverter. The method used stair pulses to synthesize eleven-voltage level. But this is not PWM method Recently, Tolbert proposed a PWM method at low modulation indices applied to both diode-clamped inverters and cascaded inverters for motor drive application[12]. The method used the redundant output voltage states and level rotation during each cycle to increase device utilization. But the method has the demerit that the switch utilization is improved only at low modulation indices. This paper deals with the PWM method for generalized cascaded inverter, which improves the switch utilization at the modulation indices and is extended easily to n-level

A carrier-based SVPWM method was developed in the diode-clamped inverter[5] The method has the advantage of simplicity in expansion to higher levels, maintaining the property of the SVPWM method based on the voltage-second balance principle. Diode-clamped inverter has no leg voltage redundancy, which leads to the property of bad switch utilization. If it is directly applied to cascaded inverter, the switching frequency of devices and the current flowing through the devices become different in each device, which result in bad switch utilization, too A new carrier-based SVPWM method was presented in order to achieve the optimized switch utilization using output leg voltage redundancies in odd-level cascaded inverter[13]. At that time, the cascaded inverter structure was regarded as having no even-level. But new topology was developed for even-level cascaded inverter in the wide meaning[14]

This paper is focused on an improved carrier-based SVPWM scheme for the generalized cascaded inverter The leg voltages for two types of four-level inverter are compared and then an improved carrier-based SVPWM method is described through the comparison of conventional one The proposed method has the following features

- Carrier-based SVPWM method using adjacent voltage vectors ,
- Easy expansion to higher levels ;
- Redistribution of carrier using the leg voltage redundancies ;
- Same utilization of all the switches at both high and low modulation indices even if the load power factor varies ,
- Even dispersion of on-off gate pulses for each switch.

## 2. Conventional Carrier-Based SVPWM

### 2.1 Diode Clamped Inverter

Fig. 1 shows a circuit for one leg of four-level diode clamped inverter. Here, the switches of $S_{a1}$ and $S_{a1}'$ represent complementary operation As shown in Table 1,

four switch states exist in four-level diode clamped inverter according to the switch sequences to produce leg voltages

Table 1 Leg voltages, their switch states and switch sequences of four-level diode clamped inverter

| Output leg voltage ($V_{an}$) | Switch State | Switch Sequence | | |
|---|---|---|---|---|
| | | $S_{a1}$ | $S_{a2}$ | $S_{a3}$ |
| $V_{dc}$ | 3 | 1 | 1 | 1 |
| $2V_{dc}/3$ | 2 | 0 | 1 | 1 |
| $V_{dc}/3$ | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

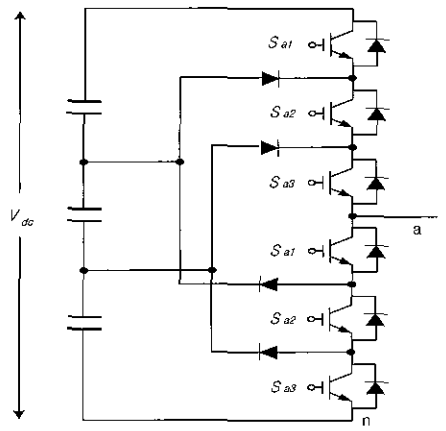



Fig 1 A circuit for one leg of four-level diode clamped inverter

There is only one switch state to each leg voltage and no leg voltage redundancy, which is defined as the different switch sequence or switch state having the same leg voltage Here *1* and *0* imply turn-on and turn-off of the switch, respectively. And *0, 1, 2, 3* are switch states. For example, *3* represents the switch state to produce leg voltage of $V_{dc}$ and to have the switch sequence *111*. *111* implies that $S_{a1}$, $S_{a2}$ and $S_{a3}$ are turned on. The leg voltages are synthesized as follows ,

1) For leg voltage $V_{dc}$. switch state *3* - switch sequence *111* ($V_{an} = V_{dc}/3 + V_{dc}/3 + V_{dc}/3$)
2) For leg voltage $2V_{dc}/3$ : switch state *2* - switch sequence *011* ($V_{an} = 0 + V_{dc}/3 + V_{dc}/3$)
3) For leg voltage $V_{dc}/3$ : switch state *1* - switch sequence *001* ($V_{an} = 0 + 0 + V_{dc}/3$)
4) For leg voltage 0 . switch state *0* - switch sequence *000* ($V_{an} = 0 + 0 + 0$)

## 2.2 Conventional Carrier-Based SVPWM

Fig 2 shows a space voltage vector diagram for four-level diode clamped inverter The reference voltage vector ($V^* = V_d + jV_q$) of a stationary reference frame can be converted into the imaginary phase voltages ($V_{as}'$, $V_{bs}'$, $V_{cs}'$) by dq/abc transformation given in (1)

$$\begin{bmatrix} V_{as}' \\ V_{bs}' \\ V_{cs}' \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & +\sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (1)$$

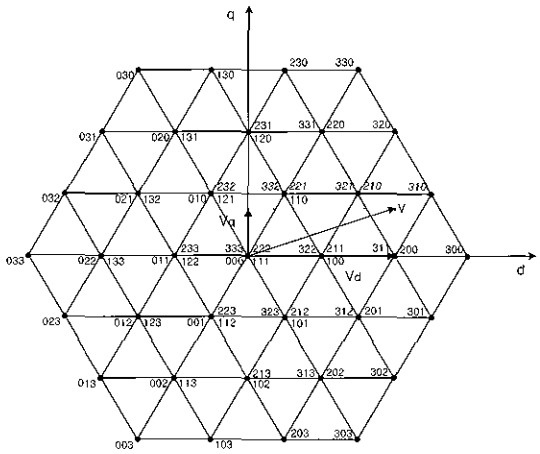



Fig 2 A space voltage vector diagram for four-level diode clamped inverter

The effective phase voltages ($V_{xs}$) can be obtained by adding the voltage offset ($V_{offset}$) in (2) to this imaginary phase voltages in (1) and is represented in (3),

$$V_{offset} = \frac{V_{dc} - V_{max} - V_{min}}{2} \quad (2)$$

where, $V_{max}$ and $V_{min}$ is the maximum and minimum voltage among the imaginary phase voltages, respectively

The offset voltage is a kind of zero sequense voltage and is calculated in order to partition zero voltage vectors in two-level inverter and small voltage vectors in multilevel inverter.

$$V_{xs} = V_{xs}' + V_{offset} \ (x = a, b, c) \quad (3)$$

The effective voltages are compared with the triangular carrierwaves to obtain gate signals.

### 2.3 Problem of switch utilization

Fig. 3 shows PWM scheme for the conventional carrier-based SVPWM method Each carrier from upper is compared with the effective phase voltage in the previous section to obtain gate signals $G_{a1}$, $G_{a2}$, $G_{a3}$. The intersections of carrier wave and effective phase voltage represent the instants of switching commutation. When the effective phase voltage is larger than carrier wave, the switch is turned on and otherwise turned off When the modulation index is high as shown in Fig. 3, where the modulation index ($MI$) is defined as $MI=V^*/(V_{dc}/\sqrt{3})$, the switches of $S_{a1}$ and $S_{a3}$ have the same switching frequency but the switch $S_{a2}$ has less switching frequency than those Moreover, as the bottom switch $S_{a3}$ has larger turn-on interval than the upper Switch $S_{a1}$, the switch $S_{a3}$ has larger rms current than that of $S_{a1}$ In case of low $MI$, the switches of $S_{a1}$ and $S_{a3}$ have no switching but the switch $S_{a2}$ has the largest switching frequency

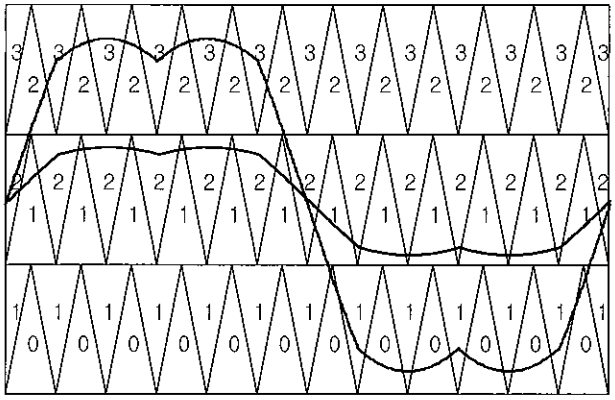


Fig 3 PWM scheme of the conventional carrier-based SVPWM method for four-level diode clamped inverter

The current of switch $S_{a3}$ is larger than that of switch $S_{a2}$ and no current flows in switch $S_{a1}$ So this PWM method has different switching frequencies and different rms currents among switch devices according to the modulation indices

If the load power factor is changed by the use of the load with the different parameters and the modulation index has the constant value larger than 1/3, the rms current of each switch varies Also after the change of the load power factor, each switch has the different division of current. Assuming that the gate signals of switch $S_{a1}$ and $S_{a2}$ are given as shown in Fig 4, the rms currents of $S_{a1}$ and $S_{a2}$ decreases and has still the different value as the load power factor changes form (a) to (b)

Therefore, the conventional carrier-based SVPWM method has the bad switch utilization because it was derived from diode-clamped inverter structure having no leg voltage redundancy This PWM scheme can be directly applied to cascaded inverter, but it concentrates the voltage and the current stress on one device This leads to confine switching frequency to low value and requires the different design of heat sink So this method needs to be modified to improve the switch utilization in cascaded inverter and a new scheme is described in the next section

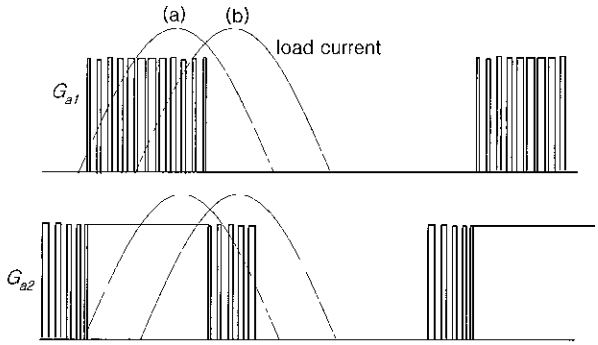



Fig 4 The effect of the variations in load power fact or on the rms current in the switch

## 3. Improved Carrier-Based SVPWM in generalized cascaded inverters

### 3.1 Four-level cascaded inverter

Fig. 5 shows a circuit for four-level cascaded inverter in the wide meaning. The topology is composed of odd-level cascaded inverter and two-level inverter Even-level structure is obtained by cascaded connection of these inverters. Table 2 represents possible switch states and switch sequences to produce leg voltages The subscripts in switch states display the leg voltage redundancies and no subscript no leg voltage redundancy. The leg voltages are synthesized as follows,

1) For leg voltage $2V_{dc}/3$ : switch state *3* -- switch sequence *111* ($V_{an} = V_{dc}/3+ V_{dc}/3$)
2) For leg voltage $V_{dc}/3$ :

a) switch state $2_1$ - switch sequence *011* ($V_{an}$ = 0+ $V_{dc}$/3)
b) switch state $2_2$ - switch sequence *101* ($V_{an}$ = 0+ $V_{dc}$/3)
c) switch state $2_3$ - switch sequence *110* ($V_{an}$ = $V_{dc}$/3+0)

3) For leg voltage 0
a) switch state $1_1$ - switch sequence *010* ($V_{an}$ = 0+0)
b) switch state $1_2$ - switch sequence *001* ($V_{an}$ = - $V_{dc}$/3+ $V_{dc}$/3)
c) switch state $1_2$ - switch sequence *100* ($V_{an}$ = 0+0)

4) For leg voltage -$V_{dc}$ /3 · switch state *0* - switch sequence *000* ($V_{an}$ = -$V_{dc}$/3+0)

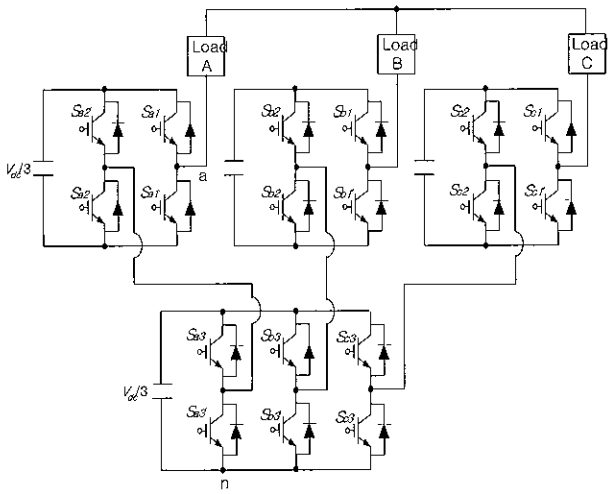



Fig 5 A circuit for three legs of four-level cascaded inverter

Table 2 Four-level cascaded inverter leg voltages, their switch states and their switch sequences

| Output leg voltage ($V_{an}$) | Switch State | Switch Sequence | | |
|---|---|---|---|---|
| | | $S_{a1}$ | $S_{a2}$ | $S_{a3}$ |
| $2V_{dc}$/3 | *3* | *1* | *1* | *1* |
| $V_{dc}$/3 | $2_1$ | *0* | *1* | *1* |
| | $2_2$ | *1* | *0* | *1* |
| | $2_3$ | *1* | *1* | *0* |
| 0 | $1_1$ | *0* | *1* | *0* |
| | $1_2$ | *0* | *0* | *1* |
| | $1_3$ | *1* | *0* | *0* |
| -$V_{dc}$/3 | *0* | *0* | *0* | *0* |

The cascaded inverter has many leg voltage redundancies, which is one of the merits. Those can be used for various purposes In this paper, the utilization of switches becomes equal through two rules using leg voltage redundancies

### 3.2 New carrier-based SVPWM

Fig 6 shows the proposed PWM scheme. In the figure the reference voltage is the same effective phase voltage as Fig 3

The proposed new carriers are obtained by redistribution of triangular waves considering each switch state, which is explained by following two rules.

First, all the switches are turned on and off one time during $2(n\text{-}1)T_s$ if the switch states given as Table 2 and the distribution of the switch states given as Fig 6 are used Here, n is level number of leg voltage and $T_s$ is sampling period So in case of four-level, three switches are turned on and off one time during $6T_s$. Since six switching occurs during $6T_s$, one switching occurs during $T_s$ on average Consequently, total number of switching has no variation as compared with conventional method, but the switching frequency in each switch become equal one another unlike conventional one

Second, the switch state determines current path of switches So the uniform selection of the possible switch states makes the currents flowing through each switch equal In case of four-level, the switch states of $2_1$, $2_2$, $2_3$ select respectively two switches among $S_{a1}$, $S_{a2}$, $S_{a3}$ during $6T_s$ to conduct As each switch state is used one time in turn during $6T_s$, each switch has the same current division.

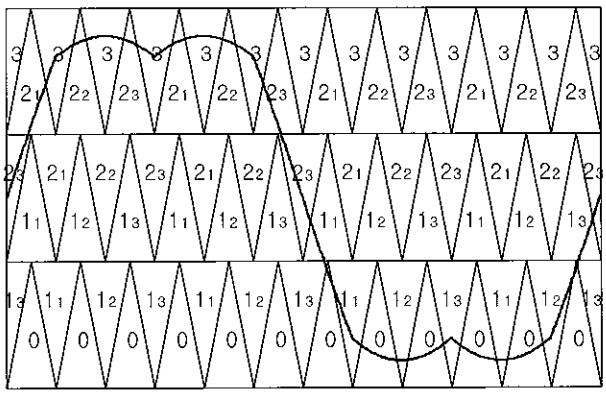


Fig 6 The proposed PWM scheme for four-level cascaded inverter

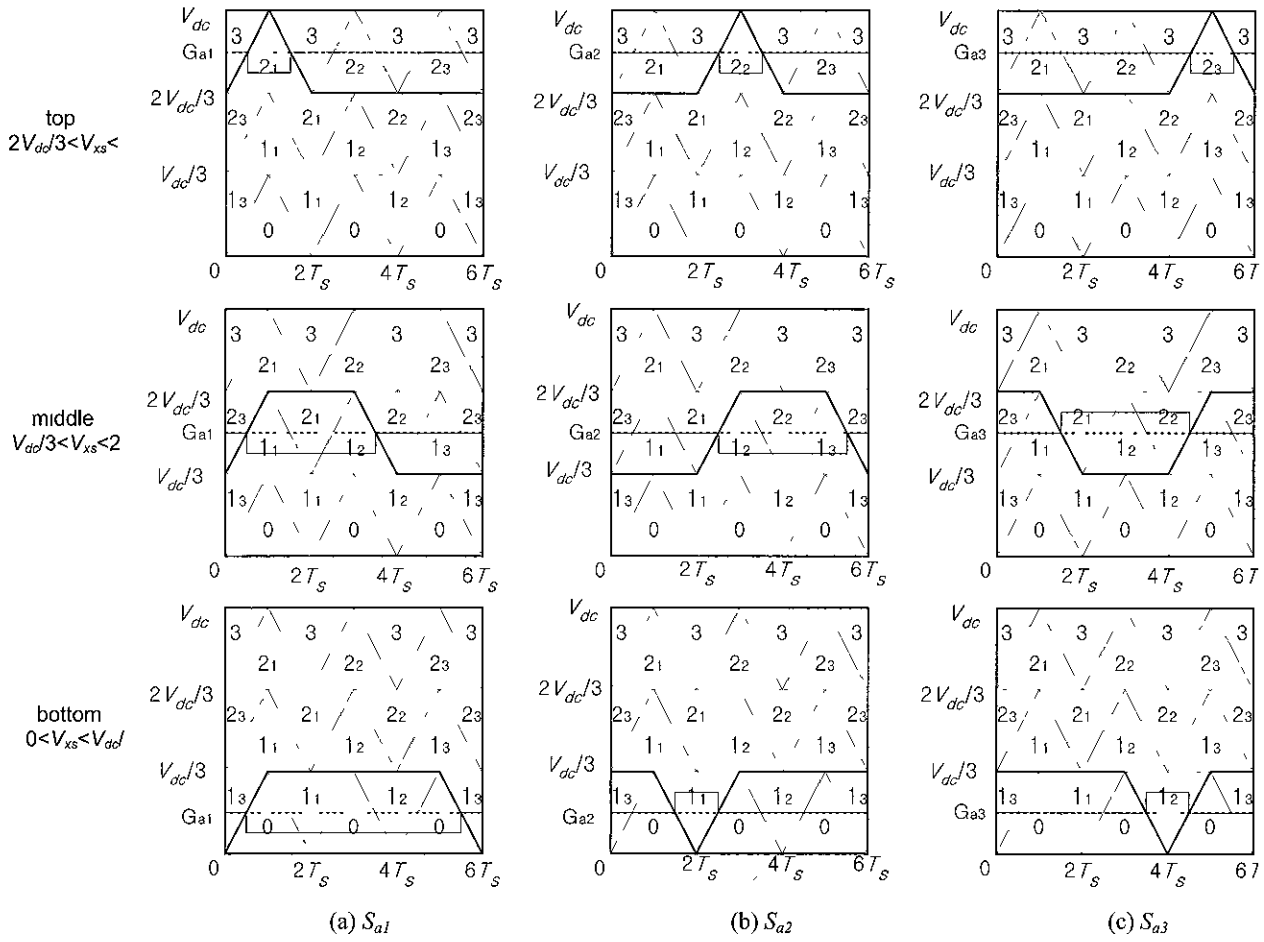



Fig 7 A mechanism to obtain new carriers for (a) $S_{a1}$, (b) $S_{a2}$ and (c) $S_{a3}$

Fig. 7 shows a mechanism to obtain new carriers, which are derived from Fig. 6 and Table 2 using two rules Fig 7(a) represents the new carriers for $S_{a1}$, 7(b) for $S_{a2}$, and 7(c) for $S_{a3}$, respectively. In the figure, the thin dot is the triangular waves, the thick dot is the effective phase voltage, the thin line is the gating pulse and the thick line is the new carrier New carrier for the switch $S_{a1}$ is achieved as follows

Firstly, in case of $2V_{dc}/3<V_{xs}<V_{dc}$ the switch state varies with $3\text{-}2_1\text{-}3\text{-}2_2\text{-}3\text{-}2_3\text{-}3$ from Fig 7(a) top and at this time the switch sequence for $S_{a1}$ varies with $1\text{-}0\text{-}1\text{-}1\text{-}1\text{-}1\text{-}1$ from Table 2. Thus the switching for $S_{a1}$ occurs only for the switch state of $3\text{-}2_1\text{-}3$ It remains turn-on in the other switch states except for $2_1$ Consequently, such carrier as the thick line of Fig 7(a) top can be obtained

Secondly, in case of $V_{dc}/3<V_{xs}<2V_{dc}/3$ the switch state varies with $2_3\text{-}1_1\text{-}2_1\text{-}1_2\text{-}2_2\text{-}1_3\text{-}2_3$ from Fig. 7(a) middle and at this time the switch sequence for $S_{a1}$ varies with $1\text{-}0\text{-}0\text{-}0\text{-}1\text{-}1\text{-}1$ from Table 2. Thus the switching for $S_{a1}$ occurs only in the switch state of $2_3\text{-}1_1$ and $1_2\text{-}2_2$ It remains turn-on in switch states of $1_3$, $2_2$, $2_3$ and turn-off in switch state of $1_1$, $1_2$, $2_1$ Consequently, such carrier as the thick line of Fig 7(a) middle can be obtained

Thirdly, in case of $0<V_{xs}<V_{dc}/3$ the switch state varies with $1_3\text{-}0\text{-}1_1\text{-}0\text{-}1_2\text{-}0\text{-}1_3$ from Fig. 7(a) bottom and at this time the switch sequence for $S_{a1}$ varies with $1\text{-}0\text{-}0\text{-}0\text{-}0\text{-}0\text{-}1$ from Table 2 Thus the switching for $S_{a1}$ occurs only in the switch state of $1_3\text{-}0$ and $0\text{-}1_3$ It remains turn-off in other switch states except for $1_3$. Consequently, such carrier as the thick line of Fig 7(a) bottom can be obtained.

Carrier waves for $S_{a2}$ and $S_{a3}$ can be derived like Fig 7(b) and 7(c) by the similar manner Note that the new carriers for $S_{a2}$ and $S_{a3}$ are equal to shifting those for $S_{a1}$

by $2T_s$ and $4T_s$, respectively

The switches always turn on and off one time during $6T_s$ regardless of modulation indices from the new carriers in Fig 7 Since the gate pulses by new method are distributed uniformly and are shifted by $2T_s$, rms currents of each switch vary but have the same value as the load power factor varies from (a) to (b)

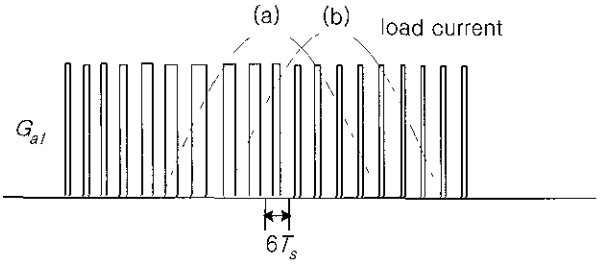



Fig 8 The effect of the variations in load power fact or on the rms current in the switch

### 3.3 Generalization to n-level

The generalization to n-level is performed by two rules with each switch state Fig. 9 shows the total number of the switch states having the same leg voltage in n-level cascaded inverter including even-level. But a limitation is accompanied that $2(n\text{-}1)$ switching cannot be obtained during $2(n\text{-}1)T_s$ by the new PWM method if all the switch states in Fig. 9 are selected Thus the possible switch states as shown in Fig 10 are used in order to keep two rules

| | | | | | | |
|---|---|---|---|---|---|---|
| 3-Level | | | 1 | 2 | 1 | |
| 4-Level | | 1 | 3 | 3 | 1 | |
| 5-Level | 1 | 4 | 6 | 4 | 1 | |
| 6-Level | 1 | 5 | 10 | 10 | 5 | 1 |

Fig 9 The possible number of switch states to make leg voltages in cascaded multilevel inverters

| | | | | | | |
|---|---|---|---|---|---|---|
| 3-Level | | | 1 | 2 | 1 | |
| 4-Level | | 1 | 3 | 3 | 1 | |
| 5-Level | 1 | 4 | 4 | 4 | 1 | |
| 6-Level | 1 | 5 | 5 | 5 | 5 | 1 |

Fig 10 The number of switch states used in the proposed PWM method to keep two rules

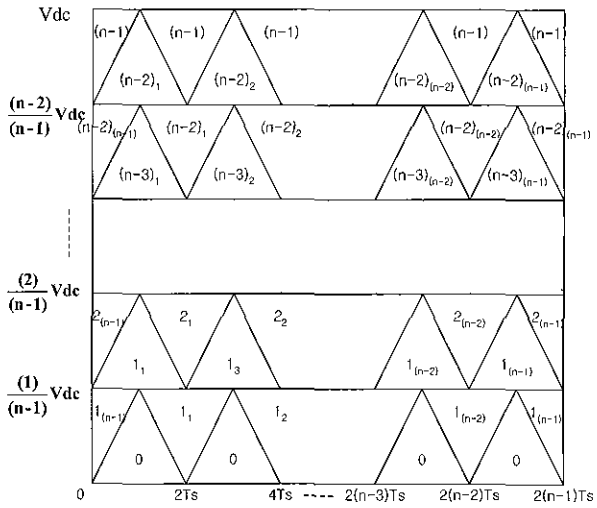



Fig 11 The proposed distribution of possible switch states generalized to $n$-level

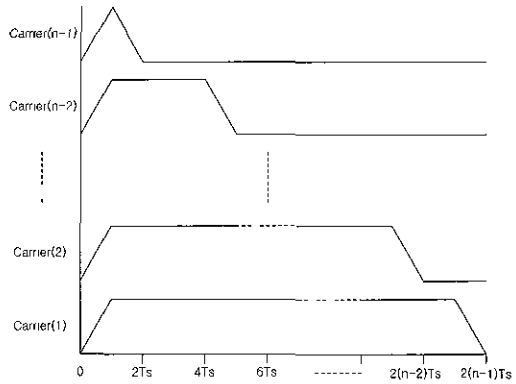



Fig 12 The new carriers generalized to $n$-level

Fig 11 and Fig 12 show the proposed distribution of possible switch states and new carriers for $S_{a1}$ when generalized to $n$-level The carriers for other switches are equal to shifting those for $S_{a1}$ by $2T_s$, , $2(n\text{-}2)T_s$, respectively

## 4. Simulation and Experiment Results

The simulation verifies the proposed method through comparing with the conventional method under same conditions The simulation is performed in three phase four-level cascaded inverter model with $R$-$L$ load as shown in Fig. 5 using *MATLAB*. Two PWM schemes are

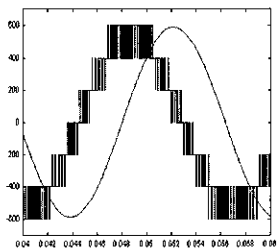
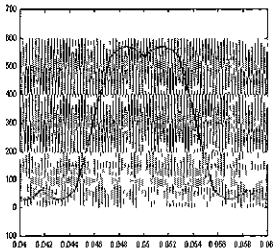
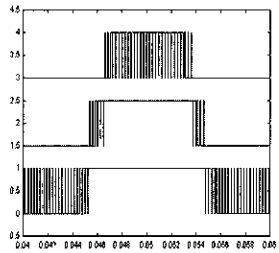
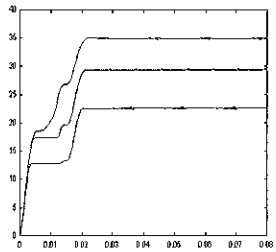
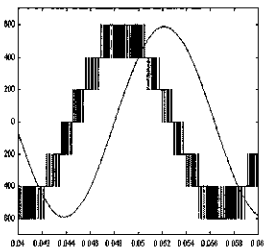
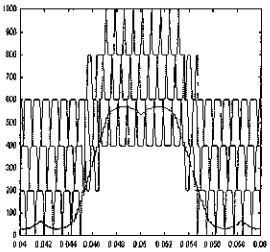


(a) (b)


(c) (d)

Fig 13 Simulation results for **four-level region operation** by the **conventional** PWM method (a) $I_a$ ×10 and $V_{ab}$ (b) PWM scheme reference voltage for phase A and carrierwaves for $S_{a1}$ , $S_{a2}$ , $S_{a3}$ (c) gate pulses for $S_{a1}$, $S_{a2}$ , $S_{a3}$ from top (d) rms currents for $S_{a1}$ , $S_{a2}$ , $S_{a3}$ from bottom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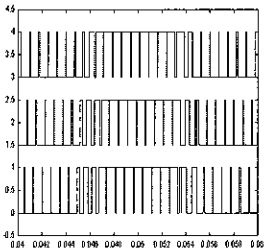
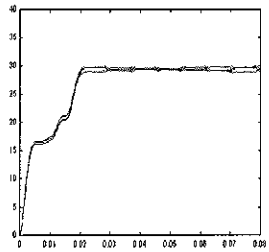
(c) (d)

Fig 14 Simulation results for **four-level region operation** by the **proposed** PWM method (a) $I_a$ ×10 and $V_{ab}$ (b) PWM scheme reference voltage for phase A and bottom-carrierwave for $S_{a1}$ , middle- 200+carrierwave for $S_{a2}$ , top- 400+carrierwave for $S_{a3}$ (c) gate pulses for $S_{a1}$, $S_{a2}$, $S_{a3}$ from top (d) the same rms currents for $S_{a1}$ , $S_{a2}$ , $S_{a3}$

simulated in turn according to the operation regions. Simulation conditions are as follows; load resistance per phase-3.7$\Omega$, load inductance per phase-10$mH$, capacitance per unit-5000$\mu F$, output frequency-60$Hz$, total DC link voltage-600$V$, capacitor voltage charged per unit-200$V$, sampling time-125$\mu s$. The modulation indices ($MI$) are used according to the operation regions, namely 0 9 and 0 3 The load parameters are selected intentionally considering induction motor and the load power factor is 0.7.

Fig. 13 and Fig. 14 are the cases in which the conventional PWM scheme and the proposed PWM one are used for four-level operation region, respectively. Fig 13(a) and 14(a) show the same line-to-line voltage and load current Fig 13(b) and 14(b) are the PWM schemes to obtain gate pulses of phase A The conventional method uses three triangular waves with the same amplitude and phase but with different position as carrier waves

However, the proposed method selects one among the new carriers given in Fig 7 according to the amplitude of the reference voltage and two rules. The carrier waves in Fig 14(b) are represented by the summation of proposed carrier waves and 0, 200, 400 to distinguish one another, respectively. Fig. 13(c) and 14(c) are the consequent gate pulses. There is a difference of switching number

In the proposed method, the switches have the same switching frequency but in the conventional one $S_{a1}$ and $S_{a3}$ have more switching frequency than $S_{a2}$ , in other word more switching loss. Fig. 13(d) and 14(d) are the rms currents of the switches. In the proposed method, those have the same value

But in the conventional method the rms current of $S_{a3}$ is larger than that of $S_{a2}$ This leads to more conduction loss in $S_{a3}$ Therefore, the proposed method is very efficient in the side of switch utilization. Fig. 15 and Fig 16 are the cases of two-level region operation

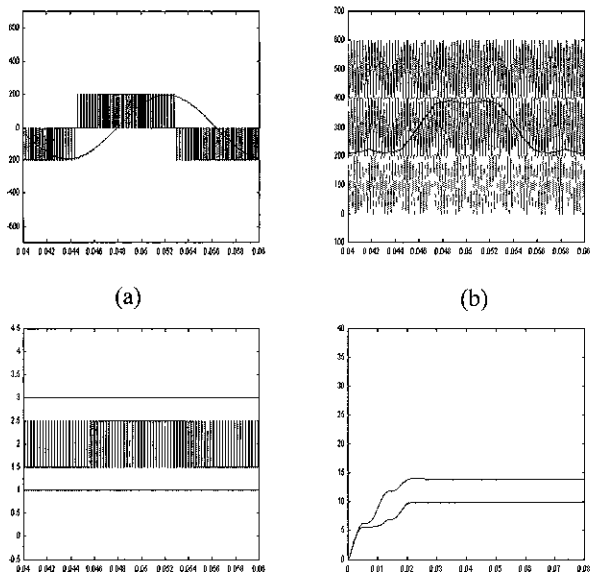

Fig 15 Simulation results for **two-level region operation** by the **conventional** PWM method (a) $I_a$ ×10 and $V_{ab}$ (b) PWM scheme reference voltage for phase A and carrierwaves for $S_{a1}$, $S_{a2}$, $S_{a3}$ (c) gate pulses for $S_{a1}$, $S_{a2}$, $S_{a3}$ from top (d) rms currents for $S_{a3}$, $S_{a2}$ from top and zero current for $S_{a1}$

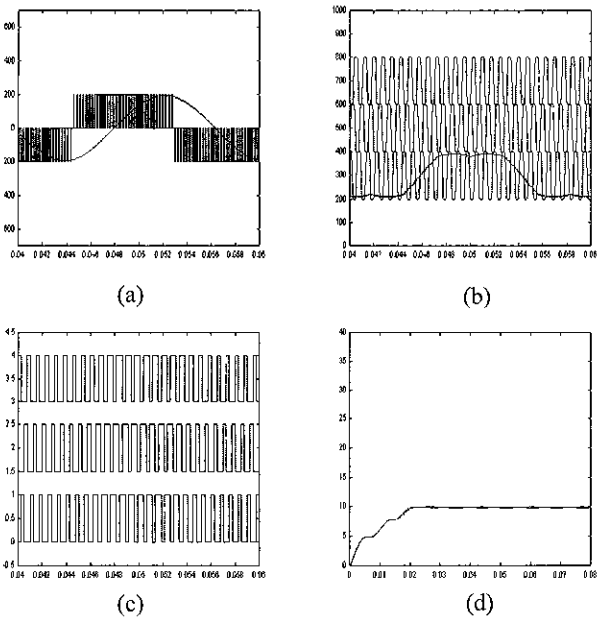

Fig 16 Simulation results in **two-level region operation** by the **proposed** PWM method (a) $I_a$ ×10 and $V_{ab}$ (b) PWM scheme reference voltage for phase A and bottom-carrierwave for $S_{a1}$, middle- 200+carrierwave for $S_{a2}$, top-400+carrier - wave for $S_{a3}$ (c) gate pulses for $S_{a1}$, $S_{a2}$, $S_{a3}$ from top (d) the same rms currents for $S_{a1}$, $S_{a2}$, $S_{a3}$

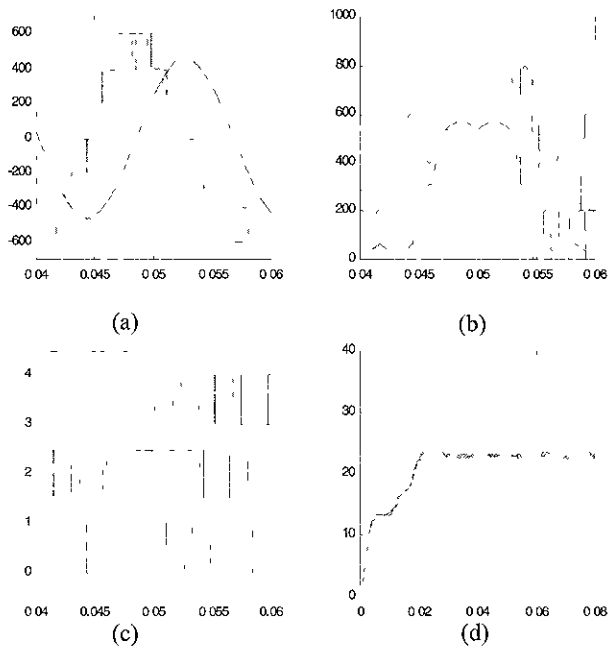

Fig 17 Simulation results when the load power factor was changed to 0 547 by the proposed PWM method (a) $I_a$ ×10 and $V_{ab}$ (b) PWM scheme reference voltage for phase A and bottom-carrierwave for $S_{a1}$, middle- 200+carrierwave for $S_{a2}$, top- 400+carrierwave for $S_{a3}$ (c) gate pulses for $S_{a1}$, $S_{a2}$, $S_{a3}$ from top (d) the same rms currents for $S_{a1}$, $S_{a2}$, $S_{a3}$

These also have the same results previously mentioned Consequently the optimized switch utilization could be acquired regardless of the variation in the modulation index.

Fig 17 shows the results when other load values are used in order to examine the effect on the variation of the load power factor. Load inductance per phase is changed to 15$mH$ and other conditions are equal to ones in Fig 14 This shows that the rms currents of the switches have the same values at other load power factor

The experiment is performed through the three phase four-level cascaded inverter with 2$HP$-induction motor The experimental conditions are as follows, capacitance per unit-5000$\mu F$, output frequency-50$Hz$, total DC link voltage-150$V$, sampling time-125$\mu s$. Two modulation indices are used according to the operation regions, namely 0 9 and 0 3

Fig 18 shows the experiment results for four-level region operation by the proposed method. Fig. 18(a)

shows line-to-line voltage ($V_{ab}$), 18(b) leg voltage ($V_{an}$), 18(c) gate pulses ($G_{a1}$ , $G_{a2}$ , $G_{a3}$), 18(d) load current ($I_a$) and 18(e) rms currents ($I_{Sa1,rms}$, $I_{Sa2,rms}$, $I_{Sa3,rms}$) The rms value is calculated through root mean square of positive current multiplied by normalized gate pulse for a period Fig. 18(c) and 18(e) represent that all the switches have the same switching frequency and the same rms current

Fig. 19 shows experiment results for two-level region operation by the proposed method The figures show the optimized switch utilization regardless of modulation indices

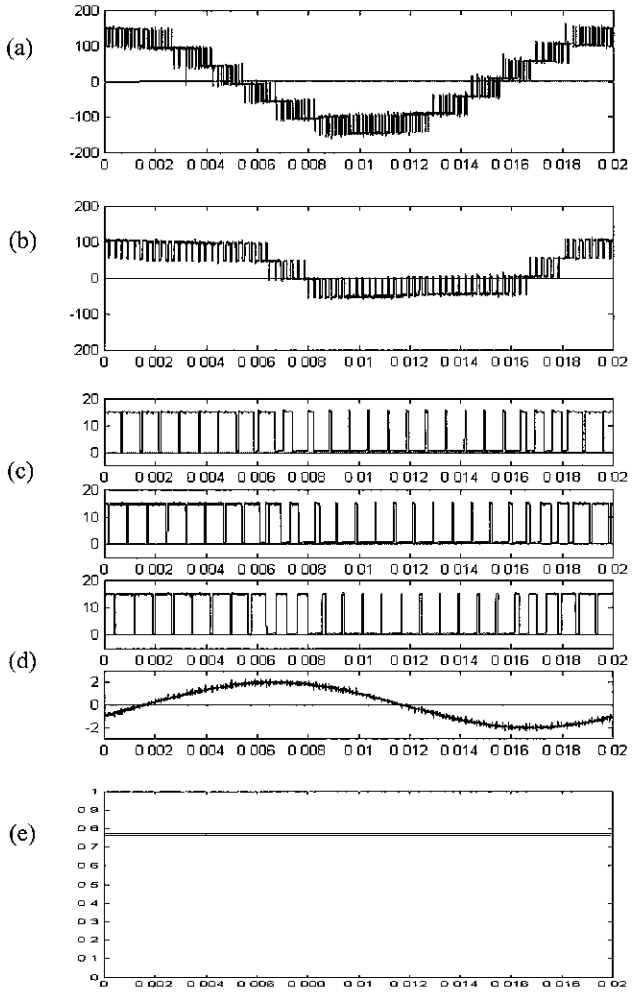


Fig 18 Experiment results for four-level region operation of four-level inverter by the proposed PWM method (a) line-to-line voltage-$V_{ab}(V)$ (b) leg voltage-$V_{an}(V)$ (c) gate pulses$(V)$ for $S_{a1}$, $S_{a2}$, $S_{a3}$ from top (d) load current-$I_a(A)$ (e) the rms currents$(A)$ for $S_{a1}$ , $S_{a2}$ , $S_{a3}$

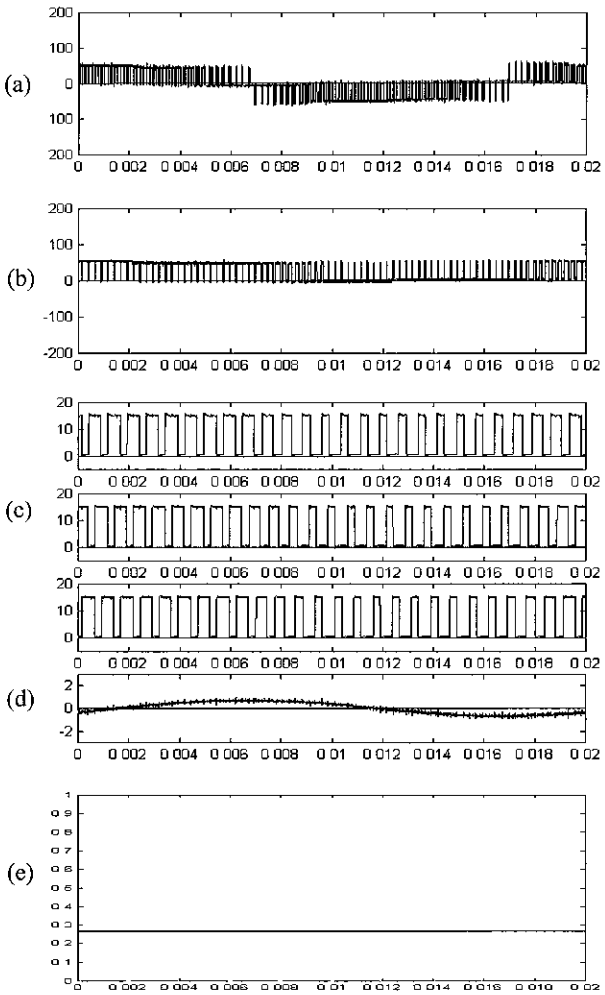


Fig 19 Experiment results for two-level region operation of four-level inverter by the proposed PWM method (a) line-to-line voltage-$V_{ab}(V)$ (b) leg voltage-$V_{an}(V)$ (c) gate pulses$(V)$ for $S_{a1}$, $S_{a2}$, $S_{a3}$ from top (d) load current-$I_a(A)$ (e) the rms currents$(A)$ for $S_{a1}$ , $S_{a2}$ , $S_{a3}$

## 5. Conclusions

This paper proposed an improved carrier-based SVPWM method The method uses leg voltage redundancies of cascaded multilevel inverter and the triangular waves are redistributed by two rules to get new carriers. The proposed method makes the utilization of switches equal. It leads to decrease of maximum power loss in a unit that multilevel structure may have and it can increase the maximum switching frequency until the devices are not destroyed Since it has the same switching and conduction loss, it is also profitable for the design of

heat sink. It can be applied easily to higher level through the generalization process. So the method would be suitable to cascaded multilevel inverter. The main advantage of the method is the optimized utilization of all the switches at both high and low modulation indices even if the load power factor varies.

## References


[1] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Applicat.*, vol. 17, no. 5, pp. 518~523, Sept./ Oct. 1981.

[2] J. S. Lai and F. Z. Peng, "Multilevel Converters - A New Breed of Power Converters," *IEEE Trans. Ind. Applicat.*, vol. 32, no. 3, pp. 509~517, May/Jun. 1995.

[3] J. K. Steinke, " Switching Frequency Optimal PWM Control of a Three-Level Inverter," *IEEE Tran. Power Electron.*, vol. 7, no. 3, pp. 487~496, July 1992.

[4] Y. H. Lee, B. S. Suh, and D. S. Hyun, "A Novel PWM Scheme for a Three-level Voltage Source Inverter with GTO Thyristors," *IEEE Trans. Ind. Applicat.*, vol. 32, no. 2, pp. 260~268, Mar./Apr. 1996.

[5] Y. H. Lee, R. Y. Kim, and D. S. Hyun, "A Novel SVPWM Strategy Considering DC-link Balancing for a Multi-level Voltage Source Inverter," *in APEC'99,* pp. 509~514.

[6] F. Z. Peng, J. S. Lai, J. McKeever and J.VanCoevering, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation," *IEEE Trans. Ind. Applicat.,* vol. 32, no. 5, pp. 1130~1138, Sept./Oct. 1996.

[7] F. Huang, P. I. Lim and E. K. Goh, "Design and Implementation of a 3-Phase Voltage Stabilizer Using 11-Level Voltage Source Inverter," *in IECON'97,* pp. 722-725.

[8] G. Joos, X. Huang and B. T. Ooi, "Direct-coupled Multilevel Cascaded Series VAR Compensators," *IEEE Trans. Ind. Applicat.,* vol. 34, no. 5, pp. 1156-1163, Sept./Oct. 1998.

[9] F. Z. Peng, J. W. McKeever and D. J. Adams, "A Power Line Conditioner Using Cascade Multilevel Inverters for Distribution Systems," *IEEE Trans. Ind. Applicat.,* vol. 34, no. 6, pp. 1293 ~1298, Nov./Dec. 1998.

[10] M. Marchesoni, "High-Performance Current Control Techniques for Applications to Multilevel High-Power Voltage Source Inverters," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 189~204, Jan. 1992.

[11] L. M. Tolbert and F. Z. Peng, "Multilevel Converters for Large Electric Drives," *IEEE Trans. Ind. Applicat.*, vol. 35, no. 1, pp. 36~44, Jan./Feb. 1999.

[12] L. M. Tolbert, F. Z. Peng and T. G. Habetler, "Multilevel PWM Methods at Low Modulation Indices," *IEEE Trans. Power Electron.,* vol. 15, no. 4, pp. 719~725, July 2000.

[13] D. W. Kang, Y. H. Lee, B. S. Suh, C. H. Choi and D. S. Hyun, "A Carrierwave-Based SVPWM Using Phase-Voltage Redundancies for the Multilevel H-bridge Inverter," *in IECON'99*, pp. 324~329.

[14] B. S. Suh, Y. H. Lee, D. S. Hyun and Thomas A. Lipo, "A New Multilevel Inverter Topology with a Hybrid Approach," *in Proc. EPE'99*, paper no. 102.


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