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Performance Analysis of SSSC with Switching-level Simulation Model and Scaled Hardware Model

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ABSTRACT

This paper describes a switching-level simulation model and scaled hardware model for SSSC, which is useful for analyzing the dynamic interaction between the SSSC and the power transmission system. A detailed simulation model with EMTP was developed to verify the SSSC operation with control system, and its increasing capability of power transmission through the line for a typical one-machine infinite-bus system. The simulation results of the developed model are compared with the experimental results from a scaled model of 2kVA rating for evaluating the whole system operation

Key Words · SSSC(synchronous static series compensator), EMTP(electro-magnetic transients program), TACS (transient analysis of control systems), Voltage Source Inverter, PWM(pulse width modulation), Scaled-model

1.Introduction

The increasing method for power transmission capability by compensating the voltage drop in the long line with series capacitor was proposed in the early days of ac power transmission However, its application for the actual system has been restricted due to the problems of reducing the transient stability and occurring the low-frequency oscillation by compensating fixed value of capacitance in series

Kimbark[1] proposes a compensator composed of series capacitors connected in parallel with mechanical switches This system can change the amount of series compensation by opening the mechanical switches in stair manner. Vithayathil[2] proposes a compensator, which is exactly same as the static var compensator, but connected in series with the line.

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This system regulates the line reactance by changing the conduction angle of the thyristor-controlled reactor.

Several modules connected in series, which is called the thyristor controlled series compensator[3], is under the commercializing test Gyugyi[4] proposes the SSSC, which consists of a voltage source inverter with dc capacitor to inject an ac voltage with 90° phase shift to the line current. The SSSC can be operated in capacitive or inductive mode by injecting a controllable ac voltage independent of the line current magnitude

The simulation model for SSSC with EMTP was already published by Sen[5] However, this model uses a TACS emulated voltage source for SSSC, instead of a switching-level voltage source inverter In this paper a switching-level simulation model will be described to verify the SSSC operation with control system And its increasing capability of power transmission through the line for a typical one-machine infinite-bus system will be investigate The simulation results of the developed model are also compared with the experimental results from a scaled model of 2kVA rating for evaluating the whole system operation

2. Operation Concept

The SSSC generates and injects in series with the line a balanced 3-phase voltage perpendicular to the line current, whose magnitude and phase can be adjusted rapidly by using semiconductor switches The SSSC is composed of a voltage-source inverter with a dc capacitor, coupling transformer, and control circuit as shown in Fig 1

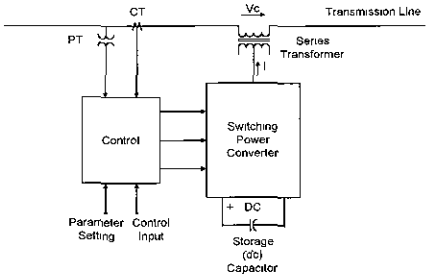


Fig 1 SSSC configuration

The output voltage of SSSC can be controlled changing the firing angle If the output voltage is lagging the line current by 90°, it supplies a capacitive reactive-power to reduce the line reactance If leading the line current, it supplies an inductive reactive-power to increase the line reactance.

The angle between the injection voltage V_C and the line current I_L in the actual system is larger than 90° to cover the losses at the inverter and the coupling transformer The inverter operates in multi-pulse mode to reduce the harmonic level of the output voltage.

The dc capacitor is required to maintain energy balance between the ac and dc terminal so that it can draw or supply the required reactive power The voltage across the dc capacitor is controlled absorbing or releasing the active power from or to the ac network.

3. Operation Analysis

The operation of SSSC can be explained using a simple equivalent circuit shown in Fig. 2. The SSSC is modeled with an ac voltage source whose output voltage has 90° phase lead or lag to the line current. The SSSC is able to emulate a compensation of the line reactance by injecting an ac voltage whose magnitude and direction can be controlled

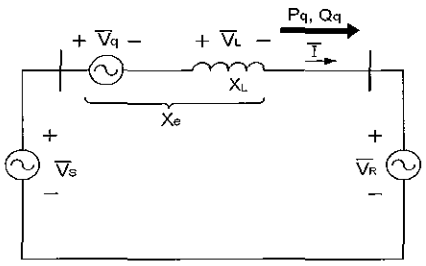


Fig 2 Two machine power system with SSSC

The effective line reactance X_e between two ends is the difference between the line reactance X_L and the compensating reactance X_q

$$X_e = X_L - X_q \tag{1}$$

The active and reactive power flow is expressed by the following equations

$$P_q = \frac{V_S V_r}{X_e} \sin\delta = \frac{V^2}{X_L(1 - X_q / X_L)} \sin\delta \tag{2}$$

$$Q_q = \frac{V_S V_r}{X_e}(1 - \cos\delta) = \frac{V^2}{X_L(1 - X_q / X_L)}(1 - \cos\delta) \tag{3}$$

The compensating reactance X_q is defined to be negative when the SSSC operates in inductive mode, and positive when the SSSC operates in capacitive mode.

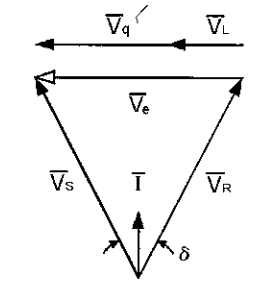
Fig 3 shows the phasor diagram when the SSSC compensates the line reactance in inductive mode and capacitive mode

The active power equation when the SSSC is connected in series with the line can be derived as the following procedures

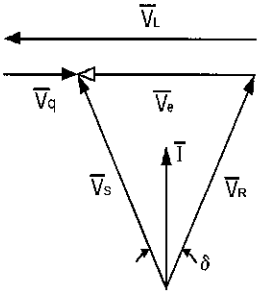
Since $X_q = V_q / I$, the active power flowing through the transmission line can be expressed by the following equation.

$$P_q = \frac{V^2}{X_L(1 - \frac{V_q}{IX_L})} \sin\delta \tag{4}$$

The active power equation when the SSSC is connected in series with the line can be derived as the following procedures



(a) L_mode copensation



(b) C_mode compensation

Fig. 3 Phasor diagram of SSSC compensation

Since $X_q = V_q / I$, the active power flowing through the transmission line can be expressed by the following equation

$$P_q = \frac{V^2}{X_L(1 - \frac{V_q}{IX_L})} \sin\delta \tag{4}$$

The voltage across the line, V_L is equal to IX_L. So, the active power can be expressed by the following equation.

$$P_q = \frac{V^2}{X_L} \sin\delta \frac{1}{(1 - \frac{V_q}{V_L})} \tag{5}$$

From the phasor diagram in Fig 3, the voltage across the line can be expressed by the following equation

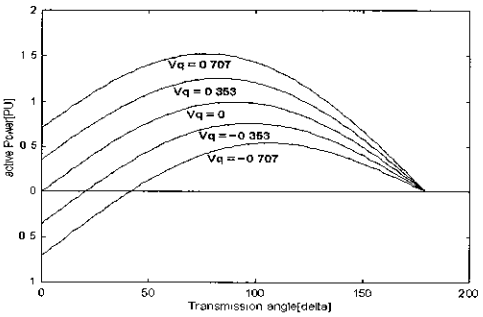
$$V_L = V_q + 2V\sin\frac{\delta}{2} \tag{6}$$

Inserting the equation (6) into the equation (5) and arranging it, the following equation can be derived

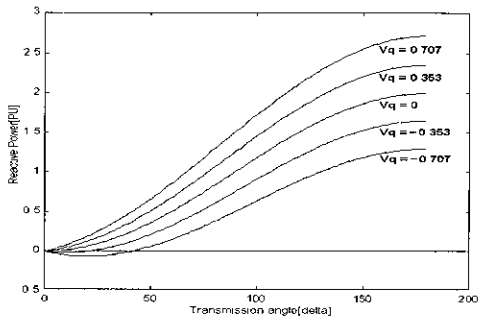
$$P_q = \frac{V^2}{X_L}\sin\delta + \frac{V}{X_L}V_q\cos(\frac{\delta}{2}) \tag{7}$$

The reactive power through transmission line can be derived by applying similar procedures as shown in equation (8).

$$Q_q = \frac{V^2}{X_L}(1 - \cos\delta) + \frac{V}{X_L}V_q\sin(\frac{\delta}{2}) \tag{8}$$



(a) Variation of P_q



(b) Variation of Q_q

Fig 4 active and reactive power flow

The active and reactive power described on the above equations can be calculated using MATLAB Fig. 4 shows the calculated results with respect to the variation of power angle It is possible to transmit active power through the line when the phase difference between the sending end and the receiving end is zero Also, the transmitted active power can be negative when the injecting voltage is inductive. If the power angle is larger than zero, the reactive power increases monotonically as the line is compensated in capacitive mode

4. EMTP Simulation

The EMTP is very effective to test the control system of SSSC and analyze the dynamic interaction between the SSSC and the ac transmission system[6]. an EMTP simulation model was developed assuming that the SSSC is connected in series with the 154kV line The main circuit of SSSC and power system is modeled with the components in the branch data and the switch data. The signal generation and control circuits are modeled with the components in the TACS.

Normally, the actual SSSC consists of a 48-pulse inverter to reduce the level of harmonics in the output voltage. However, the simulation model consists of a 12-pulse voltage source inverter with two 6-pulse bridges connected in parallel as shown in Fig. 5 so as to save the simulation time without neglecting the simulation effect. Each inverter module consists of six Type-13 switches in the EMTP to represent the GTO switches and the reverse-connected diodes in the actual system

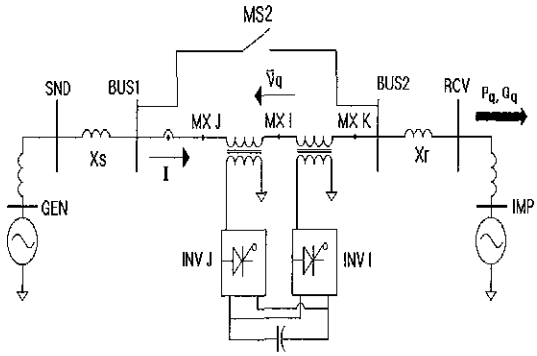
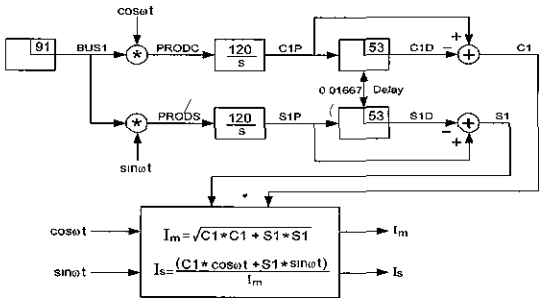


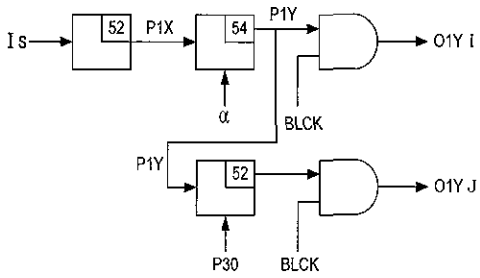
Fig 5 Network simulation model with EMTP.

4.1 Gate pulse generation

Fig. 6 shows the block diagram for current tracking and pulse generation The line current is detected and sent to the current tracking system to obtain a sinusoidal signal with unity magnitude. Its zero-crossing point is used as the reference point to generate the gate signals The sinusoidal signal is passed through the saturation amplifier for pulse generation. This pulse is delayed by the firing angle α. Two sets of gate pulses, whose phases are shifted by 30° each other, are generated and provided to the upper and lower bridges.



(a) current tracking



(b) gate pulse generation

Fig 6 Gate pulse generator with EMTP

4.2 Control circuit

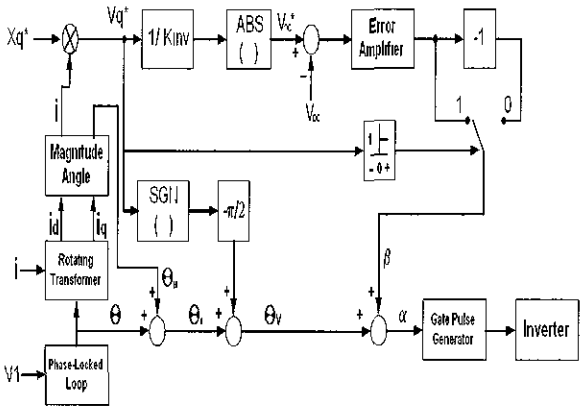


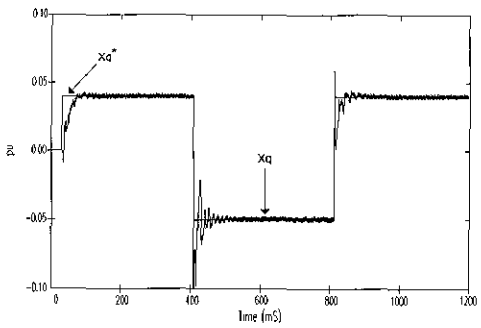
Fig 7. Control system model with EMTP

Fig 7 shows the control circuit that is modeled using the TACS. Three bus voltages at the connection point are measured for calculating phase lock angle. And three currents into the inverter are measured and converted into d and q components. The magnitude and angle are calculated using these two components. The current magnitude is multiplied by the line reactance to generate

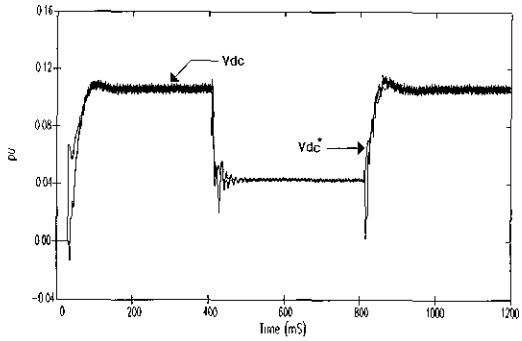
the injecting voltage reference, which is used to obtain the dc capacitor voltage reference The reference dc capacitor voltage V_{dc}^{*} is compared with the actual dc capacitor voltage to obtain the angle β through PI controller The sign of angle β is determined by the polarity of the injecting voltage V_q. Also, the polarity of V_q is used to determine the phase lead or lag of 90°, which should be added to the angle β to obtain the firing angle α.

4.3 Simulation results

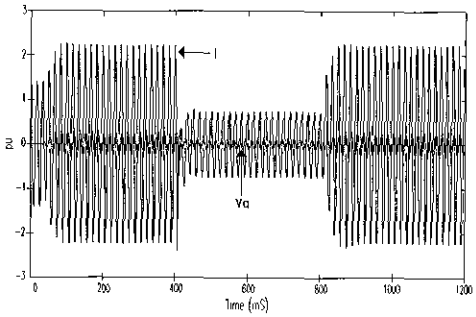
The scenario considered in the simulation is as the following There is no reference value of line reactance between 0 and 30ms because the SSSC does not inject ac voltage for this period The reference value of line reactance has 0 04pu in capacitive mode between 30 and 400ms. It suddenly changes to the inductive mode at 400ms and lasts up to 800ms with 0.05pu The reference value changes again to the capacitive mode at 800ms and lasts up to 1200ms with 0.04pu The reference value of line reactance was determined as 1 0pu for 110.55Ω.



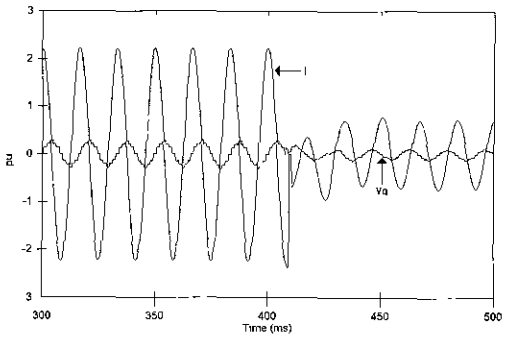
(a) reactance tracking



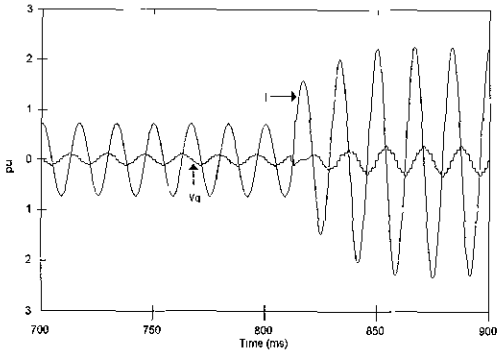
(b) capacitor voltage tracking



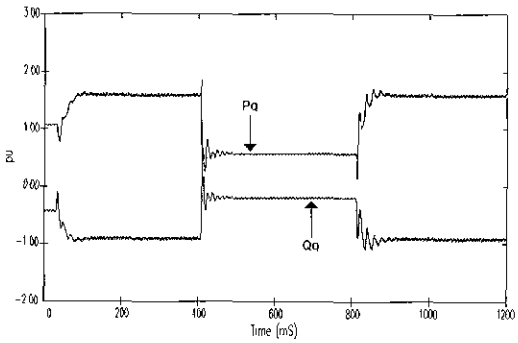
(c) line current and compensation voltage



(d) line current and compensation voltage(lead =>lag)



(e) line current and compensation voltage(lag =>lead)



(f) transmission active and reactive power

Fig 8 Simulation results

Fig 8(a) shows variation of the line reactance reference, which has same value described in the scenario Fig. 8(b) shows variation of the dc capacitor voltage, which tracks the reference value properly The capacitor voltage has 9% of overshoot at the instance changing from the capacitive to the inductive mode. The change from the inductive to the capacitive mode has damping oscillation Fig 8(c) shows variations of the series injecting voltage and the line current. The voltage and current become higher during capacitive mode and lower during inductive mode The voltage has 90° phase lead or lag to the line current in the capacitive mode or inductive mode Fig 8(d) and 8(e) show the expanded waveforms during lead to lag and lag to lead transitions. Fig 8(f) shows variation of the active and reactive power transmitted through the line The transmitted active power increases from 1.0pu to 1.6pu by compensating 107Mvar reactive power with SSSC, while the transmitted reactive power increases from 0 4pu to 1.0pu.

5. Scaled-Model Experiment

A hardware scaled-model has been built to verify the simulation results and to confirm the feasibility of actual system implementation Fig. 9 shows whole circuit diagram for the scaled model of 3ϕ/120V/2kVA rating A separate inverter was built to simulate the one-machine-infinite-bus power system. This inverter is connected to the 3-phase power source on the wall through a 3-phase line model, which was built with six reactors The SSSC model was built and connected in series with the line through the transformers

The inverter for generator model is synchronized with the supplying ac source voltage Its phase angle leads the source's phase angle to supply active power to the source. Both inverters for generator model and SSSC model are operated in PWM mode for easy implementation instead of multi-pulse mode. The switching frequency of both inverters is 3kHz to consider reduction of the output harmonics and switching losses.

An 80C196KC microprocessor system was built to generate PWM pulses for the inverters and to control the whole system operation This system contains 16-bit internal registers with 488 byte capacity. It has two timers and counters, one HSI(high speed input) for detecting input pulse width, one HSO(high speed output) for generating the output pulses with arbitrary width, 8 A/D channels, and 4 serial ports.

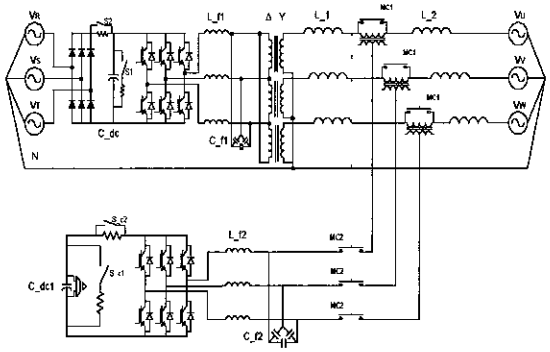
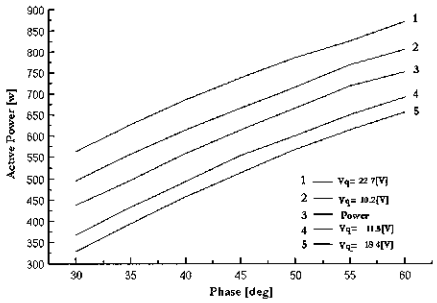
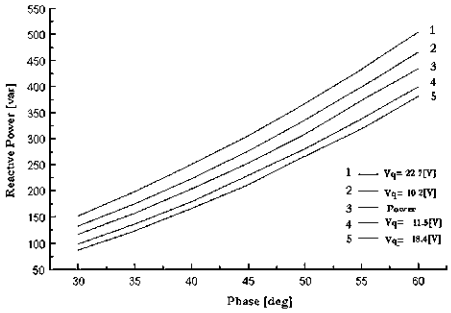


Fig 9 Scaled model circuit diagram

5.1 Steady-state analysis



(a) transmission active power



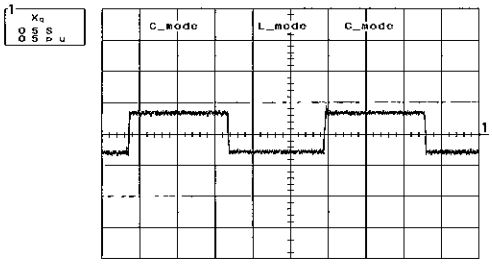
(b) transmission reactive power

Fig 10 Measured active and reactive power flow

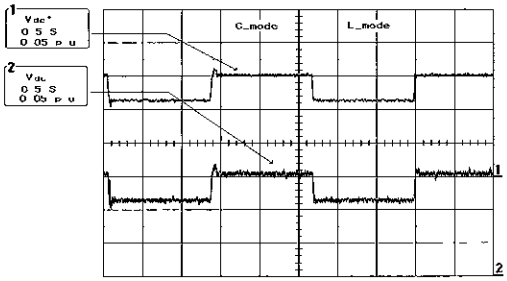
In this experiment the amount of active and reactive power through the transmission line was measured with respect to the injected voltage from the SSSC by changing the phase angle of sending-end voltage. The phase angle was increased by 5° from 30° to 60° and the injected voltage was changed regarding to four values, such as +10.2V, +22.7V, -11.5V, -18.4V. Fig. 10 shows the measured values shown as a group of graphs. Although there is some difference, it is very similar to the calculated results from the equations.

5.2 Dynamic analysis

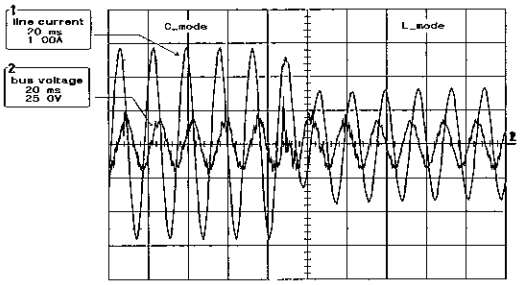
The dynamic analyses were performed to verify the simulation results Fig. 11 shows experimental results for the dynamic response of SSSC Fig. 11(a) shows the reference value of compensating reactance



(a) reference of line reactance (Xq')



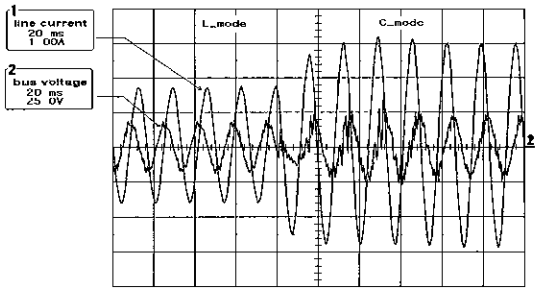
(b) Capacitor voltage and reference



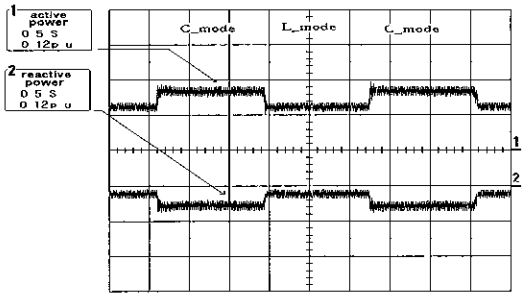
(c) injection voltage & line current (lead =>lag)

The reference value is changed from 0.34 pu in capacitive mode to 0.28 pu inductive mode. Each mode remains for 1.3 second. Fig. 11(b) shows the measured value of dc capacitor voltage in SSSC follows the reference value.

This shows that the control system of SSSC works properly to regulate the line reactance of the ac power system. Fig. 11(c) shows the bus voltage and the reactive current when the compensator supplies the lagging reactive power and then change to supply the leading reactive power The current has 90° phase lag to the bus voltage and it suddenly change to 90° phase lead with some transients Fig. 11(d) shows the bus voltage and the reactive current when the compensator supplies the leading reactive power and then change to supply lagging reactive power The current has 90° phase lead to the bus voltage and it suddenly change to 90° phase lag with some transients. Fig. 11(e) shows the active and reactive power transmitted through the transmission line. The values are obtained by measuring the sending-end voltage and the line current, and multiplying both variables after d-q transform. These values are displayed through D/A converter in the microprocessor



(d) injection voltage & line current (lad =>lead)



(e) transmitted active & reactive power

Fig 11 Experimental results

6. Conclusion

In this paper a switching-level simulation model and scaled hardware model for SSSC were described. The effectiveness of these models were verified by applying it for the one-machine-infinite-bus power system.

In the simulation model the SSSC was represented with a 12-pulse inverter, which consists of two 6-pulse modules connected in parallel. Each module is modeled with six type-13 switches in EMTP switch data to represent the GTO and the reverse-connected diode. The signal generation and control circuits are modeled with the components in the TACS. The line current is detected and passed through the synchronizing block. Its zero-crossing point is used as a reference point to generate the gate signals. Since the line current changes as the line reactance is regulated, a phase-locking procedure was considered.

A scaled hardware model for an SSSC connected in the one-machine-infinite-bus power system was built and tested to verify the simulation results. A separate inverter was built to simulate the generator in one-machine-infinite-bus power system. It is connected to the 3-phase power source on the wall through a 3-phase line model with 6 reactors. Both inverters for generator and SSSC models are operated in PWM mode, instead of multi-pulse mode for easy implementation.

Both simulation models and scaled hardware model would be very effective for evaluating the SSSC operation.

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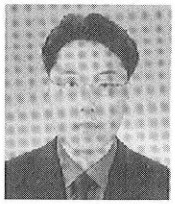

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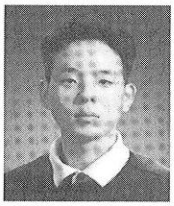

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