JPE 2-3-2

Voltage Sag Detection Algorithm for Instantaneous Voltage Sag Corrector

[1]Sanghoon Lee and [2]Jaeho Choi*

[1] POSCON Corporation, Seoul, Korea
[2] Chungbuk National University, CheongJu, Korea

ABSTRACT

Voltage sag detection algorithm for voltage sag corrector is proposed in this paper. To quantify the standard of voltage unbalance under the faulted conditions, the 3-phase unbalanced voltages are decomposed into two balanced 3-phase symmetrical components of the positive and negative sequence voltages, which is defined by the magnitude factor (*MF*) and unbalance factor (*UF*) It is analyzed that *MF* and *UF* values are given as the dc constant values even though under the voltage unbalance condition This paper also proposes the control scheme of the instantaneous voltage sag corrector based on this detection algorithm The validity of the proposed algorithm is verified through the EMTDC simulation and experiments.

Keywords· Instantaneous voltage sag corrector, Power quality, Magnitude factor, Unbalance factor

1. Introduction

The power quality problems due to a wide range of line disturbances, ranging from the voltage sags and swells to the harmonic distortions, become an important concern in the power distribution systems or the industrial power plants Among these line disturbances, the voltage sags are the most important power quality problems facing many industrial customers Voltage sag means the momentary decrease of voltage magnitude for duration of between 0 5 to 30 cycles[1][2] It is usually caused by a remote fault somewhere on the power system Customers living hundreds of miles away from the fault location can still experience the voltage sag resulting in the mal-operation of the power and control equipments when the fault is on the transmission system The large majority of the utility line faults are single line-to-ground faults (SLGF) SLGF's on the utility system is the most common cause of voltage sags in an industrial plant[3]

Voltage sags of short duration induce the fatal results to the high-technology electronic loads that are very sensitive to the deviations of the supply voltage Constant voltage transformers (CVT) or uninterruptible power supplies (UPS) are the common approach to mitigate or eliminate the voltage sag problems CVT's are easy and economic to install, but not efficient under the variable load condition or large inrush current condition UPS's are more excellent than CVT's, but these are costly, especially for larger ratings, have some frequent maintenance problems The instantaneous voltage sag correctors (IVSC) are more effective for maintaining the voltage within limits and balancing it Figure 1 shows the IVSC system using series voltage compensators Depending on the range and severity of faults to be handled, these may have ratings of

Manuscript received April 9, 2002, revised June 12, 2002.
Corresponding Author choi@power chungbuk ac kr, Tel +82-43-261-2425, Fax +82-43-276-7217

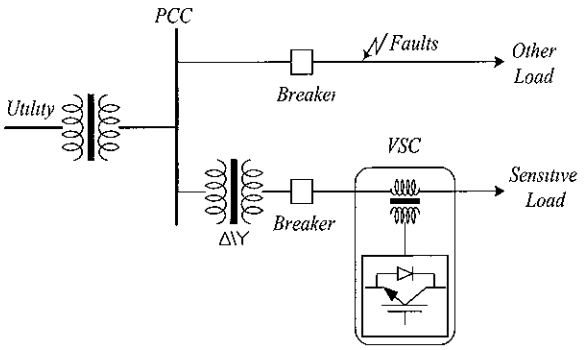


Fig 1 IVSC system in distribution line

only a fraction of the load This significantly reduces their cost comparing with the UPS solution In addition, under normal line conditions, the losses associated with the compensating operation are very small, since the injected voltage is zero and the load is supplied directly by the feeder[4][5].

Several power structures and control algorithms have appeared in the literature However, many are designed to correct small unbalances in the supply with harmonic free networks Also, they do not consider fault conditions in the distribution systems, which will more seriously affect the sags and unbalance For the application in the distribution systems, the voltage sag detection algorithm is very important, because the faulted voltage should be detected and compensated instantaneously to meet the on-line compensation The detection algorithm for faulted voltage has to meet the very short detection time and the robustness against the noise and transient change of the voltage The previous researches of faulted voltage detection method are classified as followings.

1) Averaging method
2) Single-phase relative error method
3) dq-transformation with synchronously rotating reference frame

The detection method of average value is robust against the noise and transients in the input voltage. It can detect the power source abnormality, but takes at least half period to detect the abnormality. To improve the drawbacks of the averaging method, the detection of instantaneous value has been considered using the relative ac error value But all variables described as the instantaneous ac values have time variant characteristics, so the analysis of power system and design of control variables are very complicate

If 3-phase ac values are transformed to dq-values with the synchronously rotating reference frame, the dq-values are given as the constant dc values in case of 3-phase balanced condition. Therefore, all the problems with the formal two methods can be overcome using this transformation, but it is only under the 3-phase balanced condition. Although they are transformed to dq-values, ac components are still remained under the unbalanced condition Also the control algorithm is complicated and is generated with coupling terms[8].

This paper proposes a novel detection algorithm of faulted voltages under the unbalanced condition To quantify the standard of unbalance under the fault conditions, the 3-phase unbalanced voltages are decomposed into two balanced 3-phase symmetrical components of the positive and negative sequence voltages, which is defined by the magnitude factor (*MF*) and unbalance factor (*UF*) It is analyzed that *MF* and *UF* values are given as the dc constant values even though unbalance condition This paper also proposes the control scheme of the instantaneous voltage sag corrector based on this detection algorithm.

The proposed algorithm has advantages as followings The duration time for detection is short and constant because it is not affected by the fault starting position. The control variables have time-invariant characteristics although it is under the unbalance conditions. The structure of the proposed controller is simpler than that of the previous algorithm based on the dq-transformation with the synchronously rotating reference frame

Finally the validity of the proposed algorithm is verified through the simulation and experiment. The simulation is accomplished by PSCAD/EMTDC and the prototype experimental system is implemented by using the digital signal processor (TMS320C31).

2. Detection of *MF* and *UF*

Instantaneous voltage sags are generally caused by the faults of short circuits on the distribution line Most faults are generated from the natural phenomenon such as lightning, weather condition, tree branch or animal contact, and insulation failures or human activity

All faults except three line-to-ground fault (TLGF) have 3 phase unbalanced and unsymmetrical condition. *MF* and *UF* are defined as shown (1)

$$|MF| = \frac{V_P}{V_{ref}} \tag{1a}$$

$$|UF| = \frac{V_N}{V_P} \tag{1b}$$

where, V_P is the positive sequence component, V_N is the negative sequence component and V_{ref} is the normal voltage before faults

The phase and line-to-line voltage of source is defined by (2) and (3) with the line voltage value, V to get the symmetrical components

$$v_{sa}(t) = \frac{V}{\sqrt{3}}\cos(wt + \theta_a) \tag{2a}$$

$$v_{sb}(t) = \frac{V}{\sqrt{3}}\cos(wt - \frac{2\pi}{3} + \theta_b) \tag{2b}$$

$$v_{sc}(t) = \frac{V}{\sqrt{3}}\cos(wt + \frac{2\pi}{3} + \theta_c) \tag{2c}$$

$$v_{s,ab}(t) = V\cos(wt + \frac{\pi}{6} + \theta_a) \tag{3a}$$

$$v_{s,bc}(t) = V\cos(wt - \frac{\pi}{2} + \theta_b) \tag{3b}$$

$$v_{s,ca}(t) = V\cos(wt + \frac{5\pi}{6} + \theta_c) \tag{3c}$$

To calculate *MF* and *UF* defined by (1), the symmetrical components should be calculated with the line voltage as shown by (4)

$$\begin{bmatrix} v_{s,abP} \\ v_{s,abN} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix}\begin{bmatrix} v_{s,ab} \\ v_{s,bc} \\ v_{s,ca} \end{bmatrix} \tag{4}$$

where, $\alpha = e^{J\frac{2\pi}{3}}$

As an example of faults, SLGF is considered as followings: If SLGF is happened in a-phase, the phase voltage of 'a' will be zero, and the line-to-line voltages of (3) will be given to (5)

$$v_{s,ab}(t) = -\frac{V}{\sqrt{3}}\cos(wt - \frac{2\pi}{3} + \theta_b) \tag{5a}$$

$$v_{s,bc}(t) = V\cos(wt - \frac{\pi}{2} + \theta_b) \tag{5b}$$

$$v_{s,ca}(t) = \frac{V}{\sqrt{3}}\cos(wt + \frac{2\pi}{3} + \theta_c) \tag{5c}$$

Equation (5) shows that $v_{s,bc}$ is same regardless of faults but the magnitudes of the other two decrease to 58[%] and the phase is shifted ±30[°] By substituting (5) to (4), we can get the symmetrical components as shown in (6)

$$\begin{bmatrix} v_{s,abP} \\ v_{s,bcP} \\ v_{s,caP} \end{bmatrix} = T_P \quad v_{s,abP} = \frac{2V}{3}\begin{bmatrix} \cos(\omega t + \frac{\pi}{6} + \theta) \\ \cos(\omega t - \frac{\pi}{2} + \theta) \\ \cos(\omega t + \frac{5\pi}{6} + \theta) \end{bmatrix} \tag{6a}$$

$$\begin{bmatrix} v_{s,abN} \\ v_{s,bcN} \\ v_{s,caN} \end{bmatrix} = T_N \quad v_{s,abN} = \frac{V}{3}\begin{bmatrix} \cos(\omega t + \frac{5\pi}{6} + \theta) \\ \cos(\omega t - \frac{\pi}{2} + \theta) \\ \cos(\omega t + \frac{\pi}{6} + \theta) \end{bmatrix} \tag{6b}$$

where, $T_P = \begin{bmatrix} 1 & \alpha^2 & \alpha \end{bmatrix}^T$ and $T_N = \begin{bmatrix} 1 & \alpha & \alpha^2 \end{bmatrix}^T$.

By comparing (6) with (3), it is known that the magnitudes of positive sequence component decrease to 66.7[%] and their phase are same And the magnitudes of negative sequence component decrease to 33.3[%] and the phase sequence is opposite to that in the positive sequence while the phase of $v_{s,bc}$ is same as that of the normal voltage. Therefore, *MF* for 3 line voltages is dc value of 0 667 and only *UF* for bc line voltage is dc value of 0 5 Table I shows the magnitude of *MF* and *UF* values for some kinds of faults. If the fault impedance is zero, *MF* and *UF* have the time invariant characteristics as shown in Table 1

Table 1 *MF* and *UF* under faults

	SLGF	LLF	DLGF	TLGF
MF	0.667	0.5	0.333	0
UF	0.5	-1	-1	0

3. Detection Algorithm

As shown in Fig 1, the purpose of IVSC system is to protect the sensitive load against the instantaneous voltage sag caused by the distribution line fault So IVSC system has the capability of real time compensation and its power failure detection algorithm should be designed to suitable for real time control

The detection algorithm is very important for the operation of IVSC system, because this works not only to detect the faulted voltage but also to determine the operating point of the system In case of the detection algorithm which is implemented at existing synchronous coordinator, the fault-starting-point affects the total detecting time because the algorithm has a time variant characteristic under three phase unbalanced condition As a result, the system may not be real time compensation. In this paper, to overcome the above disadvantage a new detection algorithm based on the *MF* as described in chapter 2 is proposed

Fig 2(a) shows an overall block diagram of the fault voltage detection part and it is detailed in Fig. 2(b) A basic digital filter is used to get the robust characteristics against the noise included in the feedback signal and the transients of source But the phase delay problem is evitable with this filter and it affects adversely the performance of the instantaneous detection and control algorithm.

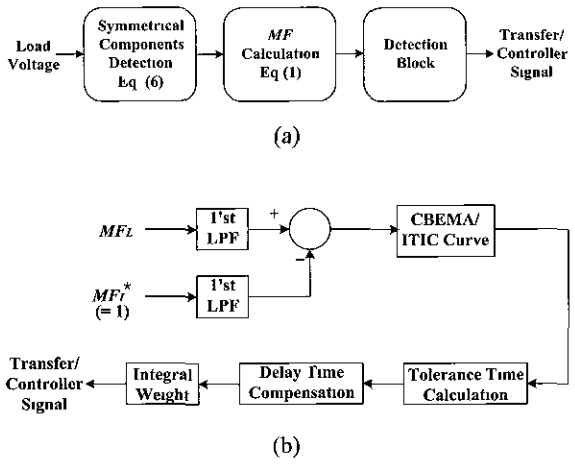


Fig 2 Proposed detection algorithm (a) Overall block diagram (b) Detailed scheme of detection block in (a)

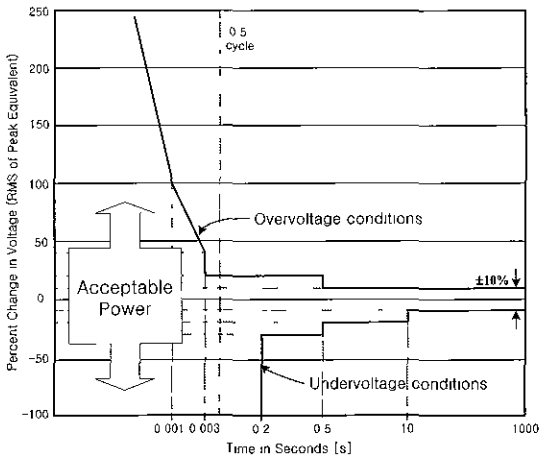


Fig 3 ITIC vurve

The ITIC (Information Technology Industry Council) curve in Fig 3 is used as the standards of power state So the switch transfer and the compensation action would be carried out under the toleration time[6]

The proposed detection algorithm has many advantages for the previous that First, it is available to a fast and precise detection regardless of the point when fault begins. It is means that the *MF* is represented as a DC value for the various faults. Second, the control algorithm, which is implemented by the proposed detection algorithm, has a time invariant characteristic, so the design and structure is very simple

4. Control Algorithm

The general requirements for IVSC system are as followings; fast dynamic response, robustness for noise, and isolation from harmonics In this paper, the last requirement is not considered The configuration of power circuit and the proposed control block diagram are shown in Fig 4 and Fig 5 Under the fault condition, the controller operates to keep the load voltage constant. Otherwise, the controller doesn't work but only the dc capacitor is charged from the source.

As shown in Fig 5, this paper proposes the novel control algorithm for IVSC system based on the proposed detection algorithm In these figures, the subscript S, L and C mean the source, load, and the compensator.

So, using IP controller, the *MF* and *UF* of compensation voltage is controlled Consequently the basic control structure is the instantaneous control of the inverter output

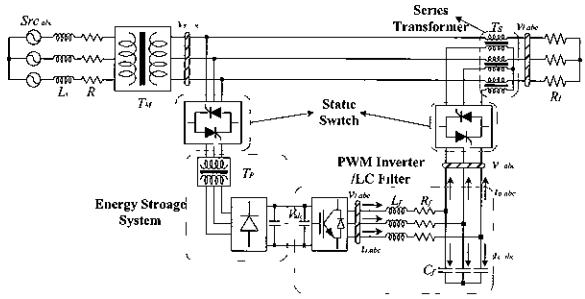


Fig 4 Configuration of power circuit for IVSC

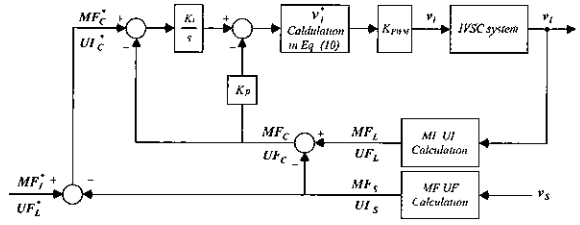


Fig 5 Proposed control algorithm

capacitor voltage For the purpose of dynamic characteristic improvement of controller, the inner current control loop of inductor could be added, but in this paper did not use it

One of the important things for the voltage compensation is how to determine the reference value of the compensator output voltage calculated by the following steps from Fig. 4 and Fig 5 In Fig. 4, the reference value of the compensator output voltage is described to be able to compensate the voltage difference between the reference load voltage and the faulted source voltage as followings

$$\left[v^{*}_{c,abc}\right] = \frac{1}{K_T}\left\{\left[v^{*}_{l,abc}\right]-\left[v_{s,abc}\right]\right\} \tag{7}$$

where, $[v_{abc}]=[v_{ab}\ \ v_{bc}\ \ v_{ca}]^T$ and K_T is the winding ratio of the series transformer

And also, the positive and negative sequence components of the reference inverter voltage are given by (8)

$$\left[v^{*}_{c,abc}\right]_P = \frac{T_P}{K_T}\left\{\left[v^{*}_{la,P}\right]-\left[v_{sa,P}\right]\right\} \tag{8a}$$

$$\left[v^{*}_{c,abc}\right]_N = \frac{T_P}{K_T}\left\{\left[v^{*}_{la,N}\right]-\left[v_{sa,N}\right]\right\} \tag{8b}$$

For the control of the voltage sag compensation under the unbalance and unsymmetrical power condition, the ideal values of the positive and negative sequence components of the load voltage is given by the reference voltage value, v_{ref}, and zero, respectively. By substituting these values in (8), the reference values of the positive and negative sequence components of the compensator output voltage are given as followings

$$\left[v^{*}_{c,abc}\right]_P = \frac{T_P}{K_T}\left(1-\frac{v_{sa,P}}{v_{ref}}\right)v_{ref} \tag{9a}$$

$$\left[v^{*}_{c,abc}\right]_N = -\frac{T_P}{K_T}\frac{v_{sa,N}}{v_{ref}}v_{ref} \tag{9b}$$

Then, by substituting (1) into (8) the compensator output voltage is described simply by (10)

$$\left[v^{*}_{c,abc}\right]_P = \frac{T_P}{K_T}(1-MF_S)v_{ref} \tag{10a}$$

$$\left[v^{*}_{c,abc}\right]_N = -\frac{T_P}{K_T}MF_S\ UF_S\ v_{ref} \tag{10b}$$

If we ignore the voltage drop at R_f, the reference voltage of inverter output will be the same value of the compensator output v_c^* and can be written as (11)

$$\left[v^{*}_{i,abc}\right] = K_{PWM}\left\{\left[v^{*}_{c,abc}\right]_P+\left[v^{*}_{c,abc}\right]_N\right\} \tag{11}$$

5. Simulation and Experimental Results

To verify the validity of the proposed algorithm, the simulation and experimental results are given as followings. The simulation is accomplished by PSCAD/EMTDC using the parameters given in Table 2 All the variables are shown as per unit values and the voltage values in Table 2 are peak value of phase voltage

Table 2 Simulation parameters

Parameter	Value	Parameter	Value
Power rating	10[kVA]	Switching frequency	5[kHz]
Voltage	311[V]	Faults duration	60[ms]
Current	37 1[A]	Winding ratio (T_S)	1 1

The voltage ratio of main transformer, T_M in Fig 4 is 22.9 kV/220 V and it is connected by Δ/Y. The winding ratios of the series and parallel transformers, T_S to T_P in Fig. 4 are 1·1 and the primary side of series transformer is connected by Δ. IGBTs (Insulated Gate Bipolar Transistor) are used as the switching devices of the inverter and the triangular wave comparison method is used as the PWM (Pulse Width Modulation) technique. And the dc capacitor value is designed through the design process proposed in [7]

Table 3 shows the parameters for the experiments. By using the TMS320C31 DSP, it is simplified to establish the control hardware and software To generate the unbalanced and unsymmetrical power condition, the ELGA SW 5250A three-phase ac power supply is used. The power rating of the prototype experimental system is limited by 1kVA with considering the rating of power supply.

In Figs 6 and 7, it is verified through the simulation and experimental results that the proposed detection algorithm can be applied to ITIC curve or not. It is shown in these figures how the delay time algorithm doesn't generate the control signal just after 0 2 sec caused by the time delay of the detection algorithm.

Table 3 Experimental parameters

Parameter	Value	Parameter	Value
Power rating	1[kVA]	Switching frequency	5[kHz]
Voltage	200[V]	Faults duration	60[ms]
Current	2 88[A]	Winding ratio (T_S)	1 1

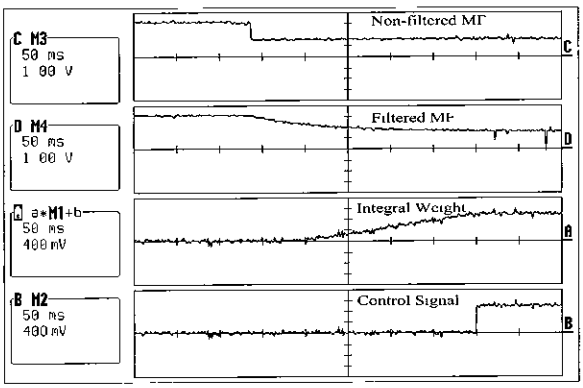


Fig 6 Experimental results for faulted voltage detection algorithm without compensation of delay time

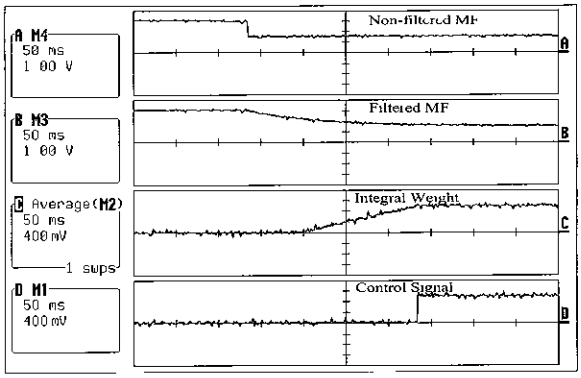


Fig 7 Experimental results for faulted voltage detection algorithm with compensation of delay time

There is 0.06 sec time delay. To overcome this problem, the delay time compensator is added to the detection algorithm and it is well verified in Fig 7 that the control signal is generated just after 0.2 sec without any time delay

Figures 8 and 9 show the simulation results of the proposed instantaneous voltage compensator as an example of SLGF accident and LLF accident. And Figs 10 and 11 show the experimental results as an example of same accidents

Figures 8 and 9 show the primary and secondary voltage of main transformer, compensator output voltage, load voltage, and DC voltage of the compensator from top to bottom and Figs 8(b) and 10(b) show *MF* and *UF* values of the source voltage at the secondary of the main transformer.

Each figure in Fig. 10(a) to (c) and Fig. 11(a) to (c) shows the voltage waveforms of source, compensator, and load, respectively Figures 10(d) and 11(d) show the *MF* and *UF* values of source voltage and load from top to bottom

As shown in Fig 8 to Fig. 11, the load voltages are well compensated under the both fault conditions of SLGF and LLF. Figures 8 and 10 show that the *MF* and *UF* values of the load voltage maintain 1 and 0 with the voltage compensation although those of the source voltage become 0 667 and 0 5 under the SLGF condition. While under the LLF condition as shown in Figs. 9 and 11, the *MF* and *UF* values of the load voltage maintain 1 and 0 with the voltage compensation under the LLF condition. From the simulation and experimental results, it is verified that the

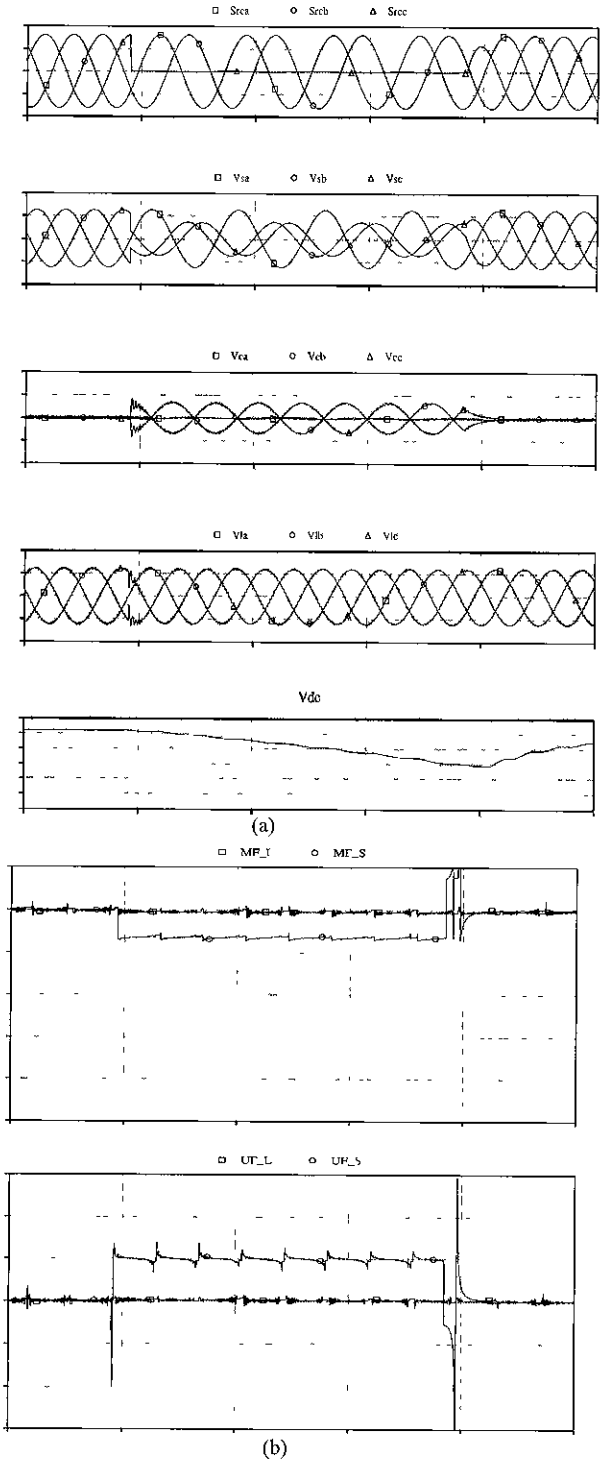


Fig 8 Simulated results under SLGF condition (a) Transformer primary voltages, transformer secondary voltages, compensation voltages, load voltages and DC voltage (b) *MF* and *UF* values of load and source voltage (from top to bottom)

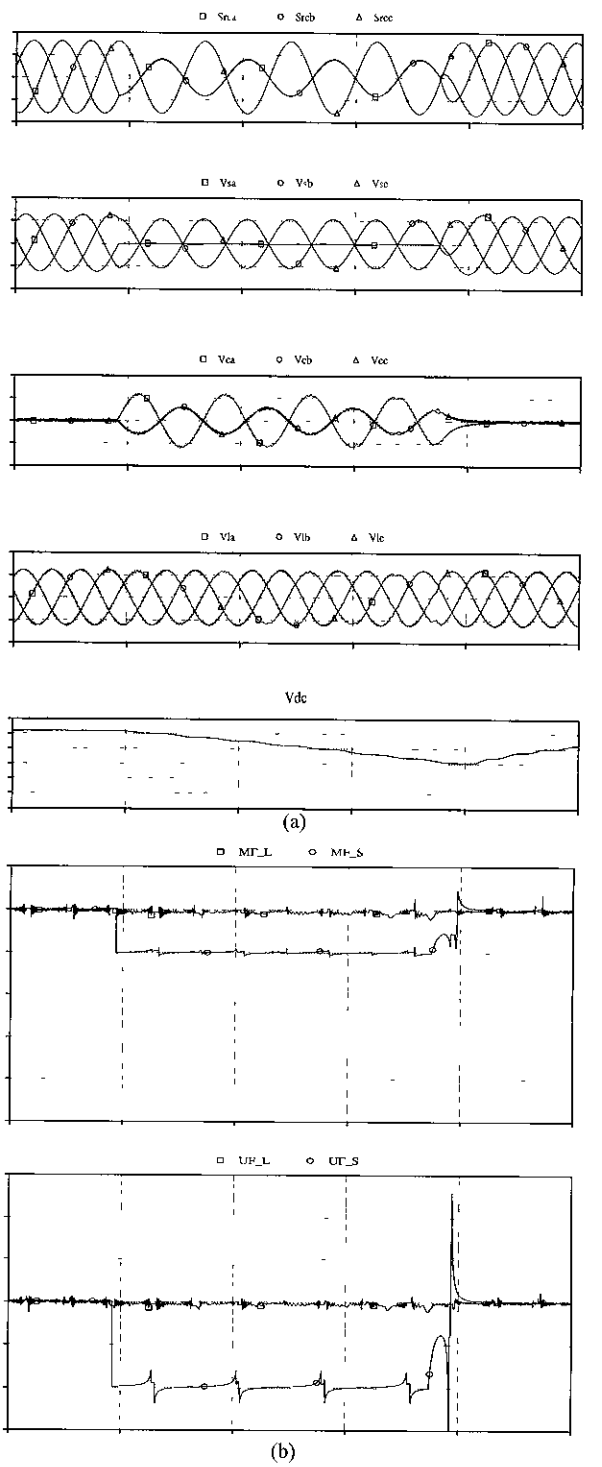


Fig 9 Simulated results under LLF condition (a) Transformer primary voltages, transformer secondary voltages, compensation voltages, load voltages and DC voltage (b) *MF* and *UF* values of load and source voltage (from top to bottom)

MF and *UF* values are regulated by the voltage compensation under the line fault condition And also, we know that this compensator works instantaneously as soon as the faults are detected.

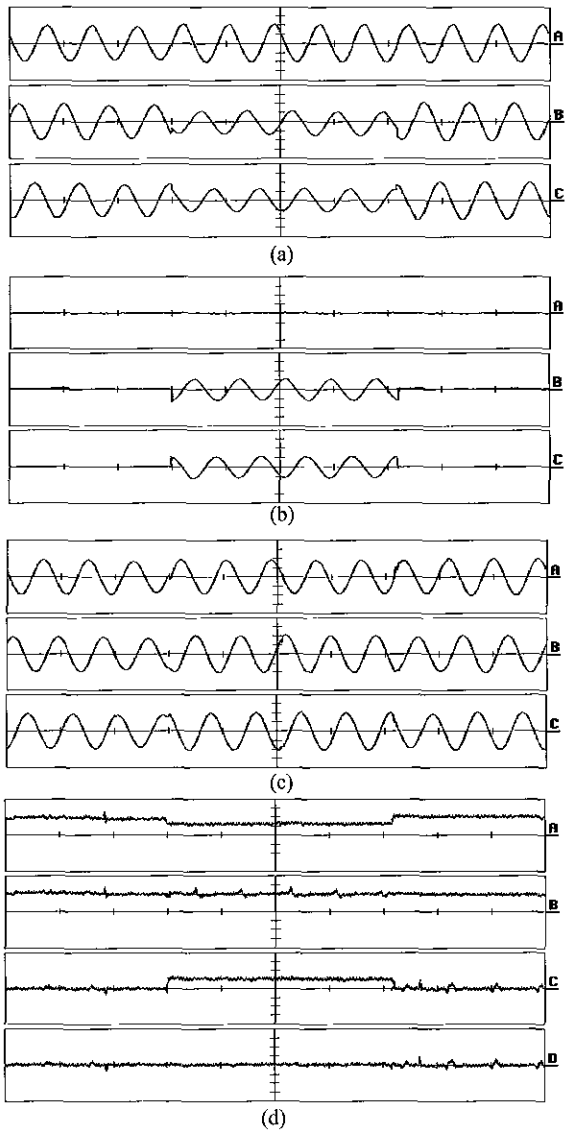


Fig 10 Experimental result under SLGF condition (a) Source voltages (100V/div) (b) Compensation voltages (50V/div) (c) Load voltages (100V/div). (d) *MF* of source voltage / *MF* of load voltage / *UF* of source voltage values / *UF* of load voltage (0 5/div)

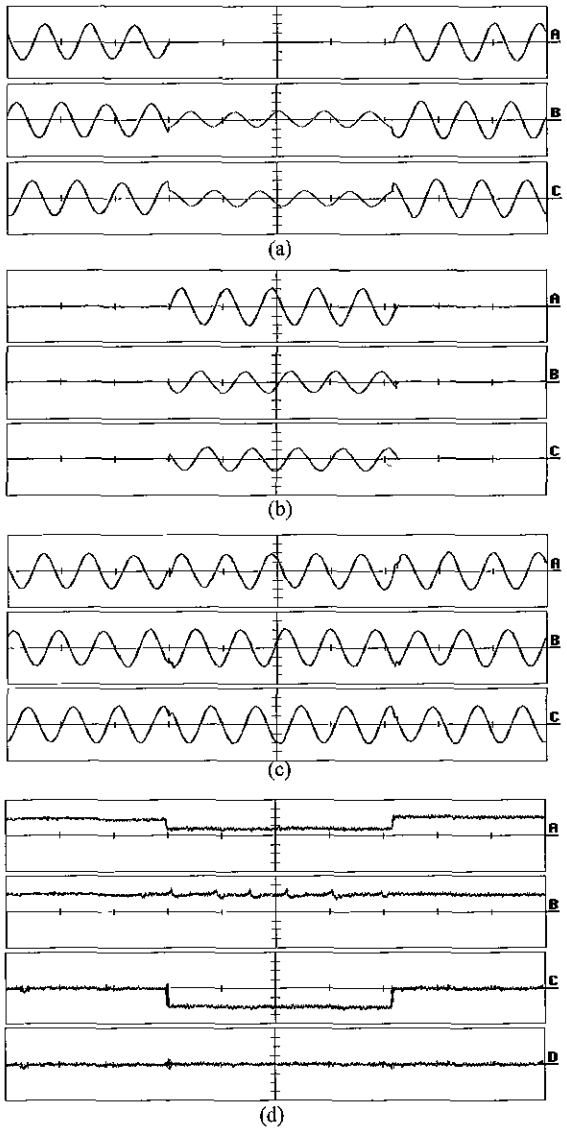


Fig 11 Experimental result under LLF condition (a) Source voltages (100V/div) (b) Compensation voltages (50V/div) (c) Load voltages (100V/div) (d) *MF* of source voltage / *MF* of load voltage / *UF* of source voltage values / *UF* of load voltage (0 5/div)

6. Conclusion

This paper proposes the detection algorithm of the faulted voltage and the control scheme of the instantaneous voltage sag corrector that can be adapted in the distribution power line The proposed detection algorithm is based on the *MF* and *UF* values to describe the reference voltage for compensation. And the turn-on time of the compensator is determined based on the ITIC curve that shows the relation between the magnitude of voltage sag and the permitted time duration of fault condition And also, the whole process for the detection and compensation is done instantaneously

A simple digital filter is inserted to suppress the noise and transient effect from the ac line voltage and it is designed that the time delay caused by this filter is compensated simultaneously for the instantaneous control The proposed algorithm includes following advantages.

compensator works with this control algorithm. For example, when 50% instantaneous voltage sag is happened, it is known from the ITIC curve of in Fig. 3 that the compensation process can be delayed for 0.2 sec after the happening of the fault accident. But as shown in Fig. 6, the fault voltage detection.

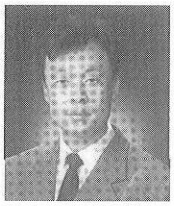
1) All control variables become to have the time invariant characteristics under the voltage fault conditions without any additional techniques.
2) The control structure becomes very simple comparing with the control algorithm of the existing synchronous coordinate.

Acknowledgements

This work has been supported in part by Electrical Engineering & Science Research Institute grant, 01-055 which is funded by Korea Electric Power Co.

References

[1] M.F. McGranaghan, et. al., *Electrical Power System Quality*, McGraw-Hill, 1996.
[2] M.H.J. Bollen, *Understanding Power Quality Problems*, IEEE Press, 1999.
[3] M.F. McGranaghan, et. al., "Voltage Sags in Industrial Systems", *IEEE Trans. on Industry Applications*, vol. 29, no. 2, pp. 397~403, 1993.
[4] G. Joos, "Three-Phase Static Series Voltage Regulator Control Algorithms for Dynamic Sag Compensation", *in Conf. Rec. of IEEE ISIE*, pp. 515~520, 1999.
[5] M.F. Granaghan, "Dynamic Sag Corrector: Cost Effective Industrial Power Line Conditioning", *in Conf. Rec. of IEEE IAS*, pp. 1339~1344, 1999.
[6] S. Lee, et. al., "A Voltage Disturbance Detection Method for Computer Application Loads", *Trans on KIPE.*, vol. 2, no. 6, pp. 584~591, 2000.
[7] S. Lee, et. al., "Power Quality Enhancement in Distribution Line using Series Compensator", *IEEE POWERCON*, pp. 1595~1600, 2000.
[8] M. Behnke, et. al., "A Three-Phase Synchronous Frame Controller for Unbalanced Load", *in Conf. Rec. IEEE PESC*, pp. 1369~1374, 1998.



Sanghoon Lee was born in Daegu, Korea, in 1969. He received B.S., M.S., and Ph. D. degrees in the Department of Electrical Engineering at the Chungbuk National University, Cheongju, S. Korea, in 1994, 1997, and 2001 respectively. Since 2001, he is a Researcher at the POSCON cooperation in S. Korea. He is a member of KIEE, KIPE, and IEEE.

Jacho Choi was born in Daejon, Korea, in 1955. He received B.S., M.S., and Ph. D. degrees from the Seoul National University, Korea, in 1979, 1981, and 1989, respectively. He was employed as a Full-time Lecturer at Jungkyoung Technical College, Daejon from 1981 to 1983. Since 1983, he has been with the Chungbuk National University, Cheongju, where he is now a Professor and Head of the School of Electrical and Electronics Engineering. In 1993 and 1998 for each a year, he was a Visiting Professor in University of Toronto, Canada and in 2000 he was a Visiting Professor in Aalborg University, Denmark. His research areas are in power electronics, power quality problems and solutions, static power converters, UPS and energy storage systems, and electrical drives. He is the Publication Editor of *JPE*.