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Analysis of Phase Error Effects Due to Grid Frequency Variation of SRF-PLL Based on APF

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Abstract

This paper proposes a compensation algorithm for reducing a specific ripple component on synchronous reference frame phase locked loop (SRF-PLL) in grid-tied single-phase inverters. In general, SRF-PLL, which is based on all-pass filter to generate virtual voltage, is widely used to estimate the grid phase angle in a single-phase system. In reality, the estimated grid phase angle might be distorted because the phase difference between actual and virtual voltages is not 90 degrees. That is, the phase error is caused by the difference between cut-off frequency of all-pass filter and grid frequency under grid frequency variation. Therefore, the effects on phase angle and output current attributed to the phase error are mathematically analyzed in this paper. In addition, the proportional resonant (PR) controller is adapted to reduce the effects of phase error. The validity of the proposed algorithm is verified through several simulations and experiments.

Key words: All-pass filter, Phase error, Grid-tied single-phase inverter, Proportional resonant (PR) controller, Synchronous reference frame phase locked loop (SRF-PLL)

I. INTRODUCTION

In general, power converters that are applicable for uninterruptible power supply, renewable energy, and distributed generation systems have been developed to transfer electric power to the grid. The performance of grid-tied single-phase inverters is continuously improving; however, it can be degraded because of the difference of phase angle and voltage between the grid and the grid-tied inverter. In order to avoid these problems, grid voltage and phase angle should be precisely synchronized with the grid-tied inverter [1]-[3].

Fig. 1 shows the conventional grid-tied single-phase inverter, which includes power conversion circuit, DC-link voltage controller, synchronous frame proportional integral (PI) current regulator, and synchronous reference frame phase-locked loop (SRF-PLL). Commonly, obtaining the grid phase angle information and frequency in the single-phase system is difficult than in the three-phase systems. Accordingly, a virtual voltage generator that uses all-pass filter (APF) is typically used in SRF-PLL [4]-[7].

In Fig. 1, the cutoff frequency of the APF is set up to 50 [Hz] or 60 [Hz] for SRF-PLL. In this case, grid frequency can be changed depending on the grid condition. The used APF can produce phase error when the actual grid frequency is different from the cutoff frequency of the APF.As a result, the estimated phase angle from the SRF-PLL is distorted, including the second harmonic component.

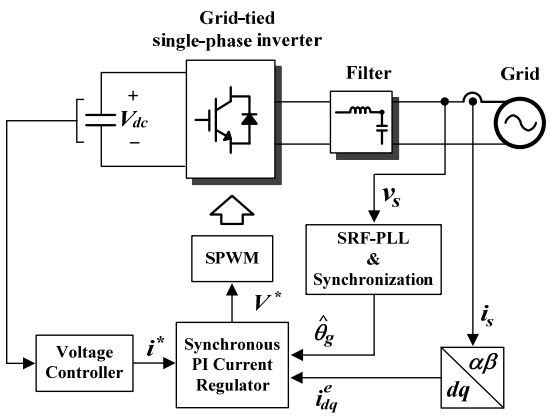

Fig. 1. Block diagram of conventional grid-tied single-phase inverter.

When the transformation matrix for synchronous frame PI current regulator with a distorted phase angle is used, synchronous *dq*-axis currents have specific ripple components [8]-[10]. The output phase current also includes

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harmonic components.

This paper analyzes the effects of the phase error in SRF-PLL on synchronous *dq*-axis voltages and output current when the grid frequency varies with the use of APF. To reduce ripple components caused by the phase error, a compensation algorithm based on the proportional resonant (PR) controller is presented [11]-[16]. The effects of phase error could be reduced significantly with the use of the proposed algorithm in the PI controller of SRF-PLL. Simulation and experimental results show the feasibility and usefulness of the proposed algorithm.

II. ANALYSIS OF SRF-PLL SYSTEM BASED ON APF

A. Generation of Virtual Grid Voltage Using APF

In a grid-tied single-phase inverter, tracking the phase angle of the grid voltage by using PLL is essential. Hence, several PLL methods exist for the single-phase inverter system, such as zero-crossing detection, enhanced phase-locked loop, and second-order generalized integrator. [8]. In this paper, SRF-PLL is used to obtain the grid phase angle for the grid-tied single-phase inverter.

Using a conventional PI controller in SRF-PLL has the advantage of steady-state error converging to zero. By contrast, because of the difficulty of tracking the phase angle in the single-phase inverter, an additional system is required to generate stationary *dq*-axis voltages.

As shown in Fig. 2, virtual two-phase voltages v_{dq}^{s} can be obtained from the measured voltage v_s by using APF. Stationary *dq*-axis voltages v_{dq}^{s} have a 90° phase difference from each other. The phase angle and frequency can be estimated by applying these two signals.

A low-pass filter can also be used to generate a virtual grid voltage, which is shifted to 90° from the grid voltage. However, the low-pass filter has a magnitude margin when the measured frequency is greater than the cutoff frequency and the phase margin is generated as well. Alternatively, with the use of an APF, which has no magnitude margin while changing grid frequency, only a phase margin is considered. Using an APF over a low-pass filter can simplify computational burden. The transfer function of APF is given by [4]

$$G_{APF}(S) = -\frac{s-\omega_A}{s+\omega_A} \tag{1}$$

where ω_A is the cutoff angular frequency.

To apply (1) on a digital platform, continuous time domain should be transformed to discrete z-domain. The digital control system is operated by sampling period T_s unlike the analog system. Therefore, delay time T_d, which is related to calculating time and output delay time, is inevitably generated. Thus, the delayed phase angle ϕ_d can be obtained as

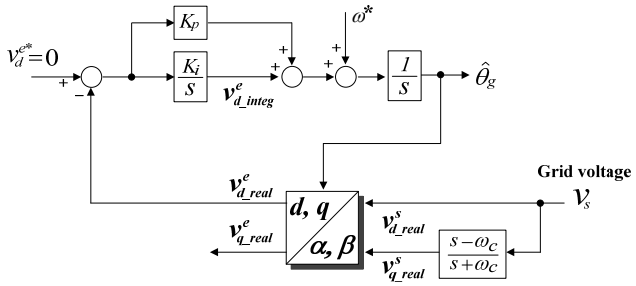


Fig. 2. Block diagram of the SRF-PLL using APF.

$$\phi_d = \frac{\pi}{2} - T_d \cdot \omega_c \tag{2}$$

The cutoff angular frequency considering the delayed phase angle can be derived as

$$\omega_A = \frac{\omega_c}{\tan\phi_d} \tag{3}$$

With the use of the bilinear transformation in (4), the transfer function of APF in discrete domain can be calculated by

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{4}$$

$$G_{APF}(z) = -\frac{\left(\frac{2}{T_s}-\omega_A\right)z-\left(\frac{2}{T_s}+\omega_A\right)}{\left(\frac{2}{T_s}+\omega_A\right)z-\left(\frac{2}{T_s}-\omega_A\right)} \tag{5}$$

B. Effects of Phase Error in SRF-PLL

The phase angle of virtual voltage can be distorted by grid frequency variation because of external factors, such as load transient characteristic when using APF.

Considering inaccurate phase information, the synchronous *dq*-axis voltages in SRF-PLL contain a harmonic component [14]. In (6), the stationary *dq*-axis voltages, including phase angle error θ_{err}, are given as follows:

$$\begin{bmatrix} v_{d\_real}^{s} \\ v_{q\_real}^{s} \end{bmatrix} = \begin{bmatrix} -V_m \sin\theta_g \\ V_m \cos(\theta_g + \theta_{err}) \end{bmatrix} \tag{6}$$

where V_m is the peak value of the grid voltage, and θ_g is the real phase angle.

Through the transformation matrix, synchronous *dq*-axis voltages can be obtained as

$$\begin{aligned} \begin{bmatrix} v_{d\_real}^{e} \\ v_{q\_real}^{e} \end{bmatrix} &= \begin{bmatrix} \cos\hat{\theta}_g & \sin\hat{\theta}_g \\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g \end{bmatrix} \begin{bmatrix} v_{d\_real}^{s} \\ v_{q\_real}^{s} \end{bmatrix} \\ &= \begin{bmatrix} -V_m \sin\hat{\theta}_g \cos\theta_g + V_m \sin\hat{\theta}_g \cos(\theta_g + \theta_{err}) \\ V_m \sin\hat{\theta}_g \sin\theta_g + V_m \cos\hat{\theta}_g \cos(\theta_g + \theta_{err}) \end{bmatrix} \end{aligned} \tag{7}$$

where $\hat{\theta}_g$ is the estimated phase angle.

On the assumption that the phase angle error is small, synchronous *d*-axis voltage on (7) can be expressed as

$$\sin\theta_{err} \approx \theta_{err}\ ,\ \cos\theta_{err} \approx 1 \tag{8}$$

$$v_{d\_real}^{e} = -V_m\,\theta_{err}\sin^2\hat{\theta}_g = -\frac{\theta_{err}V_m}{2}(1-\cos 2\hat{\theta}_g) \tag{9}$$

In (9), the second harmonic component, including the phase error, exists in the synchronous *d*-axis voltage. This harmonic affects the estimated phase angle. However, the DC component in (9) can be automatically compensated by the integral operation of PI controller. Accordingly, only the second harmonic component must be considered in estimated phase angle to analyze the effect of the phase error easily. As a result, the outputs of proportional and integral controller can be derived as follows:

$$\begin{aligned} v_{d\_\text{integ}}^{e} &= K_i\int(-v_{d\_real}^{e})dt \\ &= -\frac{K_iV_m\theta_{err}}{4\hat{\omega}_g}\sin 2\hat{\omega}_g t \end{aligned} \tag{10}$$

$$\begin{aligned} v_{d\_pro}^{e} &= K_p(-v_{d\_real}^{e}) \\ &= -\frac{K_pV_m\theta_{err}}{4\hat{\omega}_g}\cos 2\hat{\omega}_g t \end{aligned} \tag{11}$$

From (10) and (11), the total output components of the PI controller that have the phase angle error can be expressed as follows:

$$\begin{aligned} v_{d\_pi}^{e} &= v_{d\_pro}^{e} + v_{d\_\text{integ}}^{e} \\ &= -\frac{K_iV_m\theta_{err}}{4\hat{\omega}_g}\sin 2\hat{\theta}_g - \frac{K_pV_m\theta_{err}}{4\hat{\omega}_g}\cos 2\hat{\theta}_g \end{aligned} \tag{12}$$

The distorted phase angle $\hat{\theta}_{dis}$, including the second ripple component, can be ultimately written as

$$\begin{aligned} \hat{\theta}_{dis} &= \int(v_{d\_pi}^{e})dt \\ &= a\cos 2\hat{\theta}_g + b\sin 2\hat{\theta}_g \end{aligned} \tag{13}$$

where $a = -K_iV_m\theta_{err}/8\hat{\omega}_g^2$ and $b = -K_pV_m\theta_{err}/8\hat{\omega}_g^2$.

As shown in (13), the distorted phase angle can generate the specific harmonic component in the output current when using the transformation matrix. As a result, power quality could be degraded by the distorted output current.

C. Effects of Phase Error in Synchronous dq-axis Currents

In this paper, the synchronous reference frame PI current regulator is used to control the output current of the grid-tied single-phase inverter. Therefore, the effect of the phase error should be sufficiently considered in the transformation matrix. The stationary *dq*-axis currents can be expressed as follows:

$$\begin{bmatrix} i_d^s \\ i_q^s \end{bmatrix} = \begin{bmatrix} -I_m\sin\theta_g \\ I_m\cos\theta_g \end{bmatrix} \tag{14}$$

Calculated with synchronous *d*-axis voltage containing second harmonic component, the transformation matrix includes the distorted phase angle $\hat{\theta}_{dis}$ to acquire the synchronous *dq*-axis current. Hence, the synchronous *dq*-axis currents can be established as

$$\begin{aligned} \begin{bmatrix} i_d^e \\ i_q^e \end{bmatrix} &= \begin{bmatrix} \cos(\hat{\theta}_g+\hat{\theta}_{dis}) & \sin(\hat{\theta}_g+\hat{\theta}_{dis}) \\ -\sin(\hat{\theta}_g+\hat{\theta}_{dis}) & \cos(\hat{\theta}_g+\hat{\theta}_{dis}) \end{bmatrix}\begin{bmatrix} i_d^s \\ i_q^s \end{bmatrix} \\ &= I_m\begin{bmatrix} -\cos(\hat{\theta}_g+\hat{\theta}_{dis})\cdot\sin\theta_g + \sin(\hat{\theta}_g+\hat{\theta}_{dis})\cdot\cos\theta_g \\ \sin(\hat{\theta}_g+\hat{\theta}_{dis})\cdot\sin\theta_g + \cos(\hat{\theta}_g+\hat{\theta}_{dis})\cdot\cos\theta_g \end{bmatrix} \end{aligned} \tag{15}$$

When the grid angle error between θ_g and $\hat{\theta}_g$ is small, the synchronous *dq*-axis currents considering (13) can be rewritten as

$$\begin{bmatrix} i_d^e \\ i_q^e \end{bmatrix} = I_m\begin{bmatrix} \sin\hat{\theta}_{dis} \\ \cos\hat{\theta}_{dis} \end{bmatrix} = I_m\begin{bmatrix} \sin(a\cos 2\hat{\theta}_g + b\sin 2\hat{\theta}_g) \\ \cos(a\cos 2\hat{\theta}_g + b\sin 2\hat{\theta}_g) \end{bmatrix} \tag{16}$$

In (16), the synchronous *d*-axis current has the second harmonic component, and the synchronous *q*-axis current contains the fourth harmonic component attributed to the phase error.

D. Effects of Phase Error in Stationary dq-axis Voltages

The synchronous *dq*-axis currents are changed to voltage reference signals when operating the synchronous reference frame PI current regulator. The synchronous *dq*-axis voltages including phase error can be obtained by

$$\begin{bmatrix} v_{d\_o}^e \\ v_{q\_o}^e \end{bmatrix} = I_m\begin{bmatrix} K_{pc}\sin\hat{\theta}_{dis} - \dfrac{K_{ic}}{\hat{\omega}_g}\cos\hat{\theta}_{dis} \\ K_{pc}\cos\hat{\theta}_{dis} + \dfrac{K_{ic}}{\hat{\omega}_g}\sin\hat{\theta}_{dis} \end{bmatrix} \tag{17}$$

where K_{pc} is the proportional gain, and K_{ic} is the integral gain of the synchronous reference frame PI current regulator.

The output voltages of synchronous frame PI current regulator obtained by using the inverse transformation matrix can be derived as follows:

$$\begin{bmatrix} v_{d\_o}^s \\ v_{q\_o}^s \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta}_g & -\sin\hat{\theta}_g \\ \sin\hat{\theta}_g & \cos\hat{\theta}_g \end{bmatrix}\begin{bmatrix} v_{d\_o}^e \\ v_{q\_o}^e \end{bmatrix} \tag{18}$$

In addition, when the magnitude of distorted phase angle $\hat{\theta}_{dis}$ is small, (18) can be rewritten by

$$v_{d\_o}^s = v_{d\_1st}^s + v_{d\_3rd}^s \tag{19}$$

where,

$$v_{d\_1st}^s = \left(-I_mK_{pc} + \frac{aI_mK_{ic}}{2\hat{\omega}_g} + \frac{bI_mK_{pc}}{2}\right)\sin\hat{\theta}_g + \left(-\frac{I_mK_{ic}}{\hat{\omega}_g} + \frac{aI_mK_{pc}}{2} + \frac{bI_mK_{ic}}{2\hat{\omega}_g}\right)\cos\hat{\theta}_g$$

$$v_{d\_3rd}^s = \left(-\frac{aI_mK_{ic}}{2\hat{\omega}_g} + \frac{bI_mK_{pc}}{2}\right)\sin 3\hat{\theta}_g + \left(-\frac{aI_mK_{pc}}{2} + \frac{bI_mK_{ic}}{2\hat{\omega}_g}\right)\cos 3\hat{\theta}_g$$

In (19), only *d*-axis voltage is considered because the stationary *q*-axis voltage is the virtual component. The stationary *d*-axis voltage includes the third harmonic component caused by the phase error.

As a result, output current also has the same harmonic component with stationary *d*-axis voltage attributed to the phase error. According to the above equations, harmonic components in synchronous frame *dq*-axis currents and output current can be decreased by diminishing the phase error.

Hence, in this paper, compensation algorithm is proposed in SRF-PLL to efficiently reduce the effects of phase error.

III. Proposed Algorithm for Reducing Phase Error in SRF-PLL

Fig. 3 shows the block diagram of the PR controller, which is used to reduce phase error. The PR controller has a characteristic that provides an infinite gain at a selected frequency with a zero-phase shift. An ideal PR controller can be expressed as (20).

$$G_{PR\_ideal}(s) = K_{pn} + \sum_n \frac{K_{in} s}{s^2 + (n\omega_0)^2} \tag{20}$$

where K_{pn} is the proportional gain, K_{in} is the resonant gain, n is the harmonic number, and ω_0 is the resonant angular frequency.

However, infinite gain causes a decrease in the stabilization of the system. By contrast, with the use of the practical PR controller to compensate for the disadvantages of the ideal PR controller, gain and bandwidth can be modulated. The transfer function of practical PR controller can be computed as

$$G_{PR\_prac}(s) = K_{pn} + \sum_n \frac{2K_{in}\omega_c s}{s^2 + 2\omega_c s + (n\omega_0)^2} \tag{21}$$

where ω_c is the bandwidth at the cutoff frequency.

Fig. 4 shows the bode plot of the practical PR controller; the parameters that are used are proportional gain $K_{pn} = 0.2$, resonant gain $K_{in} = 1$, harmonic cumber $n = 2$, and bandwidth at cutoff frequency $\omega_c = 10$.

In order to reduce the second and fourth harmonic components in synchronous *dq*-axis currents due to phase error, two PR controllers related to each harmonic component are necessary in the synchronous reference frame PI current regulator. By contrast, in case of using PR controller in SRF-PLL, only one PR controller must be used to reduce the second harmonic component due to phase error.

Fig. 5 shows the block diagram of the proposed ripple reduction algorithm with PR controller in SRF-PLL. To decrease the second harmonic component in synchronous *d*-axis voltage of the SRF-PLL, the integrator output of PI regulator is selected as an input signal of PR controller. Also, by increasing the integrator gain K_i term, the ripple component can be expanded to easily detect the effects of phase error even if the phase error is small. Thus, the phase error effects can be reduced considerably by compensating the second harmonic component through the output signal of PR controller on synchronous *d*-axis voltage.

On the basis of the reduction of the second harmonic in synchronous *d*-axis voltage, the second and fourth harmonic components in synchronous *dq*-axis currents are decreased as well. Therefore, the third harmonic component in the output current is ultimately reduced.

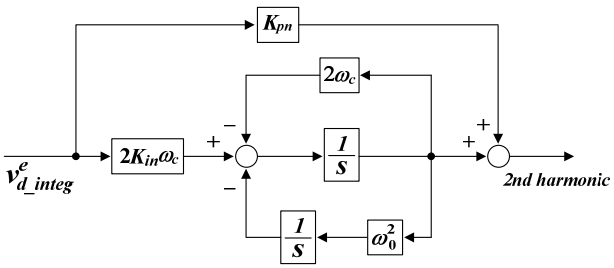


Fig. 3. Block diagram of practical PR controller.

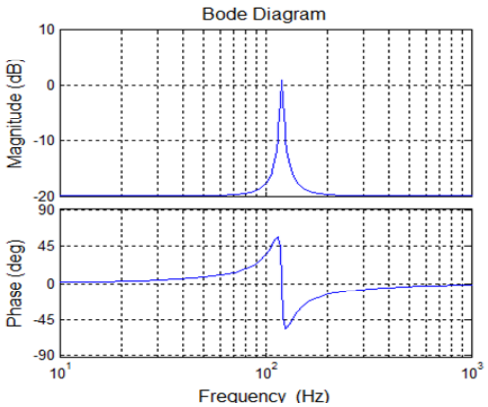


Fig. 4. Bode plot of practical PR controller.

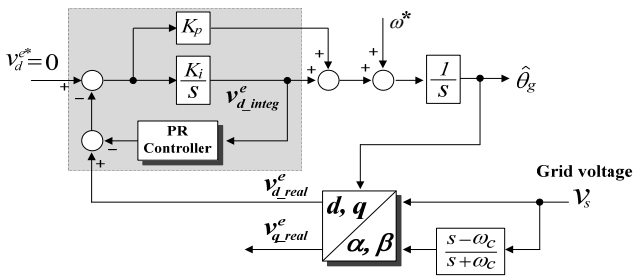


Fig. 5. Block diagram of SRF-PLL with the proposed ripple reduction algorithm.

IV. Simulation Results

To verify the proposed algorithm, simulations based on Matlab/Simulink are implemented. The designed grid-tied single-phase inverter system is shown in Fig. 6. Fig. 7 shows the SRF-PLL, including the proposed algorithm. As an input signal of PR controller, the integrator output of PI controller is chosen. As a result, the second harmonic component on the estimated phase angle due to phase error can be reduced easily by calculating the output signal of PR controller on synchronous *d*-axis voltage. The simulation was operated under conditions of 2% frequency variation.

Fig. 8 shows the synchronous *d*-axis voltage, estimated frequency, and estimated phase angle before and after using the proposed algorithm under the phase error. From Fig. 8(a), the second harmonic component due to phase error is decreased after using the proposed algorithm. In addition, tracing time for the phase error is rapid (within 0.2 [s]). Fig. 8(b) shows the estimated phase angle, including the second harmonic component. After using the proposed algorithm, the effect of phase error is reduced.

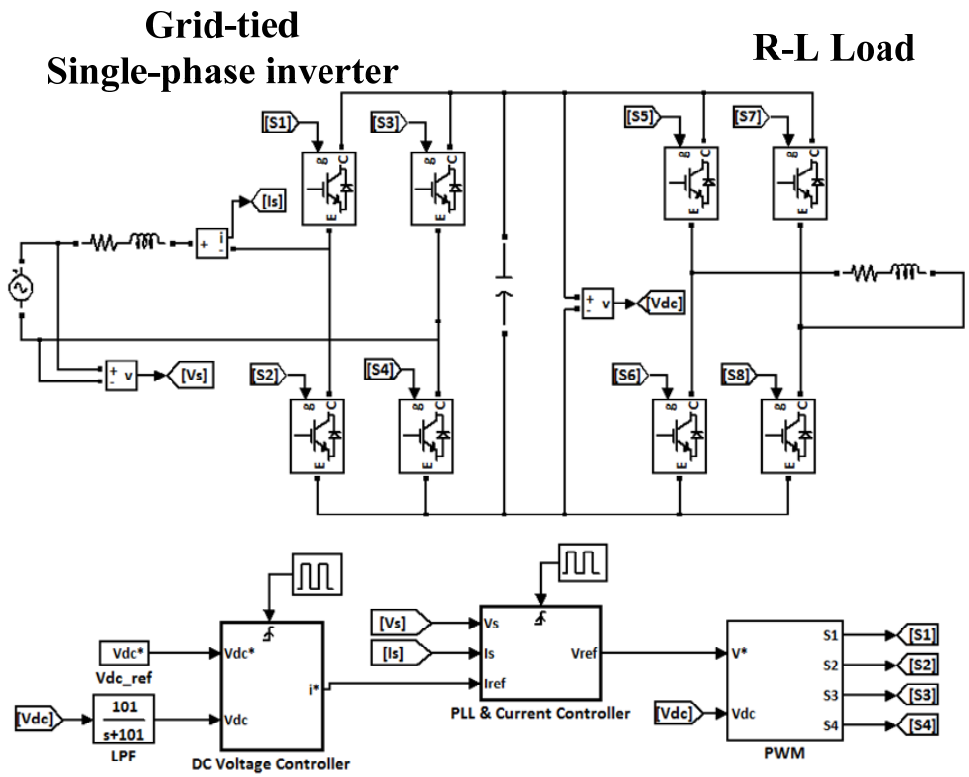


Fig. 6. Overall block diagram of grid-tied single-phase inverter.

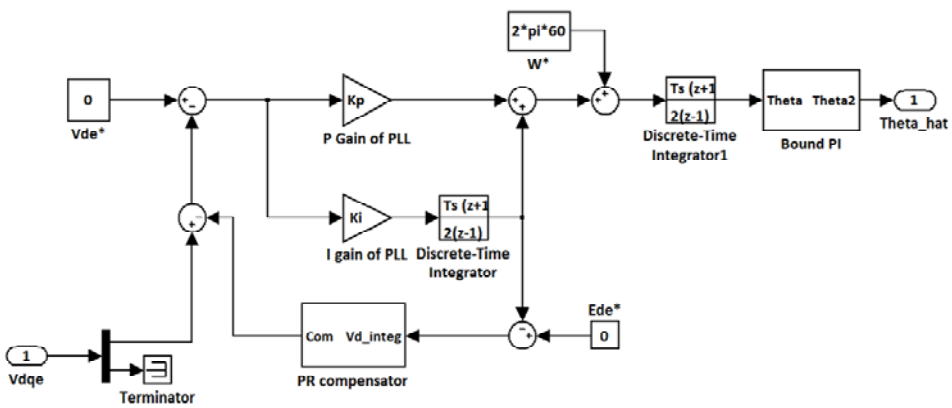


Fig. 7. Block diagram of SRF-PLL with the proposed algorithm.

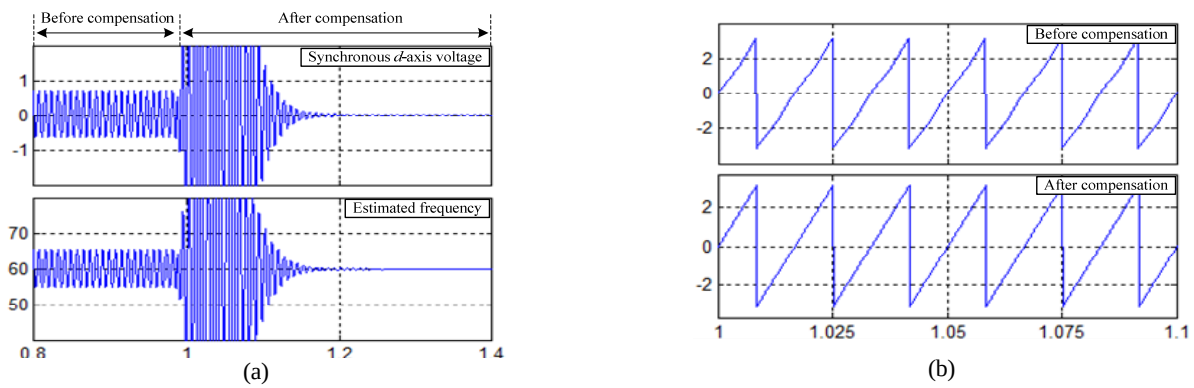


Fig. 8. Simulation results before and after using the proposed algorithm. (a) synchronous *d*-axis voltage and estimated frequency. (b) estimated phase angle.

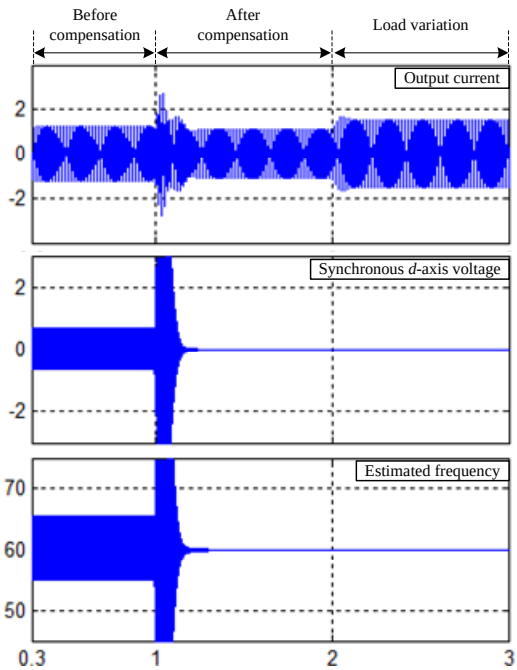


Fig. 9. Simulation waveforms of output phase current, synchronous *d*-axis voltage, and estimated frequency.

TABLE I
GRID-TIED SINGLE-PHASE INVERTER SPECIFICATIONS

Parameters	Value
Rated power	3 [kW]
Grid voltage	220 [V], 60 [Hz]
DC link capacitance	5240[uF]
Reactor inductance	5 [mH]
Sampling period	100 [us]
Switching frequency	10 [kHz]

Fig. 9 shows the output current, synchronous *d*-axis voltage, and estimated frequency before and after using the proposed algorithm under load variation. Although the output current increased from 1 A to 1.5 A because of load variation, results show that the proposed algorithm is stable and fast.

Fig. 10 shows the fast Fourier transform (FFT) results of the output current. The output current includes the third harmonic component, as computed with an imprecise phase angle. However, after using the PR controller to compensate this ripple component in synchronous *d*-axis voltage, the total harmonic distortion (THD) of output phase current improved from 6.21% to 0.95%.

V. EXPERIMENTS

The experiment platform is composed of TMS320VC33 as the digital signal processor for calculation as shown in Fig. 11. Detailed parameters and experimental setup of the designed grid-tied single-phase inverter are shown in Table I and Fig. 12, respectively. To confirm the effects of phase error, an experiment was performed under the condition of changing cutoff frequency of the APF from 55 [Hz] to 65 [Hz]. Adjusting the cutoff frequency of the APF produced the same result with grid frequency variation.

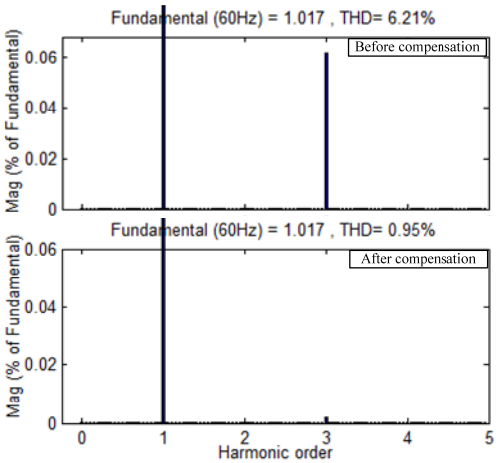


Fig. 10. FFT result of the output phase current before and after using the proposed algorithm.

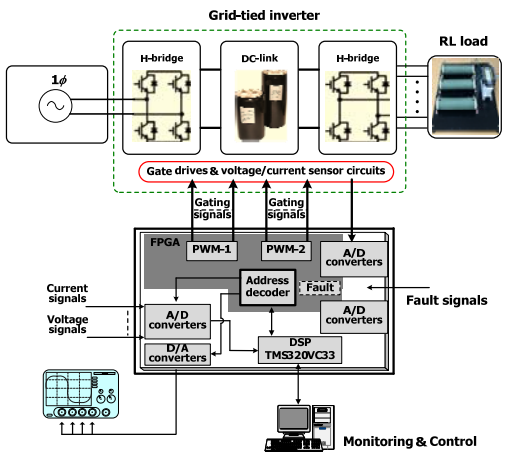


Fig. 11. Overall block diagram for grid-tied single-phase inverter.

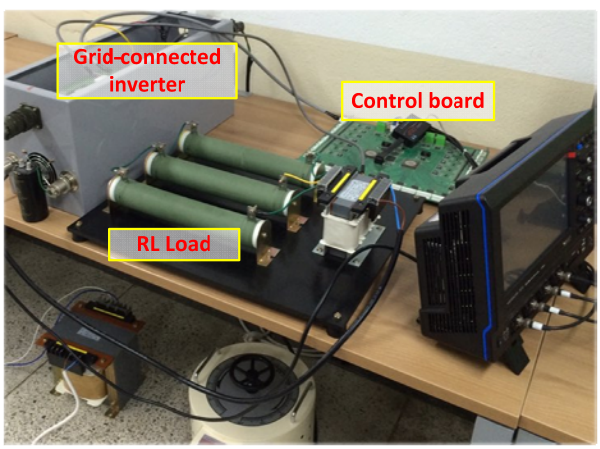


Fig. 12. Experimental setup.

Fig. 13 shows the waveforms of the estimated phase angle, integrator output of synchronous *d*-axis voltage with and without using the proposed algorithm. The integrator output of synchronous *d*-axis voltage increased the amplitude by

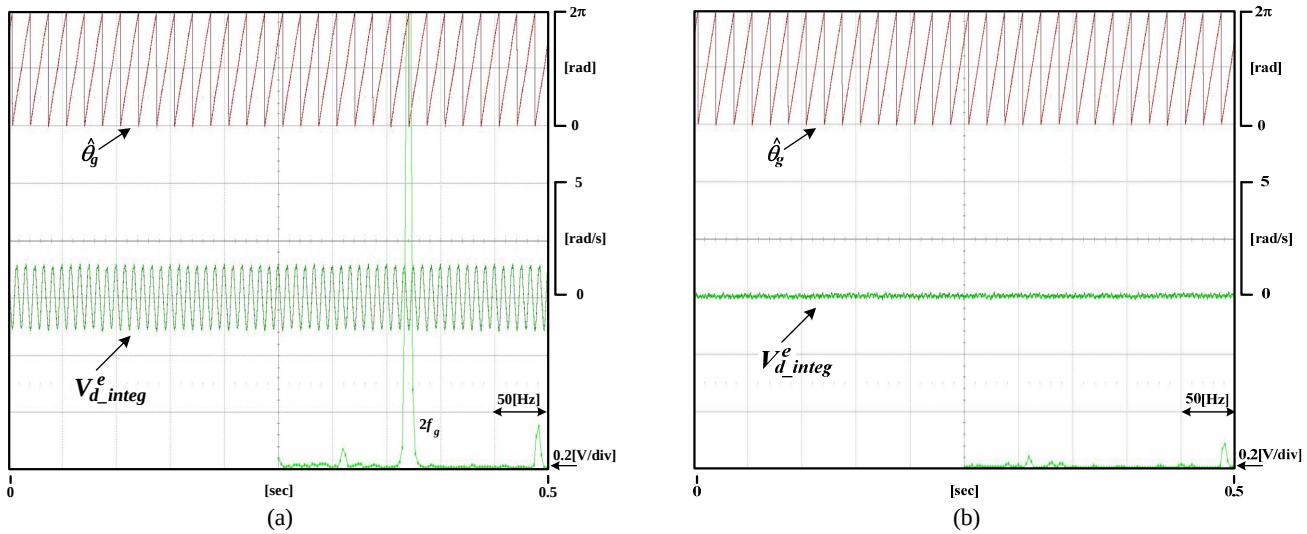


Fig. 13. Estimated phase angle, integrator output of synchronous *d*-axis voltage and FFT result. (a) without the proposed algorithm. (b) with the proposed algorithm.

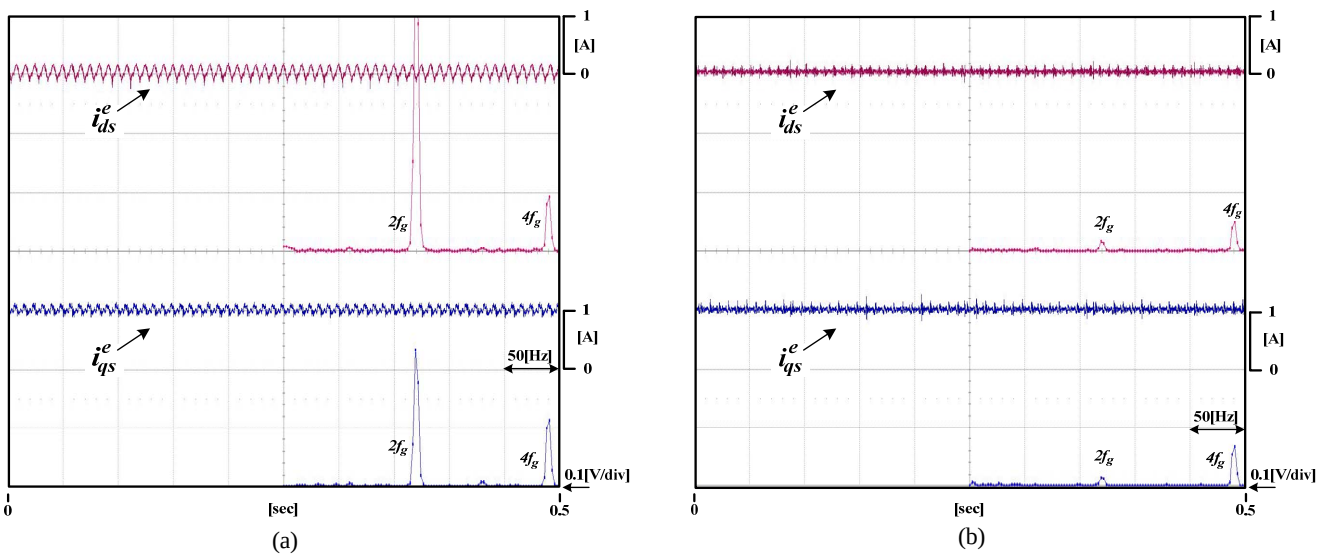


Fig. 14. Synchronous *dq*-axis currents and FFT result. (a) without the proposed algorithm. (b) with the proposed algorithm.

adjusting K_i term. Therefore, the integrator output is appropriate for the input signal of PR controller.

In Fig. 13(a), the integrator output of synchronous *d*-axis voltage has a second harmonic component under the condition of 65 [Hz] cutoff frequency of the APF. As a result of the second ripple component, the estimated phase angle contains a ripple component as well, identical to the result in (13). However, the effect of phase error is reduced significantly by using the proposed algorithm, as shown in Fig. 13(b).

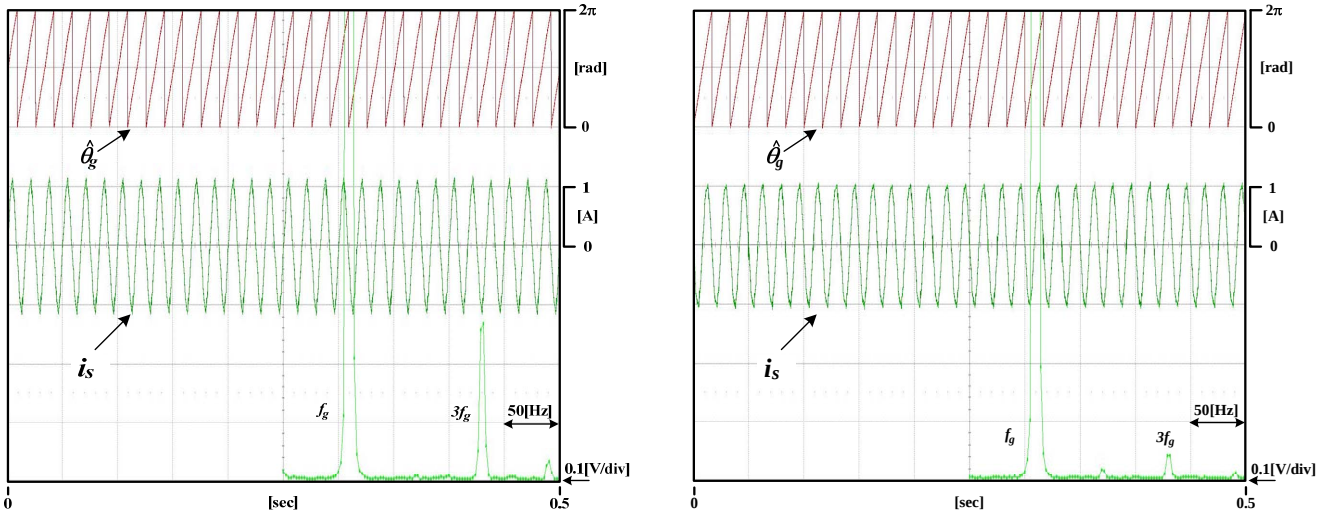
In Fig. 14, synchronous *dq*-axis currents and FFT results are expressed when the cutoff frequency of the APF is set to 65 [Hz]. In Fig. 14 (a), the synchronous *dq*-axis currents contain the second and fourth harmonic components by calculating with an inaccurate phase angle due to phase error.

However, with the use of the proposed algorithm, the effects of phase error is largely reduced, as shown in Fig. 14(b). The fourth harmonic component, which still exists after using the proposed algorithm, is the effect of dead time that is inserted to prevent switching devices from short circuiting.

Fig. 15 shows the estimated phase angle, output current, and FFT result with and without using the proposed algorithm when the cutoff frequency of the APF is set to 65 [Hz]. The third harmonic component in the output current is generated because of the phase error. Therefore, with the use of the proposed algorithm in SRF-PLL, the quality of the output current is improved, as shown in Fig. 15(b).

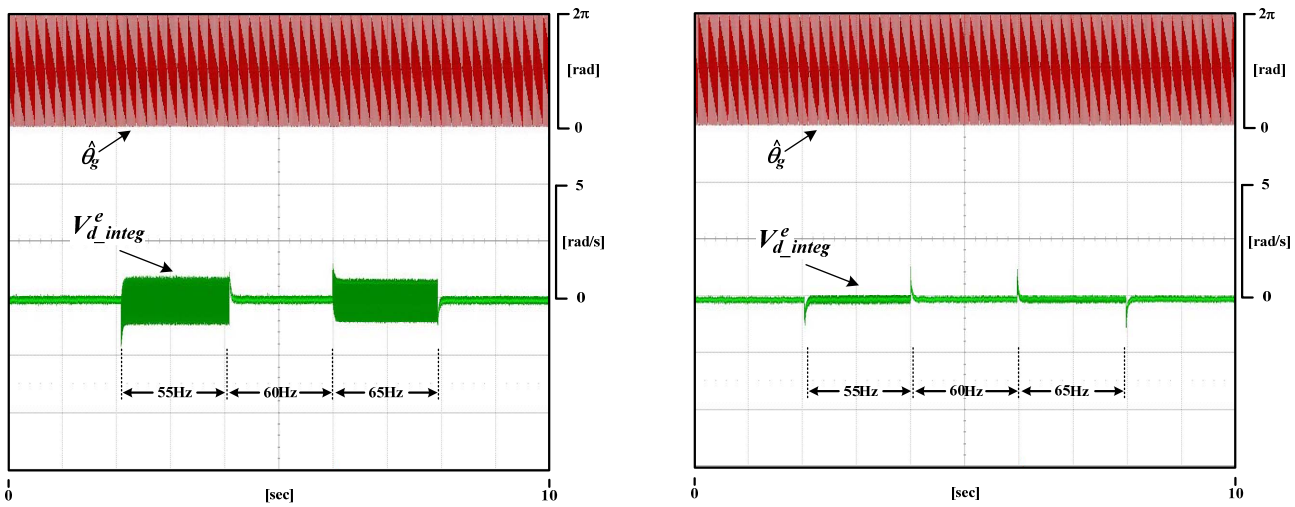
Fig. 16(a) presents the waveforms of the estimated phase angle and integrator output of synchronous *d*-axis voltage according to a grid frequency variation from 55 [Hz] to 65 [Hz]. In accordance with the grid frequency fluctuation, synchronous *d*-axis voltage includes the second harmonic component.

However, Fig. 16(b) shows that the proposed algorithm



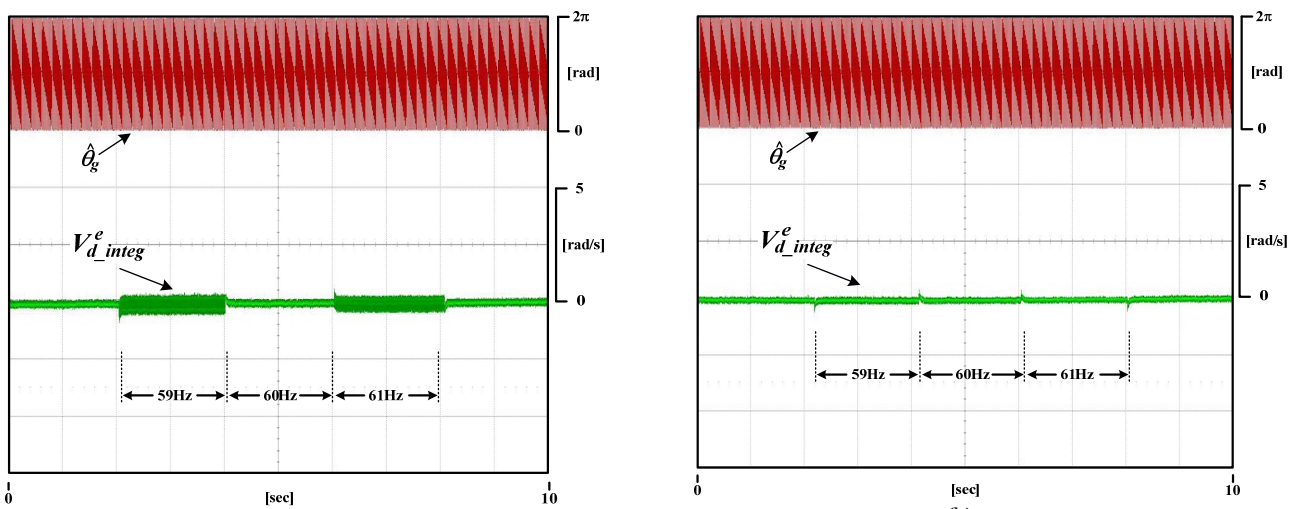
(a) (b)

Fig. 15. Estimated phase angle, output current, and FFT result. (a) without the proposed algorithm. (b) with the proposed algorithm.



(a) (b)

Fig. 16. Estimated phase angle, integrator output of synchronous *d*-axis voltage, and FFT result. (a) without the proposed algorithm. (b) with the proposed algorithm.



(a) (b)

Fig. 17. Estimated phase angle, integrator output of synchronous *d*-axis voltage, and FFT result. (a) without the proposed algorithm. (b) with the proposed algorithm.

works well when changing the grid frequency.

To prove that the proposed algorithm has good response characteristics under small- and large-scale frequency variation, Fig. 17 shows the estimated phase angle and integrator output of synchronous *d*-axis voltage when the grid frequency changes from 59 [Hz] to 61 [Hz].

Hence, the ripple component in the synchronous *d*-axis voltage is decreased by using the proposed algorithm, as shown in Fig. 17(b).

VI. CONCLUSION

In this paper, phase error effects grid frequency variation when using SRF-PLL with the APF are investigated in detail with mathematical analysis.

The phase error generates the second harmonic component in the synchronous *d*-axis voltage and the estimated phase angle. A calculation of the distorted phase angle and the transformation matrix of the current controller indicates that the synchronous *dq*-axis currents and output current also degraded. To reduce the effects of the phase error and improve the performance of the grid-tied inverter, a ripple reduction algorithm using PR controller was proposed in the PI controller of SRF-PLL. The algorithm reduced the ripple component in synchronous *d*-axis voltage significantly and enhanced the THD of the output current. Experiments and simulation results prove the value of the proposed algorithm.

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