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Optimal Design Methodology of Zero-Voltage-Switching Full-Bridge Pulse Width Modulated Converter for Server Power Supplies Based on Self-driven Synchronous Rectifier Performance

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Abstract

In this paper, high-efficiency design methodology of a zero-voltage-switching full-bridge (ZVS-FB) pulse width modulation (PWM) converter for server-computer power supply is discussed based on self-driven synchronous rectifier (SR) performance. The design approach focuses on rectifier conduction loss on the secondary side because of high output current application. Various-number parallel-connected SRs are evaluated to reduce high conduction loss. For this approach, the reliability of gate control signals produced from a self-driver is analyzed in detail to determine whether the converter achieves high efficiency. A laboratory prototype that operates at 80 kHz and rated 1 kW/12 V is built for various-number parallel combination of SRs to verify the proposed theoretical analysis and evaluations. Measurement results show that the best efficiency of the converter is 95.16%.

Key words: Full bridge converter, High efficiency, Self-driver, Synchronous rectifier, Zero-voltage switching

I. INTRODUCTION

Nowadays, high efficiency is an important key parameter in power converter design to provide good utilization of energy sources. Energy demand for Internet data centers increases continuously because of the rapid development of information technology. Therefore, data centers or server power systems need efficient power supplies to save energy and increase power density [1]-[6].

For Internet data center applications, zero-voltage-switching full-bridge (ZVS-FB) pulse width modulation (PWM) converter or phase-shifted full bridge (PSFB) converter is usually preferred because of its advantages, such as high conversion efficiency, high power density, and low electromagnetic interference (EMI) [1]-[3], [6]-[16]. For the secondary side, the use of a center-tapped rectifier is common because of the low output voltage and high output current of server power supplies [2], [6], [8]. In these applications, secondary-side conduction loss is dominated by the total conversion losses. Thus, the design optimization procedures proposed in literature usually take into account the secondary-side conduction loss of the converter to achieve high efficiency [2], [8], [11].

Synchronous rectifier (SR) is usually preferred to reduce conduction loss in converters with low output voltage and high output current applications. The parallel combination of SR achieves high efficiency effectively, as presented in [2]. In this method, eleven SRs are parallel connected, and the switching frequency is kept low to reach high efficiency. However, the use of an active gate drive method to drive SRs increases the complexity and the cost of the converter design. The self-driver method that generates the drive signals by using a power transformer is a simpler and more affordable solution than the active drive method [8], [17], [18].

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Current-driven or voltage-driven self-drivers can drive the SRs. A current-driven self-driving method proposed in [19] requires a current transformer to sense the output current and an external circuit that delivers the sensed current to a DC voltage source. A current transformer and an external circuit make the driver design complex and costly. An optimal phase- shifted full-bridge converter design is proposed in [8] uses a current-driven self-driver method proposed in [9]. This method is also a complex solution that requires a current transformer and makes the converter design more complicated compared with active gate drive methods.

A voltage-driven self-driver methods with an auxiliary method is proposed in [20]. The performance of this method depends strongly on the coupling of the transformer windings. It provides SR conduction even if the primary voltage is zero during dead time. This is the most prominent feature of the proposed self-driver method using an auxiliary winding when it uses in the converters operating with dead time. The method is also a simple and cheap solution. The performance of the proposed self-driver was tested for various transformer designs that have different couplings and for 22.5 W output power. However, detailed operation analysis taken into account the gate source capacitance or parallel connection of SRs, the stray inductance on the gate line and the body diode conduction has not been evaluated to obtain the best efficiency at high power levels.

Another solution to extend the gate drive signal of SRs during dead time is proposed in [21]. In the method, a regulated voltage is produced on the secondary side of the transformer to extend the gate drive voltages of SRs when the primary voltage is zero. The method requires two separate auxiliary windings and an extra voltage regulator circuit. The method has a complex structure, and therefore, it is a costly solution. The proposed method in [22] uses output inductor voltage to turn on SRs and uses the power transformer for the turn-off process of SRs to provide the conduction of SRs during dead time. However, this method requires two metal–oxide–semiconductor field-effect transistors (MOSFETs), two diodes, and two auxiliary windings coupled with the output inductor. Thus, the increased component number makes the method unattractive.

In this paper, high-efficiency ZVS-FB PWM DC–DC converter design methodology for server computer power supply based on the self-driven SR performance is proposed. The self-driven circuit proposed in [20] is used to drive parallel-connected SRs because of its simplicity, which allows operation during dead time. The purpose of this work is to reduce high conduction loss at the secondary side by the optimum number of self-driven SRs connected in parallel. The increase in efficiency was achieved in [2] by the parallel connection of active controlled SRs, as mentioned earlier. However, a parallel-connected self-driven SR approach has not been proposed and implemented yet. The parallel

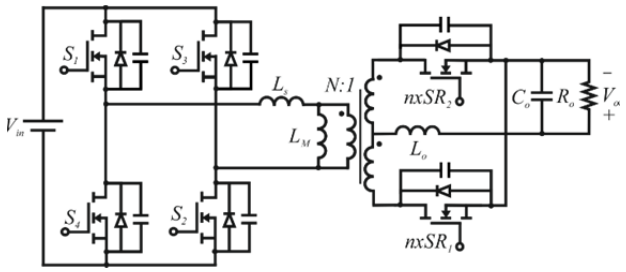


Fig. 1. Schematic of the ZVS-FB converter with parallel-connected SRs.

connection of the SRs increases the stray inductance on the gate line of SRs. Thus, inductance resonates with large gate–source capacitance of parallel-connected SRs during the operation of the converter, and this resonance can destroy the gate terminal of the SRs. Moreover, large gate–source capacitance and stray inductance on the gate line create delays on the gate voltage of the SRs, which extends the body diode conduction interval. Therefore, in this study, a variable number of self-driven parallel-connected SRs were evaluated in terms of oscillation, reliability and delay times of the gate voltage, and body diode conduction interval to achieve maximum efficiency. The proposed optimal design procedure was validated with a server power supply prototype implemented for 1 kW output power, 12 V output voltage, and 80 kHz operation frequency.

The rest of the paper is organized as follows: Section II presents the operation of power stages of the conventional ZVS-FB PWM converter. Section III presents the power loss analysis of the converter. Section IV evaluates the detailed SR self-driver analysis. Section V presents the experimental results. Section VI provides the conclusions.

II. Operation of ZVS-FB PWM DC–DC Converter

The circuit schematic of ZVS-FB PWM converter is shown in Fig. 1. A center-tapped rectifier is used because of low output voltage and high output current applications. In the circuit schematic, S_1–S_4 are the primary switches, which include antiparallel diodes and parasitic capacitors. $nxSR_1$ and $nxSR_2$ are the parallel-connected SRs used to reduce conduction losses. L_M is the mutual inductance, and L_s includes the leakage inductance of the transformer and additional inductance series connected to the primary side of the transformer. L_o and C_o are the output filter components, V_{in} is the input voltage source, and V_o is the output voltage. The transformer of the converter has N turns ratio.

In the powering stages, two diagonal MOSFETs of each leg are turned on, and in the freewheeling stage, the upper or lower side MOSFET (S_1 or S_4) and an antiparallel diode of the opposite MOSFET (S_3 or S_2) are switched on. During the output current commutation, the secondary side is clamped to the zero, and both SRs are turned on so the conduction loss is

high in this mode. However, the SRs will help to reduce conduction loss compared with the diode rectifier. In the ZVS-FB converter, the switching losses are reduced significantly by allowing a delay time between the control states of two diagonal switches. During this delay time, the parasitic capacitors of MOSFETs in one leg are discharged/charged, and ZVS turn-on is achieved.

The analytical model of the converter is required to provide the design optimization. Optimization can be derived using a basic operation principle of the converter. The operation key waveforms of the converter and the equivalent circuit diagrams of the switching states are given in Figs. 2 and 3, respectively. The operation of the ZVS-FB PWM converter can be explained in detail through three operation stages, which are presented as follows:

Stage 1 (t_0–t_1): This stage starts at $t=t_o$ through the conduction of S_1 and S_2. Thus, constant DC input voltage is applied to the primary side of the transformer, and the primary current increases linearly from the I_{p1} operation point. During this interval, SR_1 is at on-state, and the power is transferred to the output, as shown in Fig. 3(a). The primary current change for this operation can be written as

$$\frac{di_p}{dt} = \frac{V_{in} - V_o'}{(L_o' + L_s)}, \tag{1}$$

where V_o' and L_o' represent the reflected output voltage and the output filter inductor to the primary side, which can be written as

$$V_o' = nV_o \tag{2}$$

and

$$L_o' = n^2 L_o . \tag{3}$$

At $t=t_1$, the primary current reaches its peak value $I_{p\text{-}pk}$, and this stage is completed.

Stage 2 (t_1–t_3): At $t=t_1$, S_1 is turned off, and the reflected output current charges and discharges the parasitic capacitors of the S_1 and S_4 MOSFETs, as shown in Fig. 3(b). At $t=t_2$, the charge and discharge of the parasitic capacitors are completed. The reflected output current is always enough to charge and discharge the parasitic capacitors of MOSFETs in the leading leg because of high output current application. After the completion of charge and discharge processes, at $t=t_2$, freewheeling mode starts with the conduction of antiparallel diode of S_4 MOSFET, as shown in Fig. 3(c). Thus, the primary windings of the transformer are short circuited. At the secondary side, SR_1 is turned on and conducts the output current. In the freewheeling mode, the control signal of S_4 is applied to achieve ZVS turn-on. In this interval, the charge and discharge times of the parasitic capacitors are very short; therefore, these time intervals can be neglected. Thus, the primary current change can be written as

$$\frac{di_p}{dt} = \frac{V_o'}{L_o' + L_s} . \tag{4}$$

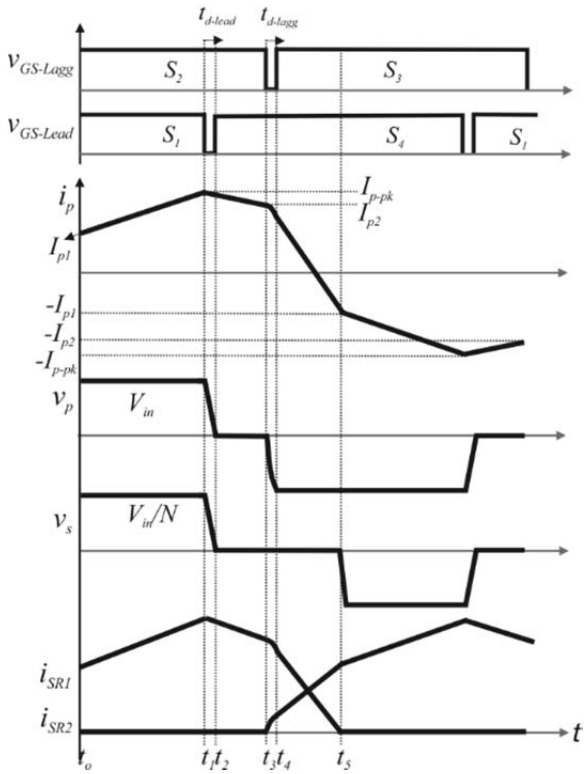


Fig. 2. Operational key waveforms of the ZVS-FB converter with the center-tapped rectifier.

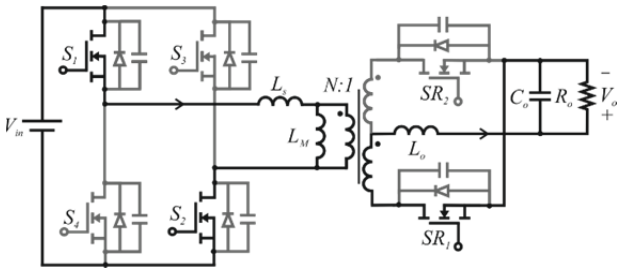
At $t=t_3$, the primary current reaches I_{p2}, S_2 turns off, and this stage finishes.

Stage 3 (t_3–t_5): In this stage, the parasitic capacitors of S_2 and S_3 MOSFETs are charged and discharged by turning off S_2, as shown in Fig. 3(d). In this interval, SR_2 also turns on, while SR_1 is under on condition. Thus, output current commutation starts from SR_1 to SR_2, and the secondary side of the transformer is short circuited. The output current cannot be reflected to the primary side. Therefore, to provide ZVS turn-on of the lagging leg switches, the stored energy in L_s inductance has to be enough because no energy is reflected from the output. After the output capacitor of S_3 discharges completely, at $t=t_4$, the antiparallel diode of S_3 conducts, as shown in Fig. 3(e). Then, the input voltage with inverse direction is applied to the primary side. The output current commutation continues between two SRs, and the secondary side of the transformer is still short circuited. In this stage, to achieve ZVS turn-on of the S_3, the control signal of the S_3 MOSFET should be applied while its antiparallel diode is on.

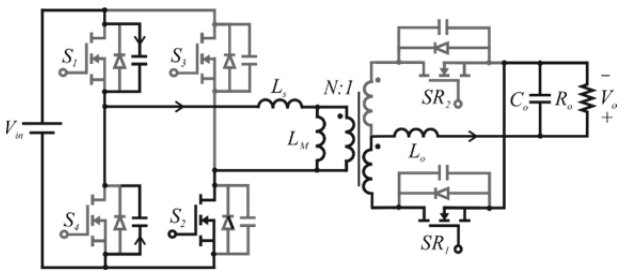
If the charge and discharge time interval of the parasitic capacitor is neglected, then the primary current change for this stage can be written as follows:

$$\frac{di_p}{dt} = -\frac{V_{in}}{L_s} . \tag{5}$$

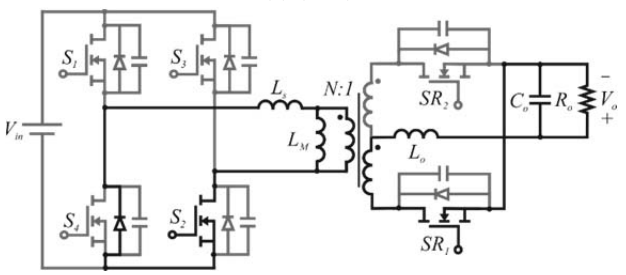
In this operation interval, the output current commutation at the secondary side causes lost duty cycle, ΔD, because no energy is transferred from the input to the output. This



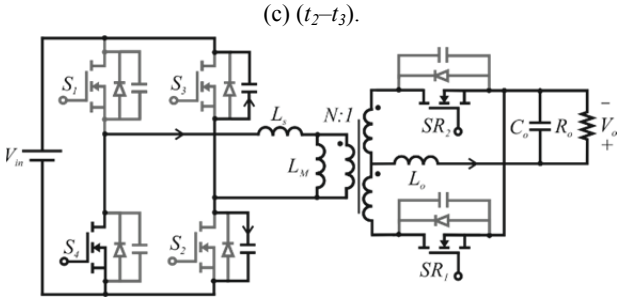
(a) (t_0–t_1).



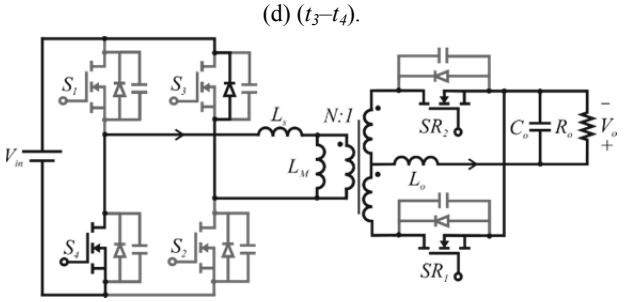
(b) (t_1–t_2).



(c) (t_2–t_3).



(d) (t_3–t_4).



(e) (t_4–t_5).

Fig. 3. Equivalent circuits belong to the switching states of the ZVS-FB converter with the center-tapped rectifier: (a) t_0–t_1; (b) t_1–t_2; (c) t_2–t_3; (d) t_3–t_4; and (e) t_4–t_5.

situation can be defined approximately as

$$\Delta D \approx \frac{2I_o L_s f_s}{NV_{in}} \tag{6}$$

where f_s is the switching frequency, and I_o represents the output current. At $t=t_5$, the primary current is changed from I_{p2} to $-I_{p1}$, and the half of one switching period is completed. The remaining half cycle operates with the same principle but with a change in the direction of the primary current and voltage.

III. Power Loss Analysis

The total power losses of the ZVS-FB PWM DC–DC converter mainly come from the magnetic components, the primary semiconductors, and the secondary semiconductors. To compute the power loss, the calculation procedure that applies data sheet parameters can be derived as follows:

A. Magnetic Components

The magnetic components of the converter are composed of the transformer and the output filter inductor. The losses of the magnetic components consist of the copper and the core loss. The copper losses can be estimated by using high-frequency AC resistance of the windings as follows:

$$P_{Cu-Tr} = I_{p-RMS}{}^2 R_{AC-pr} + 2I_{\sec-RMS}{}^2 R_{AC-\sec} \tag{7}$$

where $R_{AC\text{-}pr}$ and $R_{AC\text{-}sec}$ are the AC resistance of the primary and secondary windings, respectively, $I_{p\text{-}RMS}$ is the root mean square (RMS) current value of the primary windings, and $I_{sec\text{-}RMS}$ is the RMS current value flowing in secondary windings.

The core losses can be extracted by using Steinmetz equation given as follows:

$$P_{Core-Tr} = Kf_s{}^{\alpha} B_m{}^{\beta} V . \tag{8}$$

The parameters of k, β, and α are found by curve fitting. B_m is the peak value of the magnetic flux density applied to the transformer, and V is the volume of the core.

The losses of the output filter inductor are calculated through the same approach applied for the transformer loss calculation. However, the output current has very small high-frequency AC component compared with its DC component. Therefore, skin effect and proximity effects can be neglected in the copper loss calculation. The core loss is usually neglected because the magnetic flux density variation is extremely small. Thus, the copper loss can be written as

$$P_{Cu-Lo} = I_o{}^2 R_{DC-Lo} \tag{9}$$

where $R_{DC\text{-}Lo}$ is the DC resistance of the windings of the output filter inductor.

B. Primary Semiconductors

The MOSFETs were used as primary switches in the converter because of their high-frequency operation capability. The switching loss and the conduction loss are taken into account in the optimization of MOSFETs. The turn-on switching loss of the leading leg MOSFETs can be accepted as zero because of their soft switching turn-on process. The lagging leg MOSFETs is also turned on with the ZVS up to a certain load condition. Under light load

conditions, the switching loss for the lagging leg MOSFETs can be defined as

$$P_{sw,on-lagg} = 2 \times \frac{1}{2} C_{lagg} V_r^2 f_s. \quad (10)$$

In Equ. (10), V_r is the remaining voltage across equivalent resonant capacitor C_{lagg} in the lagging leg after the dead time interval is completed. V_r can be defined as follows:

$$V_r = V_{in} - \sqrt{\frac{L_s}{C_{lagg}}} I_{p2} \quad (11)$$

where I_{p2} is the primary current starting resonance between the L_s and C_{lagg} and also the turn-off current of the lagging leg MOSFETs, as shown in Fig. 2. The turn-off switching loss of the switches at each leg can be written as

$$P_{sw,off-lead} = \frac{1}{2} V_{in} I_{p-pk} t_f f_s \quad (12)$$

and

$$P_{sw,off-lagg} = \frac{1}{2} V_{in} I_{p2} t_f f_s, \quad (13)$$

where $I_{p\text{-}pk}$ is the turn-off current of the leading leg MOSFETs, t_f is the falling time obtained from the datasheet of MOSFETs.

The conduction loss of a primary MOSFET is defined by

$$P_{cond-pr} = I_{pr-MOSFET-RMS}^2 R_{pr-MOSFET-on} \quad (14)$$

where $I_{pr\text{-}MOSFET\text{-}RMS}$ is the RMS current value that flows in the primary MOSFETs, and $R_{pr\text{-}MOSFET\text{-}on}$ is the turn-on resistance of the primary MOSFETs.

The drive loss of a MOSFETs can be written as

$$P_{drive} = \frac{1}{2} C_{GS} V_{GS}^2 f_s \quad (15)$$

where C_{GS} is the gate–source capacitance of the MOSFET, and V_{GS} is the drive voltage applied to the gate–source terminal of the MOSFET.

C. Secondary Semiconductors

The losses of the secondary switches are calculated using the same approach applied for the primary MOSFETs. A parallel combination of SRs is considered to reduce high conduction losses because of the application of high output current. Thus, the conduction loss of SRs can be extracted by

$$P_{SR,cond} = I_{SR-RMS}^2 \frac{R_{SR-on}}{n_{SR}} \quad (16)$$

where $I_{SR\text{-}RMS}$ is the RMS current that flows in the parallel-connected SRs, $R_{SR\text{-}on}$ is the conduction resistance of the SR, and n_{SR} is the number of parallel-connected SRs.

The switching loss of the SRs can be neglected because SRs are turned on and off during the freewheeling operation interval of the converter, which gives approximately zero voltage across the SRs.

The body diodes of the SRs conduct to provide a current path below the threshold voltage level during the turn-on and turn-off transitions of the SRs. The conduction losses of the body diodes will be evaluated in detail in Section IV.

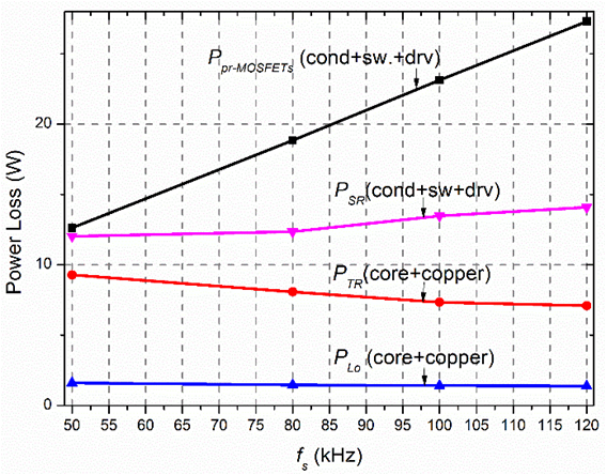


Fig. 4. Power loss breakdown of the proposed ZVS-FB converter based on switching frequency.

D. Loss Breakdown Based on Switching Frequency

To evaluate the switching frequency effects on power loss analysis, the loss breakdown of the proposed ZVS-FB converter based on the switching frequency was extracted and presented in Fig. 4. The MOSFETs on the primary side are turned off hard in the ZVS-FB converter, as mentioned earlier. This limits the switching frequency of the converter. The switching and driving loss increase the total power loss of primary switches $P_{pr\text{-}MOSFETs}$ while the switching frequency increases. The secondary switches have approximately zero switching loss because they are turned on and off during the freewheeling interval of the converter. The driving loss increases the total power loss of secondary switches P_{SR} with increased switching frequency.

The magnetic flux density variation of the transformer is reduced by the increase in the switching frequency. Thus, the core loss of the transformer reduces at the increased switching frequency operations. The high-frequency AC resistance losses of the windings can be reduced by using thin copper foils or litz wire in the transformer design. Proximity effects can also be reduced by the interleaved transformer design. Therefore, conduction loss does not change the total power loss of transformer P_{TR} at high-switching-frequency regions. The core loss change is more dominant than the winding loss; thus, the loss variation curve drops in Fig. 4.

The AC component variation of the output filter inductor is very small; therefore, its power loss P_{Lo} is not affected by the frequency change.

IV. Performance Evaluation of The Self-Driven Secondary Switches

SR is usually used to reduce high conduction loss and obtain high efficiency for low output voltage and high output current applications. Thus, in this optimal design approach,

SR is considered for the secondary switches of the center-tapped rectifier. The parallel combination of SRs also helps to further reduce high conduction loss. To drive the SRs, two options, namely, active drive and self-driven techniques, are applicable. The self-driven method generating signal by using an auxiliary winding or a directly power transformer is a cheap and simple option compared with the active gate drive method. However, the parallel combination of the SRs works safely depending on the self-driver performance because of high stray inductance on the gate line of the SRs.

The self-driver technique, which uses an auxiliary winding proposed in [20], is selected to drive the SRs because the self-driven circuit keeps the gate voltage above the threshold voltage when the primary voltage is zero. The circuit schematics of the self-driver and the equivalent circuits that operates it are given in Figs. 5 and 6, respectively. A detailed analysis of the self-driver is given in [20] and [23]. The effects of the parallel-connected SRs on self-driver performance are discussed in this section.

In the equivalent circuit of the self-driver, R_g is the series gate resistor connected to the gate terminal of the SR. R_p is the parallel resistor connected to the gate–source terminal of the SR. L_e represents the total inductance on the gate line of SRs. L_e includes the stray inductance on the printed circuit board (PCB) and the leakage inductance of the auxiliary winding. The voltage across the auxiliary winding is represented by v_g. C_{GS} is the internal gate–source capacitance of the SR. SR_1 and SR_2 are the SRs used for the center-tapped rectifier.

In the operation of the self-driver, the gate–source capacitance of SR_1 is charged when V_g voltage is positive, and the same charge current discharges the gate–source capacitor of SR_2, as shown in Fig. 6(a). Thus, the gate voltage of SR_2 drops to zero, and D_2 diode conducts. Then, the gate–source terminal of SR_2 is clamped by the drop voltage of D_2, $-V_{D2}$. The gate voltage expressions that belong to each SR can be extracted by analyzing the equivalent circuit given in Fig. 6(a) as follows:

$$v_{G1S}(t)=v_{G1S}(t_0)+\frac{V_g R_p}{2R_p+R_g}\times \left[\begin{array}{l} 1+e^{-\frac{1}{2}\alpha(t-t_0)}\left(-\cosh\left(\frac{1}{2}(t-t_0)\sqrt{\alpha^2-4\beta}\right)\right. \\ \left.-\frac{\alpha}{\sqrt{\alpha^2-4\beta}}\sinh\left(\frac{1}{2}(t-t_0)\sqrt{\alpha^2-4\beta}\right)\right) \end{array}\right]; \quad (17)$$

$$v_{G2S}(t)=v_{G2S}(t_0)-\frac{V_g R_p}{2R_p+R_g}\times \left[\begin{array}{l} 1+e^{-\frac{1}{2}\alpha(t-t_0)}\left(-\cosh\left(\frac{1}{2}(t-t_0)\sqrt{\alpha^2-4\beta}\right)\right. \\ \left.-\frac{\alpha}{\sqrt{\alpha^2-4\beta}}\sinh\left(\frac{1}{2}(t-t_0)\sqrt{\alpha^2-4\beta}\right)\right) \end{array}\right]; \quad (18)$$

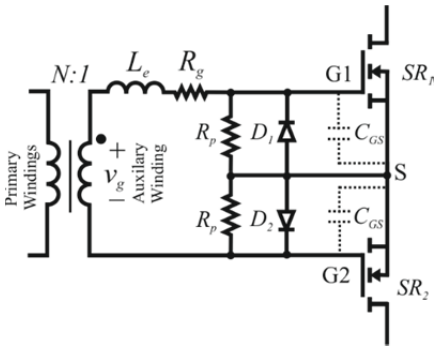
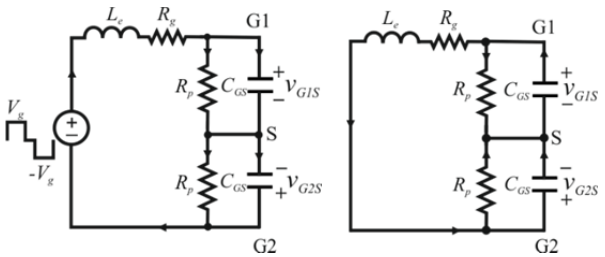


Fig. 5. Self-driver circuit proposed in [20].



(a) v_g>0. (b) v_g=0.

Fig. 6. Equivalent circuits of the self-driver operation principle.

$$\alpha=\frac{R_g R_p C_{GS}+L_e}{L_e C_{GS} R_p}; \quad (19)$$

$$\beta=\frac{2R_p+R_g}{L_e C_{GS} R_p}; \quad (20)$$

$$v_{G1S}(t_0)=v_{G2S}(t_0)\geq V_{th}; \quad (21)$$

and

$$V_G=\frac{V_{in}}{N} \quad (22)$$

In the aforementioned equations, the gate–source voltage of each SR at $t=t_0$ is assumed to be higher than threshold voltage, V_{th}.

During the dead time period or while the primary voltage of ZVS-FB converter is zero, the gate–source capacitance of SR_1 discharges, and its discharge current charges the gate–source capacitance of SR_2, as shown in the equivalent circuit given in Fig. 6(b). Thus, both gate–source capacitances have the same voltage level, which can maintain both SRs in the on condition during the output current commutation of the converter. On the basis of the analysis of the equivalent circuit given in Fig. 6(b), the gate voltage expressions are found as follows:

$$v_{G1S}(t)=v_{G1S}(t_1)-\frac{(V_g-V_{Rg}-V_{D2})R_p}{2R_p+R_g}\times \left[\begin{array}{l} 1+e^{-\frac{1}{2}\alpha(t-t_1)}\left(-\cosh\left(\frac{1}{2}(t-t_1)\sqrt{\alpha^2-4\beta}\right)\right. \\ \left.-\frac{\alpha}{\sqrt{\alpha^2-4\beta}}\sinh\left(\frac{1}{2}(t-t_1)\sqrt{\alpha^2-4\beta}\right)\right) \end{array}\right]; \quad (23)$$

$$v_{G2S}(t) = v_{G2S}(t_1) + \frac{(V_g - V_{Rg} - V_{D2})R_p}{2R_p + R_g} \times \left[1 + e^{-\frac{1}{2}\alpha(t-t_1)} \left(-\cosh\left(\frac{1}{2}(t-t_1)\sqrt{\alpha^2 - 4\beta}\right) - \frac{\alpha}{\sqrt{\alpha^2 - 4\beta}} \sinh\left(\frac{1}{2}(t-t_1)\sqrt{\alpha^2 - 4\beta}\right) \right) \right]; \quad (24)$$

$$v_{G2S}(t_1) = -V_{D2}; \quad (25)$$

and

$$v_{G1S}(t_1) \geq V_g - V_{Rg} - V_{D2}, \quad (26)$$

when the V_g voltage is negative, same operation principle given for positive V_g works with the inversed current direction.

A. Gate Voltage Oscillation Analysis

The increase in the number of parallel-connected SRs can cause a large stray inductance on the gate line because of the long interconnections. Thus, an overshoot can occur on the gate voltage because of the resonance between the gate capacitance and the inductance, which includes the stray inductance on the PCB and the leakage inductance of the transformer. The parallel connection of the SRs also causes large gate–source capacitance. The change in the gate voltage according to the inductance value on gate line, L_e, and gate capacitance, C_{GS}, was calculated by using Equ. (24). In the calculations, the gate voltage was not damped because R_g resistor is selected as 0.1 Ω to show the effect of C_{GS} and L_e on gate voltage oscillation. The IRFP4110Pbf MOSFET that has 9.62 nF gate–source capacitance was used as the SR, taking into consideration the output rates of the converter. The variation of L_e was assumed to vary between 3 nH and 28 nH. The calculation results are plotted in Fig. 7. The increase in the gate capacitance reduces the peak value of the gate voltage because of the limited gate charge current. The graph also shows that increasing L_e causes the high peak value of the gate voltage. This voltage oscillation can be damped by suitable gate resistance R_g and parallel-connected resistance R_p. Fig. 8 evaluates the gate voltage response for different R_g and R_p values. As shown in Fig. 8(b), R_p variation cannot effectively damp the gate voltage oscillation occurred with 0.1 Ω gate resistance. R_g and L_e are the main parameters to improve the quality of the gate voltage of SRs.

B. Delay Times and Body Diode Conduction Analysis

In driver optimization, the body diode conduction period is also an important parameter to evaluate conduction loss. The body diodes of SRs conduct until the gate voltage reaches the threshold voltage and after the gate voltage falls below the threshold voltage level. The rising and falling edge delay times can be extracted by the gate voltage waveforms plotted with gate voltage expressions, which are given in Equs. (24) and (18), respectively, because these expressions define the charge and discharge of the gate–source capacitances of SRs.

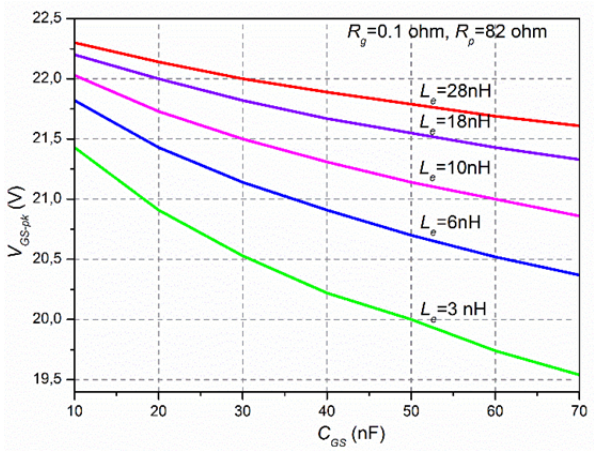
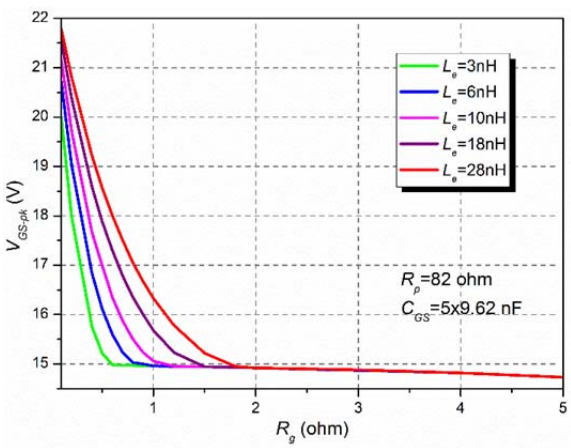
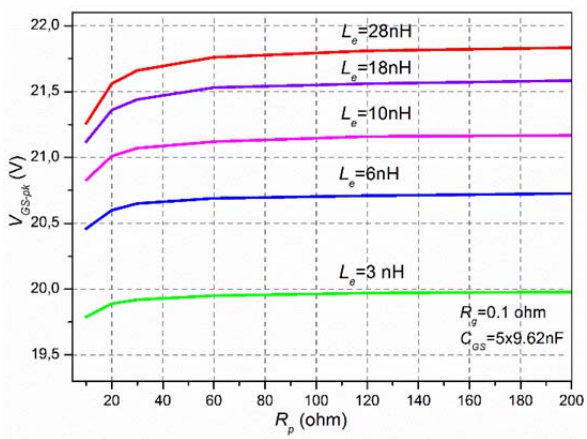


Fig. 7. Gate voltage response for different C_{GS} and L_e values.



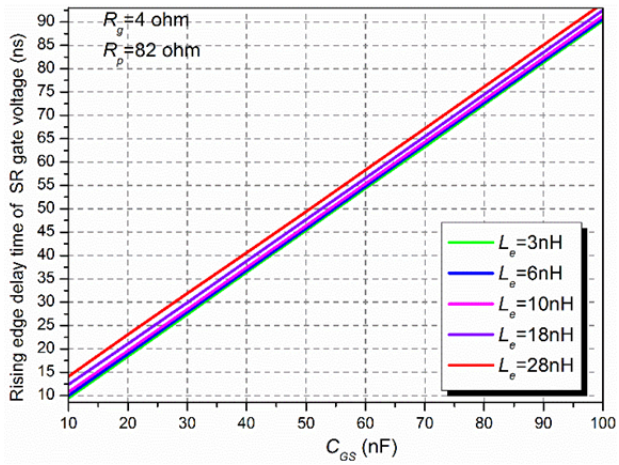
(a)



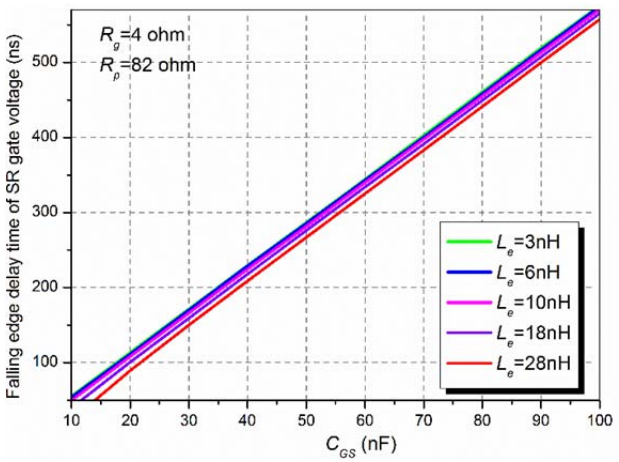
(b)

Fig. 8. Gate voltage response for different (a) R_g and (b) R_p values.

The varying delay times on the rising and falling edges as a function of the inductance on the gate line and gate capacitance were calculated and plotted in Fig. 9. In the calculations, threshold voltage of IRFP4110Pbf MOSFET is obtained as 2 V from its datasheet. Fig. 9(a) shows that the rising edge delay time is extended with the increase in inductance value and gate capacitance. However, in Fig. 9(b),



(a)



(b)

Fig. 9. (a) Rising edge and (b) falling edge delay times as functions of C_{GS} for different L_e.

the falling edge delay is decreased by the increase in inductance value on the gate line and increased by the increase in gate capacitance. The large inductance value limits the discharge of the gate capacitance. Thus, the gate voltage belatedly falls to the threshold voltage and body diode conduction at the falling edge decreases. However, this condition can cause an overshoot problem; thus, the inductance on the gate line cannot be a parameter to reduce body diode conduction period. According to the performance analysis, low L_e provides the best results in terms of oscillation on the gate voltage and body diode conduction.

In the proposed analytical model, L_e value was supposed to predict the gate voltage behavior. Determination of the real inductance value requires a three-dimensional magnetic modeling technique, which is not the focus of this study.

To prevent the shoot-through problem, the following analysis that determines the limit of falling edge delay time is presented. Fig. 10 shows the conduction of the SR_1 and its body diode. The body diode of SR_1 conducts at the rising edge and the falling edge of the gate control voltage. The conduction loss of the body diode can be written with the

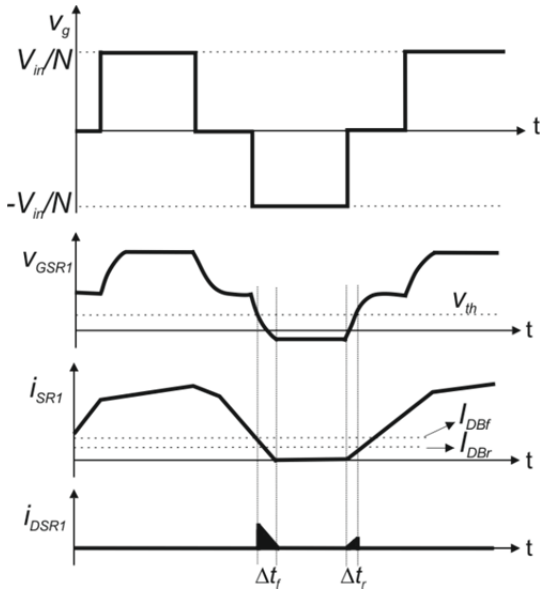


Fig. 10. Key waveforms belonging to the operation of SR_1.

help of the given waveforms as follows:

$$P_{cond-body} = f_s \frac{1}{2} V_{FW} (I_{DBf} \Delta t_f + I_{DBr} \Delta t_r) \quad (27)$$

where V_{FW} is the drop voltage of the body diode, and I_{DBf} and I_{DBr} are the secondary current values when SR_1 is turned off and on, respectively. These current expressions can be written as

$$\frac{I_{DBf}}{\Delta t_f} = \frac{V_{in}/N}{L_s/N^2} \Rightarrow I_{DBf} = \frac{V_{in} N \Delta t_f}{L_s} \quad (28)$$

$$\frac{I_{DBr}}{\Delta t_r} = \frac{V_{in}/N}{L_s/N^2} \Rightarrow I_{DBr} = \frac{V_{in} N \Delta t_r}{L_s}. \quad (29)$$

In Equs. (28) and (29), Δt_f and Δt_r are the falling and rising edge delay times of the gate voltage evaluated in Fig. 9, respectively. These time intervals also show the body diode conduction intervals. Thus, to prevent the shoot-through problem, the falling edge delay time can be limited as follows:

$$\frac{\Delta D}{f_s} = \frac{(I_{p1} + I_{p3}) L_s}{V_{in}} \quad (30)$$

and

$$\Delta t_f \le \frac{\Delta D}{f_s}. \quad (31)$$

The calculated body diode conduction loss and the full load efficiency variation based on the gate–source capacitance are given in Fig. 11. The efficiency values were calculated according to power loss analysis given earlier and body diode conduction loss given in Equ. (27). The efficiency values were marked on the curve of the body diode conduction loss variation along the gate–source capacitance values. The calculations show that the best efficiency can be obtained with the 5xSR operation. The further increase in the

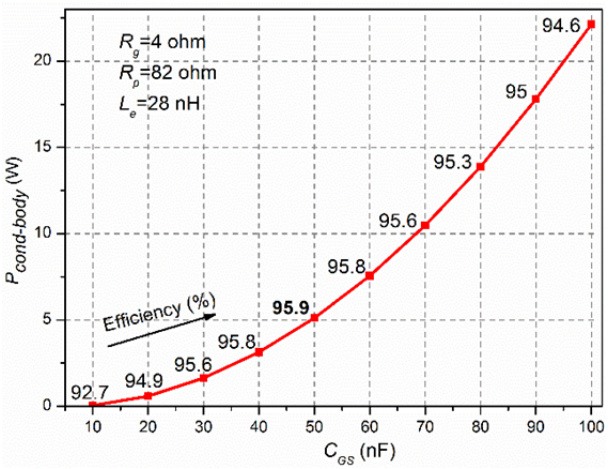


Fig. 11. Body diode conduction loss and efficiency variation based on gate–source capacitance.

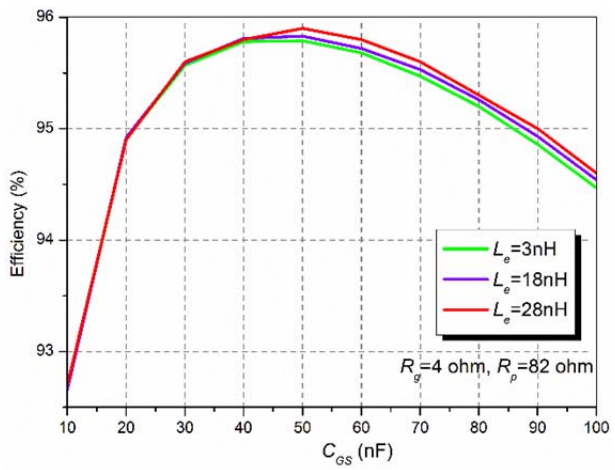


Fig. 12. Efficiency variation based on C_{GS} and L_e.

parallel connection of SR reduces the efficiency because of the extended delay times at the rising and falling edges.

Fig. 12 shows the efficiency variation as a function of stray inductance on the gate line and gate–source capacitance. The best efficiency is obtained with the 5xSR operation for all L_e values. Although the highest L_e value shows the highest efficiency, the shoot-through problem does not allow the operation of the converter.

V. Experimental Results

A server power supply prototype, which has 12 V output voltage and 1 kW output power, was built to verify the proposed design approach. The components used in the prototype are listed in Table I. The input voltage is obtained from a DC power supply with 400 V. The secondary side of the converter was separately tested for the 3x*SR*, 4x*SR*, 5x*SR*, 8x*SR*, and 10x*SR* operations.

In Fig. 13, the gate voltage waveforms of the SRs for the 3x*SR*, 5x*SR*, 8x*SR*, and 10x*SR* operations were separately given. The measurements were taken with R_g=3.9 Ω and

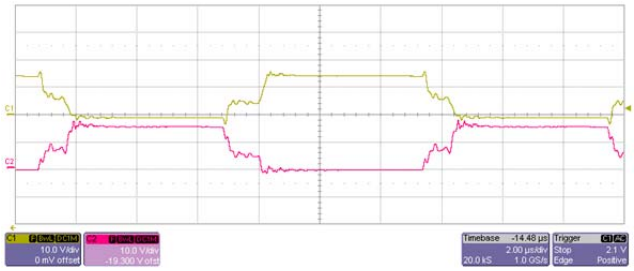
TABLE I
Components Used in the Built Prototype

Primary switches	CMF20120D
Secondary switches	3xIRFP4110Pbf 4xIRFP4110Pbf 5xIRFP4110Pbf 6xIRFP4110Pbf 8xIRFP4110Pbf 10xIRFP4110Pbf
Transformer	E65/32/27, N:25 N_p=25, N_s=1, N_{aux}=1
Output inductor, L_o	1.1 μH
Additional inductor, L_s	15 μH
Output capacitor	264 μF Ceramic capacitor

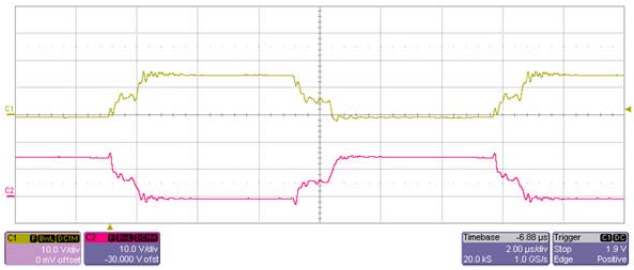
R_p=82 Ω. In Figs. 13(a)-13(c), the gate drive voltage of SRs during dead time were measured above the 2 V threshold voltage. The gate voltage waveforms obtained with the 3x*SR*, 5x*SR*, and 8x*SR* operations seem to be more reliable compared with that obtained by the 10x*SR* operation. In Fig. 13(d), the gate voltage has large ringing at the falling edge although full input voltage was not applied because of the shoot-through problem.

After the measurement of the gate voltage performance, 10x*SR* operation is considered an unsafe operation. Therefore, the efficiency measurements were taken with the 3x*SR*, 4x*SR*, 5x*SR*, 6x*SR*, and 8x*SR* operations to validate the theoretical analysis. Fig. 14 shows the efficiency curves according to the load conditions. The light load efficiency is reduced, while the parallel-connected SR number increases because of the increase in the driving loss. The maximum efficiency was measured with the 5x*SR* operation as 95% and 94.5% under half load and full load condition, respectively. The measured maximum efficiency is 5% higher than the efficiency of the diode-rectified ZVS-FB converter. The light load efficiency of the 3x*SR* and 4x*SR* operations is higher than that of the 5x*SR* operation. However, their full load efficiencies are lower than that of the 5x*SR* operation. As given in the theoretical prediction in Fig. 11, full load efficiency starts to decrease after the 5x*SR* operation. The efficiency values are slightly different from the theoretical calculations because the inductance on the gate line was assumed to be 28 nH for the calculation, and the inductance is not accurately known in the measurement.

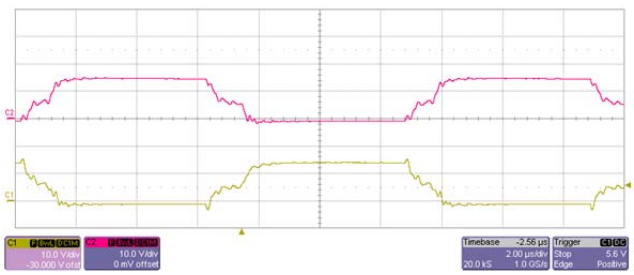
The gate voltage was measured for different R_g values, and the obtained results were compared in Fig. 15 to evaluate the series gate resistance effect on the gate voltage. The measurements were taken with the 5x*SR* operation and 82-Ω parallel resistor R_p. The increase in gate resistance extends the delay times and the body diode conduction time at the rising and falling edges. However, the increase in the gate resistance reduces the oscillation on the gate voltage, as



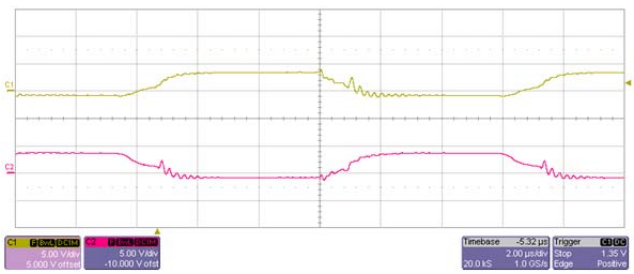
(a) 3x*SR*.



(b) 5x*SR*.



(c) 8x*SR*.



(d) 10x*SR*.

Fig. 13. Gate voltage waveforms of the SRs under full load condition: (a) 3x*SR* operation, (b) 5x*SR* operation, (c) 8x*SR* operation, and (d) 10x*SR* operation.

mentioned in the theoretical analysis.

To evaluate the series gate resistance effect on the efficiency, different R_g values were tested with the 5xSR operation, and the obtained results are given in Fig. 16. The low gate resistance provides the best efficiency at light load conditions because the gate drive loss decreases. However, the resistor lower than 2 Ω destroyed the gate of the SRs because of the undamped low-frequency oscillation on the gate voltage. Therefore, the best efficiency was safely measured with 3 Ω gate resistance in terms of light load efficiency.

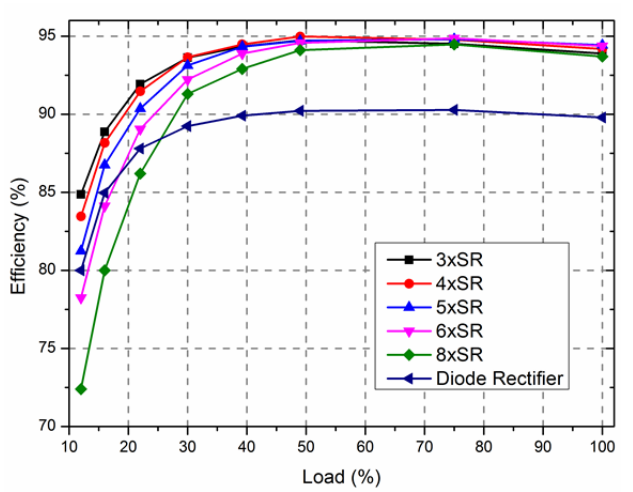
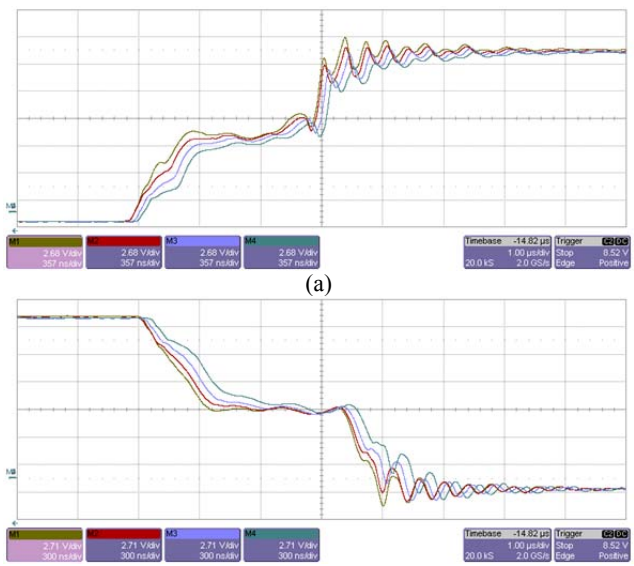


Fig. 14. Efficiency measurement according to the load condition.



(a)

(b)

Fig. 15. Gate voltage variation for different R_g values: (a) extended rising edge and (b) extended falling edge. M1: R_g=2 Ω, M2: R_g=3 Ω, M3: R_g=3.9 Ω, and M4: R_g=5.1 Ω.

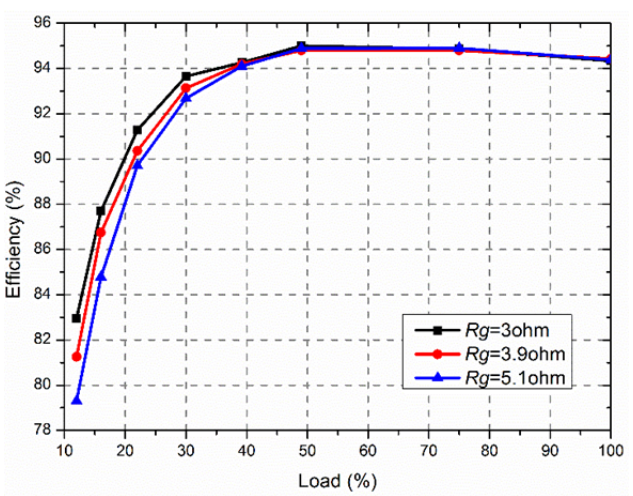
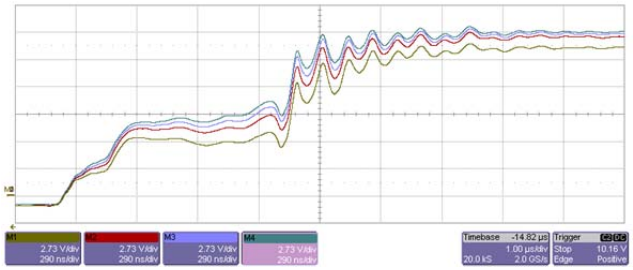


Fig. 16. Efficiency measurements as the function of R_g.


(a)

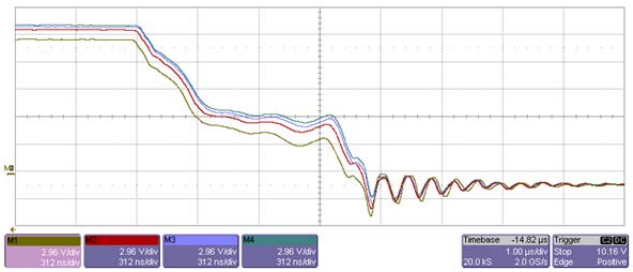

(b)

Fig. 17. Gate voltage variation for different R_p values: (a) extended rising edge and (b) extended falling edge. M1: R_p=22 Ω, M2: R_p=39 Ω, M3: R_p=59 Ω, and M4: R_p=82 Ω.

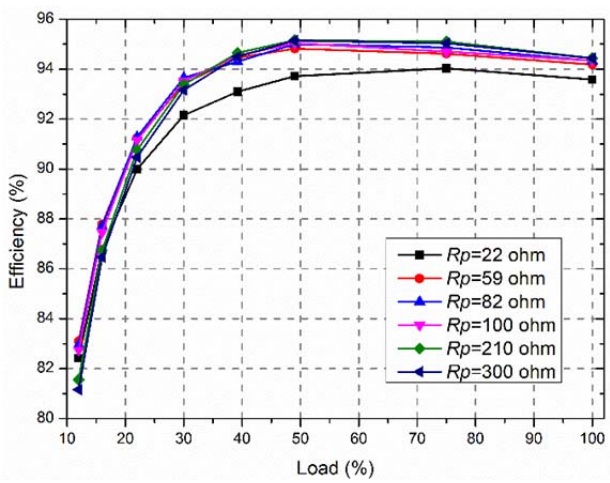


Fig. 18. Efficiency measurements as the function of R_p.

The effect of parallel resistor R_p on the gate voltage is shown in Fig. 17. The measurements were taken with the *5xSR* operation. The increase in R_p accelerates and delays the charge and discharge times of the gate–source capacitance, respectively. The measured efficiency evaluation was also performed based on R_p variation in Fig. 18. The best efficiency under the full load was measured with the highest value of R_p at 300 Ω. However, light load efficiency was lower with 300 Ω compared with lower values of R_p because the driving loss increases with the extended rising time under the light load condition. Values that are higher than 300 Ω did not further change the efficiency values and negatively affect the behavior of the gate voltage oscillation. The decrease in R_p reduces the efficiency because of the increase in driving loss. For values lower than 59 Ω, the decrease in efficiency is more prominent. Therefore, R_p can be selected between 82 Ω and 300 Ω, taking into consideration the wide load range efficiency. After the evaluation of R_p variation, R_p was selected as 82 Ω in the designed prototype to keep light load efficiency high.

The best efficiencies obtained after experimental optimization of the series gate resistor and the parallel resistor were 95.16% and 94.44% under half load and full load condition, respectively.

VI. Conclusion

An optimal design procedure of a ZVS-FB PWM DC–DC converter based on self-driven SR performance has been discussed. In the presented design approach, the operation of a self-driver was analyzed, taking into consideration the parallel combination of SRs to obtain maximum efficiency. According to the proposed analytical model, the best efficiency was obtained with the *5xSR* operation condition because a further increase in the number of the parallel-connected SRs extended the body diode conduction interval. The decrease in series gate resistor R_g improved the light load efficiency, but values lower than 2 Ω destroyed the gate terminals of the SRs. The light load efficiency of the converter was reduced, while R_g increased. The increase in R_p increased the efficiency slightly, while it reduced the light load efficiency slightly. For a value lower than 59 Ω, the decrease in efficiency was more prominent because of the increase in conduction losses in the self-driver. The proposed design approach is experimentally validated with a server power supply prototype, which has 12 V output voltage and 1 kW output power. The self-driver parameter optimization produced maximum efficiencies of 95.16% and 94.44% under half and full load conditions, respectively.

Acknowledgment

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