JPE 16-1-15

http://dx.doi.org/10.6113/JPE.2016.16.1.133
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Novel Five-Level Flying-Capacitor Dual Buck Inverter

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Abstract

This paper focuses on the development of a Five-Level Flying-Capacitor Dual Buck Inverter (FLFCDBI) based on the main circuit of dual buck inverters. This topology has been described as not having any shoot-through problems, no body-diode reverse recovery problems and the half-cycle work mode found in the traditional Multi-Level Flying-Capacitor Inverter (MLFCI). It has been shown that the flying-capacitor voltages of this inverter can be regulated by the redundant state selection within one pole. The voltage balance of the flying-capacitors can be achieved by charging or discharging in the positive (negative) half cycles by choosing the proper logical algorithms. This system has a simple structure but demonstrates improved performance and reliability. The validity of this inverter is conformed through computer-aided simulation and experimental investigations.

Key words: Balancing capacitor voltage, Dual buck, Five-level inverter, Flying-capacitor

I. INTRODUCTION

Multi-Level Inverters (MLI) have been attracting more and more attention in terms of renewable energy sources (i.e., photovoltaic, wind and fuel cells) due to their high power levels, low voltage stress, low THD of the output waveform, and low EMI phenomenon and losses. MLI systems are generally classified as diode-clamped, cascaded or Flying-Capacitor Inverters (FCI) [1]-[7]. For constructing a circit with the same number of levels, the number of required components can be quite depending on the inverter type. For example, to build a n-level circuit: (i) n-1 divider capacitors and (n-1)×(n-2) clamping diodes are required for a diode-clamped inverter; (ii) (n-1)/2 independent DC sources are needed for a cascade inverter; and (iii) n-1 divider capacitors and (n-1)×(n-2)/2 flying-capacitors are needed for an FCI inverter [7]-[9]. In other words, to construct a circuit with the same number of levels, a FCI needs only half the number of clamping devices that are needed for a diode-clamped inverter, and it does not require multiplex DC sources like the cascade inverter. Accordingly, Flying-Capacitor Inverters are easier to expand to multi-level inverters. However, Flying-Capacitor Inverters have a severe shoot-through problem when they are compared to the diode-clamped and cascade inverters. This problem will be analyzed in following sections. Several methods including stringently controlling the switching vector, banning the modes that lead to direct shooting-through, setting the dead-time [10], [11], eliminating the zero-current crossing problem [12], [13], keeping the devices efficient in the dead-time period to avoid a narrow-pulse [14], modifying the commanded converter terminal voltages [15]-[17], modifying the lengths of the gate-drive pulses in the modulator (pulse-based methods) [18], and eliminating the reverse recovery of the parasitic diodes of the transistors [8]. However, the drawback of these methods is that they add complexity to the systems. In this paper, a Five-Level Flying-Capacitor Dual Buck Inverter (FLFCDBI) is presented based on the dual buck inverter. The Multi-Level Flying-Capacitor Dual Buck Inverter and the proposed Five-Level Flying-Capacitor Dual Buck Inverter will be described in Section II. Voltage balancing will be analyzed in Section III. Control strategies will be introduced in Section IV. Simulation and experiment results will be presented in Section V and Section VI, respectively. Finally, some conclusions will be given in Section VII.

Manuscript received Jan. 28, 2015; accepted May 2, 2015.
Recommended for publication by Associate Editor Younghoon Cho.
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II. MULTI-LEVEL FLYING CAPACITOR DUAL BUCK INVERTER AND FIVE-LEVEL FLYING CAPACITOR DUAL BUCK INVERTER

Fig. 1 shows a traditional n-level FCI diagram in which shooting-through can easily take place [19]-[26]. Fig. 2 summarizes a shooting-through fault diagram of four short-circuits. Summing up, shoot-through can easily take place in the four short circuits, i.e., (i) input voltage sources and transistors (Fig. 2(a)), (ii) input voltage sources and flying-capacitors (Fig. 2(b)), (iii) flying-capacitors (Fig. 2(c)), and (iv) flying-capacitors and transistors (Fig. 2(d)).

The shoot-through problem that occurs in the traditional FCI can be avoided by using Dual Buck Inverters (DBIs). DBIs have the distinct merits of a half cycle work mode, no shoot-through problems, and no reverse-recovery of the parasitic diode of the switches [20]-[24]. Fig. 3(a) and (b) show the topology and waveforms of the DBI, respectively.

DBIs work in the positive or negative half cycle work modes. During the positive half cycles, Buck Circuit I works and the current of inductor L_1 (i_{L1}), which flows from transistor S_1 or freewheels from diode D_1, is above zero. During the negative half cycles, Buck Circuit II works and the current of inductor L_2 (i_{L2}), which flows from transistor S_2 or freewheels from diode D_2, is above zero. Therefore, in the half cycle work mode, there are no-loop currents, and the circuits can achieve more efficient and higher frequencies.

Two filtering inductors L_1 and L_2, which are in series, are connected to two switches S_1 and S_2, which eliminates the problem of shooting-through [21], [23]-[25], [27]-[28]. Due to this, all of the switch combinations can be used without setting the dead-time and the reliability of the system increases.

Fast Recovery Diodes (FRDs) D_1 and D_2 take the place of the parasitic diode of switches S_1 and S_2 which overcomes shortcomings such as too large a reverse recovery current, too long a reverse recovery time, and too much loss of the parasitic diode [20], [21], [23]-[25], and [28]. In addition, the efficiency can be improved, the frequency can be increased, and the volume and weight of the model can be decreased.

Furthermore voltage balancing of the flying-capacitor can be achieved by selecting proper redundant switch combinations to charge or discharge the flying-capacitors through proper logical algorithms.

Fig. 4 shows the topology of the Flying-Capacitor Dual Buck Multilevel Inverter (FCDBMLI), which is a combination of a FCI and a DBI. This topology has the benefits of both the FCI and the DBI.

Table I lists the number of components of the FCDBMLI. The switch number for n-levels is n+1 (when n is odd) or n (when n is even). Table II lists the number of components for a traditional FCI [9], [19], and [23]. The switch number of a n-level traditional FCI is 2(n-1). When n>3, the switch numbers of the FCDBMLI are obviously less than those of the traditional FCI. Thus, the FCDBMLI is more cost effective than the traditional FCI, especially when the number

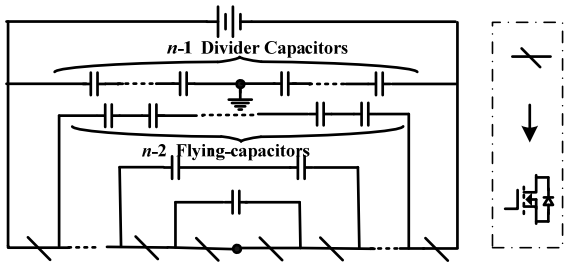


Fig. 1. Traditional n-level FCI.

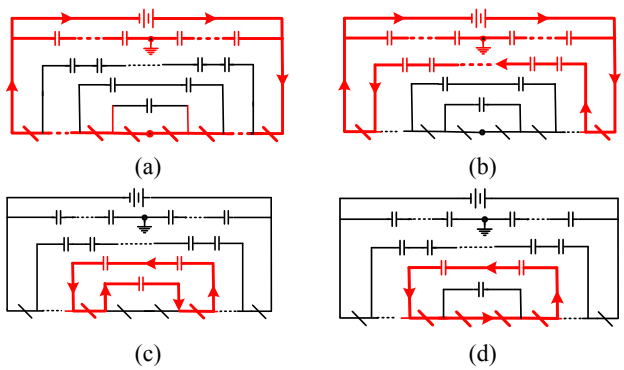


Fig. 2. Shooting-through fault diagram of traditional FCI showing short circuit of: (a) voltage sources and transistors, (b) voltage sources and flying-capacitors, (c) flying-capacitors, and (d) flying-capacitors and transistors.

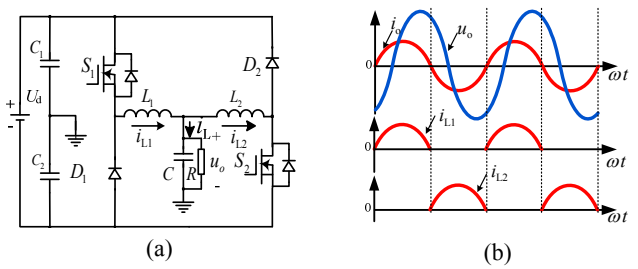


Fig. 3. (a) topology of Dual buck half bridge inverter and (b) waveforms of dual buck half bridge inverter in half period work mode.

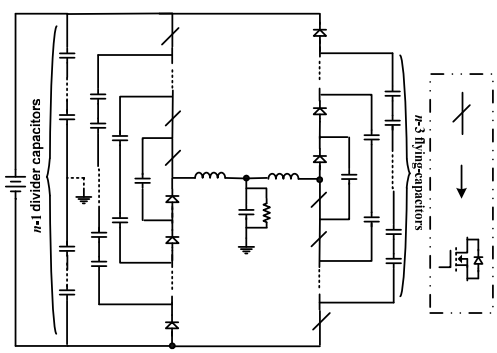


Fig. 4. N-level FCDBMLI.

of output levels is greater than three.

Fig. 5 shows the topology of the FLFCDBI. As mentioned earlier, the FCDBMLI is based on a DBI. Buck Circuit I consists of S_{11}, S_{12}, S_{13}, D_{11}, D_{12}, D_{13}, C_{11}, C_{12}, and L_1. Buck

Circuit II consists of S_{21}, S_{22}, S_{23}, D_{21}, D_{22}, D_{23}, C_{21}, C_{22}, and L_2.

The modes of the FLFCDBI will be discussed together with the sequence diagram (Fig. 6), working mode diagrams (Fig. 7) and transformation diagram of the modes (Fig. 8).

To commence with the analysis, the following assumptions are made:

a. All of the diodes and switches are ideal;

b. All of the capacitors and inductors are ideal;

c. $L_1 = L_2 = L$.

When the output current i_L is above zero ($i_L \geq 0$, $i_L = i_{L1} - i_{L2}$), the circuit works in the positive half cycle, which corresponds to the region $[t_0, t_4]$ in Fig. 6. When Buck Circuit I works, Buck Curcuit II does not work. The switch combinations(Mode I-0~Mode I-7) are shown in Table III.

1) Mode I-0 (Fig. 7(a)): S_{11}, S_{12} and S_{13} are OFF, i_{L1} freewheels from D_{11}, D_{12} and D_{13}, and the flying-capacitors C_{11} and C_{12} neither charge nor discharge. The voltage of pole ① is $-U_d/2$. In this mode:

$$\frac{di_{L1}}{dt} = \frac{1}{L}(-\frac{1}{2}U_d - u_o) \tag{1}$$

2) Mode I-1 (Fig. 7(b)): S_{13} is ON, S_{11} and S_{12} are OFF, i_{L1} freewheels from D_{11} and D_{12}, and the flying-capacitor C_{12} discharges. The voltage of pole ① is $-U_d/4$. In this mode:

$$\frac{di_{L1}}{dt} = \frac{1}{L}(-\frac{1}{4}U_d - u_o) \tag{2}$$

3) Mode I-2 (Fig. 7(c)): S_{12} is ON, S_{11} and S_{13} are OFF, i_{L1} freewheels from D_{11} and D_{13}, and the flying-capacitors C_{11} and C_{12} discharge. The voltage of pole ① is $-U_d/4$. In this mode:

$$\frac{di_{L1}}{dt} = \frac{1}{L}(-u_o) \tag{3}$$

4) Mode I-3 (Fig. 7(d)): S_{12} and S_{13} are ON, S_{11} is OFF, i_{L1} freewheels from D_{13}, and the flying-capacitor C_{11} discharges. The voltage of pole ① is 0. In this mode:

$$\frac{di_{L1}}{dt} = \frac{1}{L}(-\frac{1}{4}U_d - u_o) \tag{4}$$

5) Mode I-4 (Fig. 7(e)): S_{11} is ON, S_{12} and S_{13} are OFF, i_{L1} freewheels from D_{11} and D_{12}, and the flying-capacitor C_{11} charges. The voltage of pole ① is 0. In this mode:

$$\frac{di_{L1}}{dt} = \frac{1}{L}(\frac{1}{4}U_d - u_o) \tag{5}$$

6) Mode I-5 (Fig. 7(f)): S_{11} and S_{13} are ON, S_{12} is OFF, i_{L1} freewheels from D_{12}, the flying-capacitor C_{11} charges, and the flying-capacitor C_{12} discharges. The voltage of pole ① is $U_d/4$. The current i_L increases. In this mode:

$$\frac{di_{L1}}{dt} = \frac{1}{L}(\frac{1}{2}U_d - u_o) \tag{6}$$

7) Mode I-6 (Fig. 7(g)): S_{11} and S_{12} are ON, S_{13} is OFF, i_{L1} freewheels from D_{11}, and the flying-capacitor C_{12} charges.

The voltage of pole ① is $U_d/4$. In this mode:

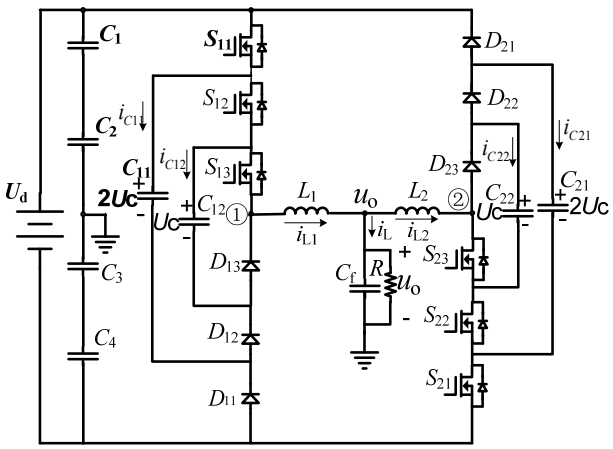


Fig. 5. Topology of FLFCDBI.

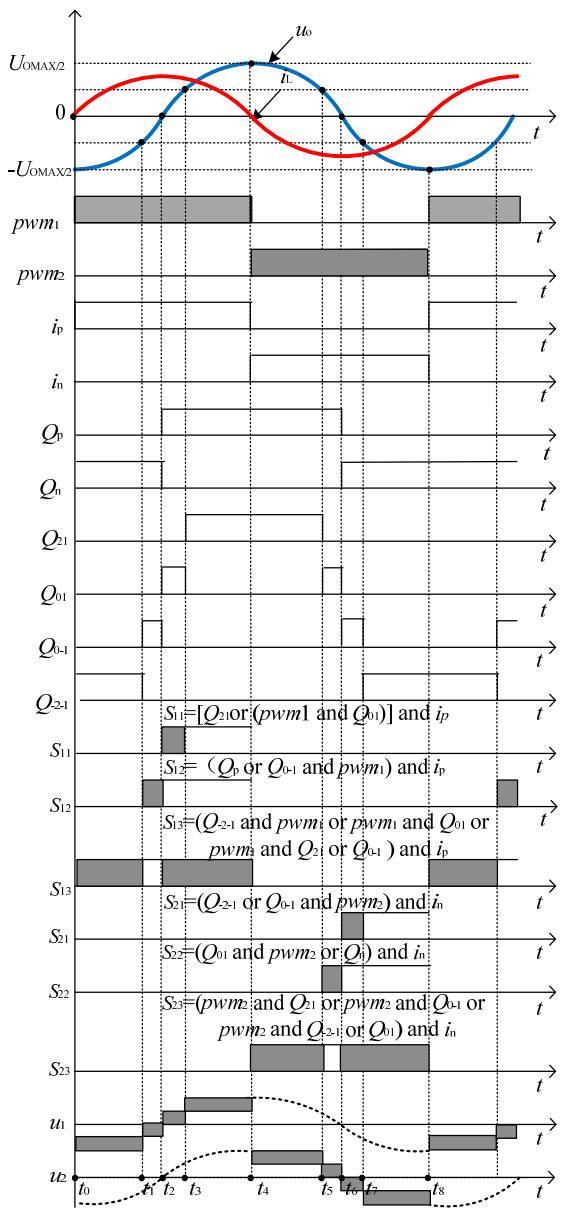


Fig. 6. Sequence diagram of FLFCDBI.

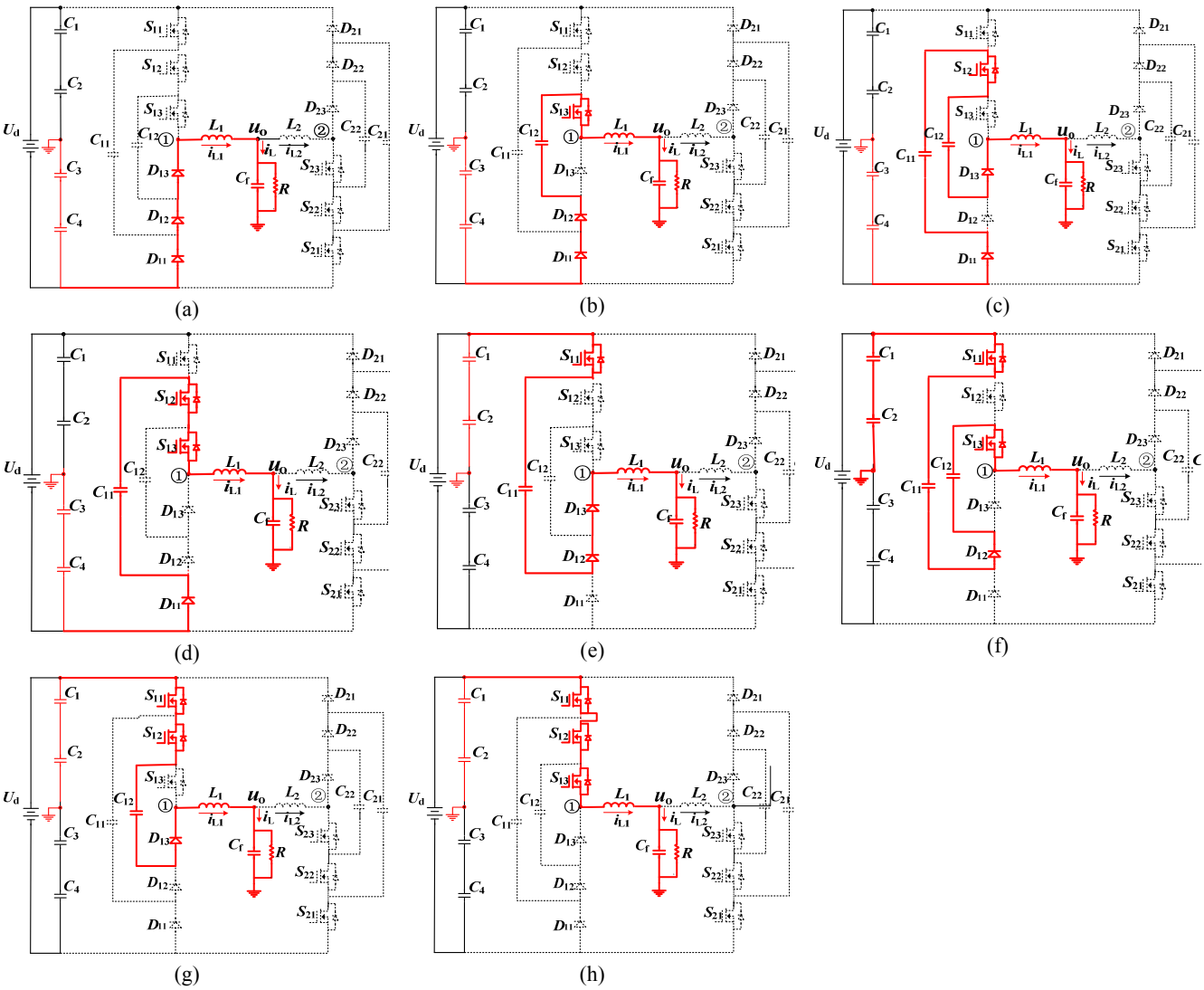


Fig. 7. Working modes of FLFCDBI: (a) Mode I-0, (b)Mode I-1, (c) Mode I-2, (d) Mode I-3, (e) Mode I-4, (f) Mode I-5, (g) Mode I-6, and (h) Mode I-7.

TABLE I
SWITCH SCHEME AT POSITIVE HALF CYCLE

Output level	Cell number	Flying-capacitor number	Transistor number	Switch array states number
3	2	2	4	2^3=8
4	2	2	4	2^3=8
5	4	6	6	2^4=16
6	4	6	6	2^4=16
⋮	⋮	⋮	⋮	⋮
n（odd）	$n-1$	$\frac{(n-1)(n+1)}{4}$	$n+1$	$2^{\frac{n+3}{2}}$
n（even）	$n-1$	$\frac{n(n-2)}{4}$	n	$2^{\frac{n+2}{2}}$

TABLE II
TRADITIONAL FCI COMPONENTS

Output level	Cell number	Flying-capacit or number	Transistor number	Switch array states number
3	1	1	4	2^3=8
4	2	3	6	2^3=8
5	3	6	8	2^4=16
⋮	⋮	⋮	⋮	⋮
n	$n-2$	$\frac{(n-1)(n-2)}{2}$	$2(n-1)$	2^{n-1}

$$\frac{di_{L1}}{dt}=\frac{1}{L}(\frac{1}{4}U_d-u_o) \tag{7}$$

8) Mode I-7 (Fig. 7(h)): S_{11}, S_{12} and S_{13} are ON, D_{11}, D_{12} and D_{13} turn OFF, and the flying-capacitors C_{11} and C_{12} neither charge nor discharge. The voltage of pole ① is $U_d/2$. In this mode:

$$\frac{di_{L1}}{dt}=\frac{1}{L}(\frac{1}{2}U_d-u_o) \tag{8}$$

TABLE III
SWITCH SCHEME AT POSITIVE HALF CYCLE

Mode	S_{11}	S_{12}	S_{13}	C_{11}	C_{12}	u_1
I-0	0	0	0	×	×	$-U_d/2$
I-1	0	0	1	×	-	$-U_d/4$
I-2	0	1	0	-	+	
I-3	0	1	1	-	×	0
I-4	1	0	0	+	×	
I-5	1	0	1	+	-	$+U_d/4$
I-6	1	1	0	×	+	
I-7	1	1	1	×	×	$+U_d/2$

When the output current i_L is less than zero, the circuit works in the negative half cycle, which corresponds to the region [t_4, t_8] (Fig. 6). When Buck Circuit II functions, Buck Circuit I does not function. The work modes of the negative half cycles are opposite those of the positive half cycles.

III. FLYING-CAPACITOR VOLTAGE CONTROL

The voltage balancing of flying-capacitors is the key technology of this topology. It can be achieved by the charging or discharging of the flying-capacitors through choosing proper logical algorithms.

As shown in Fig. 5, x represents pole ① or ②. α_{xm} represents the mth switch state of the pole. α_{xm}=1, if the switch is ON; and α_{xm}=0, if it is not. I_{Cxn} represents the current of the nth flying-capacitor of the xth pole. I_{Lx} represents the current of the xth filtering inductor. The expressions of the current of the flying-capacitor are as shown below:

$$I_{Cx1} = (\alpha_{x1} - \alpha_{x2}) I_{Lx} \tag{9}$$

$$I_{Cx2} = (\alpha_{x2} - \alpha_{x3}) I_{Lx} \tag{10}$$

The differential equations of the voltages of the flying-capacitors are as shown below:

$$\frac{dU_{Cx1}}{dt} = \frac{I_{Lx}}{C_{x1}}(\alpha_{x1} - \alpha_{x2}) \tag{11}$$

$$\frac{dU_{Cx2}}{dt} = \frac{I_{Lx}}{C_{x2}}(\alpha_{x2} - \alpha_{x3}) \tag{12}$$

$$\Delta U_{Cx1} = \frac{1}{C_{x1}} \int (\alpha_{x1} - \alpha_{x2}) i_{Lx} dt \tag{13}$$

$$\Delta U_{Cx2} = \frac{1}{C_{x2}} \int (\alpha_{x2} - \alpha_{x3}) i_{Lx} dt \tag{14}$$

If the equations hold during a period:

$$\int (\alpha_{x1} - \alpha_{x2}) i_{Lx} dt = 0 \tag{15}$$

$$\int (\alpha_{x2} - \alpha_{x3}) i_{Lx} dt = 0 \tag{16}$$

The voltage balancing of the flying-capacitors C_{11} and C_{12} can be realized.

There are redundant transferring modes corresponding to each of the four regions of the output voltage u_o, [$-U_{omax}/2$, $-U_{omax}/4$], [$-U_{omax}/4$, 0], [0, $U_{omax}/4$], and [$U_{omax}/4$, $U_{omax}/2$]. Table 3 lists the switch combinations termed as Mode I-0 - Mode I-7, and the corresponding charging state of the flying capacitors in the positive half cycle ($i_L \geq 0$). The value "1" indicates the closing state of the switches (S_{11}, S_{12}, and S_{13}) and "0" indicates the closing state. The charging state of the flying-capacitors is indicated by "+", the discharging state of the flying capacitors is indicated by "-", and "×" indicates neither the charging nor discharging states. Fig. 8 reveals every transferring mode corresponding to each of the four regions at the positive half circle.

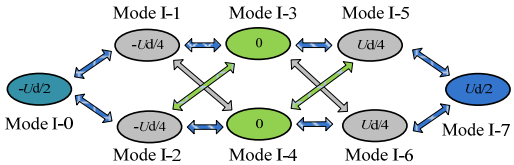


Fig. 8. Transformation of modes.

TABLE IV
SWITCH SCHEME AT POSITIVE HALF CYCLE

Mode	S_{11}	S_{12}	S_{13}	C_{11}	C_{12}	u_1
I-0	0	0	0	×	×	$-U_d/2$
I-1	0	0	1	×	-	$-U_d/4$
I-2	0	1	0	-	+	
I-3	0	1	1	-	×	0
I-4	1	0	0	+	×	
I-5	1	0	1	+	-	$+U_d/4$
I-6	1	1	0	×	+	
I-7	1	1	1	×	×	$+U_d/2$

TABLE V
CHARGING STATES OF FLYING-CAPACITOR C_{11}

Mode	S_{11}	S_{12}	S_{13}	C_{11}	C_{12}	u_1
I-0	0	0	0	×	×	$-U_d/2$
I-1	0	0	1	×	-	$-U_d/4$
I-4	1	0	0	+	×	0
I-6	1	1	0	×	+	$+U_d/4$
I-7	1	1	1	×	×	$+U_d/2$

Since there is no transferring mode that can be implemented in the period of the four regions for achieving a voltage balance of C_{11} and C_{12} at the same time in the positive half cycle ($i_L \geq 0$), two switch groups of charging (Table IV) and discharging of flying-capacitors C_{11} (Table V) are grouped. In each of the two groups, the voltage of C_{12} satisfies (16). The two groups are used to ensure that the voltage balance of these two components is done simultaneously by a hysteresis comparator with a threshold of (Δh). The logical circuit of the discharging C_{11} is pitched on, while v_{C11} (the voltage of C_{11}) is above $U_d/2+\Delta h$ (U_d is the dc-link voltage). Then v_{C11} begins to decrease. The logical circuit of the charging C_{11} is pitched on, while v_{C11} is below $U_d/2-\Delta h$. Then v_{C11} begins to increase. While v_{C11} is between [$U_d/2-\Delta h$, $U_d/2+\Delta h$], the logical circuit does not switch to

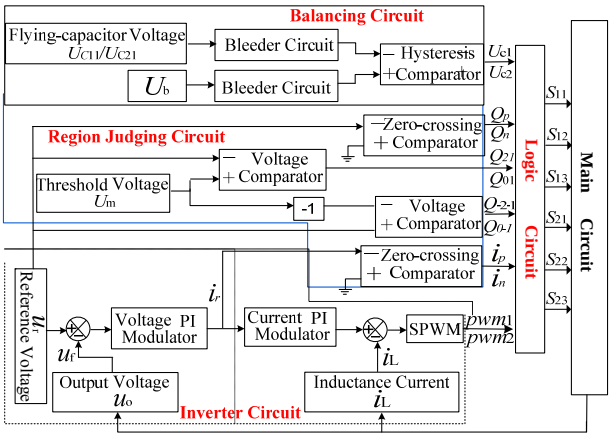


Fig. 9. Control block diagram.

another circuit. This way, the voltage of C_{11} satisfies (15). Therefore, C_{11} and C_{12} can realize voltage balancing during a full cycle.

In the negative half period (i_L<0), the flying-capacitors C_{21} and C_{22} can realize the voltage balancing. These principles and methods are similar to those of the positive half cycle.

IV. Control Strategy

According to the principles of the inverting and balancing of the flying-capacitor voltage of the FLFCDBI, the control

block diagram is divided into four sections: the inverter circuit, region judging circuit, voltage balancing circuit, and logic circuit (Fig. 9).

The inverter circuit: the control strategy adopts a two-loop system (both of the loops are PI loops): an external voltage loop and an inner current loop. The outputs of the two loops intersect on a triangular wave and generate the SPWM signals pwm_1 and pwm_2.

The region judging circuit: the sinusoidal signal u_r is the voltage reference signal. i_r is the signal of the output of the voltage loop and it is also the current reference signal. u_r (i_r) is compared through the zero-crossing comparator and generates Q_p (i_p), which indicates the positive or negative features of u_r (i_r). u_r is compared with $\pm U_m$ (U_m=u_r/2) and generates the signals of Q_{-2-1}, Q_{0-1}, Q_{10} and Q_{21}, which correspond to the regions of $-2U_m \le u_r \le -U_m$, $-U_m \le u_r \le 0$, $0 \le u_r \le U_m$, and $U_m \le u_r \le 2U_m$, respectively.

The voltage balancing circuit: the flying-capacitor voltage U_{c11} (U_{c21}) is compared with $U_b \pm \Delta h$ ($U_b = U_d/2$) through the bleeder comparator and the hysteresis comparator and generates U_{c1} (U_{c2}), which indicates the charging or discharging features of the flying-capacitor C_{11} (C_{21}). Therefore, the charging or discharging mode can be chosen in the current positive half cycle or the current negative half cycle and realize the voltage balancing of the flying-capacitor occurs.

All of the signals created above are sent through a logic circuit and generate the signals of the switches S_{11}, S_{12}, S_{13}, S_{21}, S_{22} and S_{23}. These switch functions, which are included in Fig. 6, are expressed at the discharging states of C_{11} and C_{21}. They control the switches in the main circuit as show in Fig. 5. As illustrated in Fig. 6, the SPWM waves u_1 and u_2 are the outputs of poles ① and ②. They indicate the five-level output voltages and the voltage balancing of the flying-capacitor, and are synthesized into the sinusoidal wave u_o after the filtering circuit.

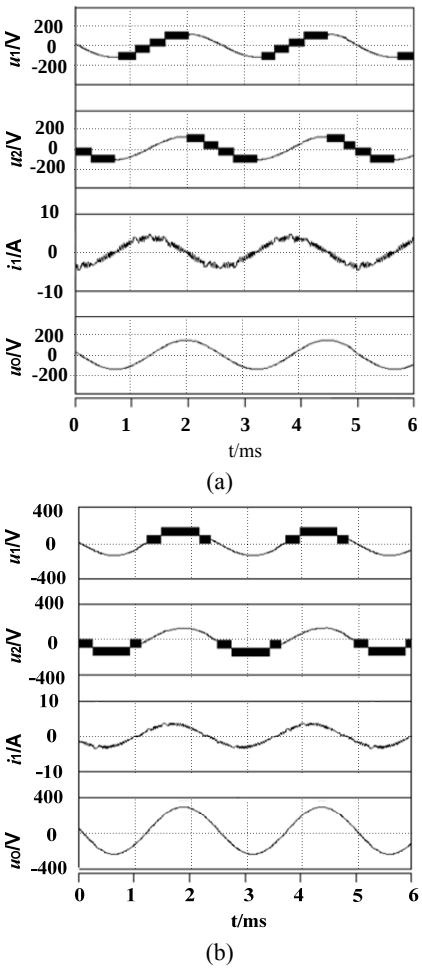


Fig. 10. (a) no load waveforms of simulation and (b) full load waveforms of simulation.

V. Simulation Result

To test the schematics, SABER Simulation software was used to simulate the topology of the FLFCDBI. The conditions were as follows: the input DC voltage was ±180V, the output voltage was 110V/400Hz, the unit flying-capacitor was C=470μF, the output filter capacitor was C_f =10μF, the output filter inductor was L_1= L_2=100μH, and the output resistance was 50Ω. Fig. 10 illustrates the simulation waves at the no-load and full-load conditions. u_1 is the voltage of pole ①, u_2 is the voltage of pole ②, i_L is the inductor current, and u_o is the output voltage.

In the case of the steady state, the circuit works at the half cycle work mode. Fig. 10(a) reveals waveforms at the no-load condition. These waveforms show that the voltage phase is lagged behind the current phase by exactly 90°. In the positive half cycle, the output voltage u_o rises, Buck Circuit I functions, and the output voltage of pole ① has five levels: $\pm U_d/2$, $\pm U_d/4$, and 0. Buck Circuit II does not function, i_{L2} is zero, and the voltage of pole ② u_2 is u_o. In the negative half cycle, the output voltage falls, Buck Circuit II functions, and the output voltage of pole ② has five levels: $\pm U_d/2$, $\pm U_d/4$, and 0. Buck Circuit I does not function, i_{L1} is zero, and the voltage of pole ① u_1 is u_o.

Fig. 10(b) reveals the waveforms at the full-load condition. The current phase of the inductor almost conforms to the voltage phase. In the positive half cycle, the output voltage is above zero, and the voltage of pole ① has three levels: $U_d/2$, $U_d/4$ and 0. In the negative half cycle, the output voltage is less than zero, and the voltage of pole ② has three levels: $-U_d/2$, $-U_d/4$ and 0. This simulation is in accordance with the principles and methods analyzed above.

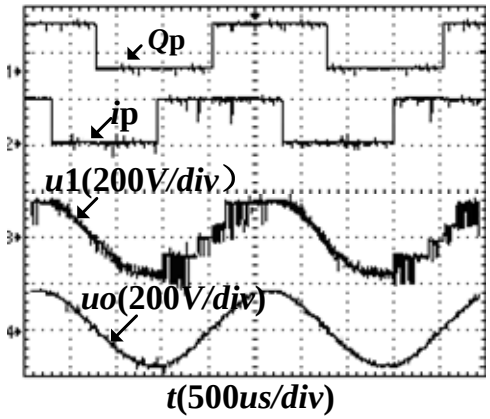
VI. Laboratory Validation

An experimental prototype was built in the laboratory to verify the actual performance of the FLFCDBI. The parameters were as follows: the input DC voltage was ±180V, the output voltage was 110V/400Hz, the rated power was 1000W, the unit flying-capacitor was C=470μF, the output filter capacitor was C_f =10μF, and the output filter inductor was L_1= L_2=100μH. Power MOSFETs (IRFP460) were used for the controllable switching devices (S_{11}, S_{12}, S_{13}, S_{21} S_{22}, and S_{23}). DSEI60-06A power diodes were used for D_{11}, D_{12}, D_{13}, D_{21}, D_{22}, and D_{23}.

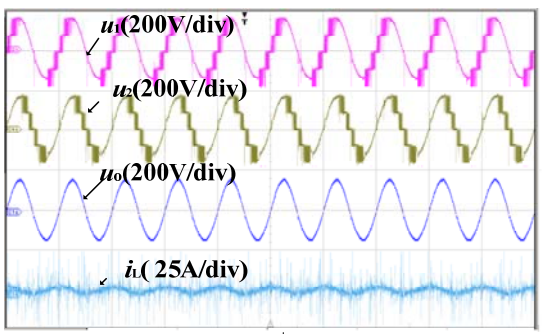
In the steady state, the circuit works in the half cycle work modes. Fig. 11(a) and (b) reveal the waveforms at the no-load condition. The signal of Q_p indicates the positive or negative features of u_o. The signal of i_p indicates the positive or negative features of i_L. *ch*3 of Fig. 11(a) is the pole voltage u_1, *ch*4 of Fig. 11(a) and *ch*3 of Fig. 11(b) are the output voltage u_o, and *ch*4 of Fig. 11(b) is the inductor current i_L. The waveforms of Q_p and i_p show the voltage phase lags behind the current phase by 90°. In the positive half cycle (i_p=1), the output voltage rises, Buck Circuit I functions, and the output voltage of pole ① has five levels: ±Ud/2, ±Ud/4, and 0.

In the negative half period, the output voltage falls, Buck Circuit II functions, and the output voltage of pole ② has five levels: $\pm U_d/2$, $\pm U_d/4$, and 0. Buck Circuit I does not function, i_{L1} is zero, and the voltage of pole ① u_1 is equal to u_o.

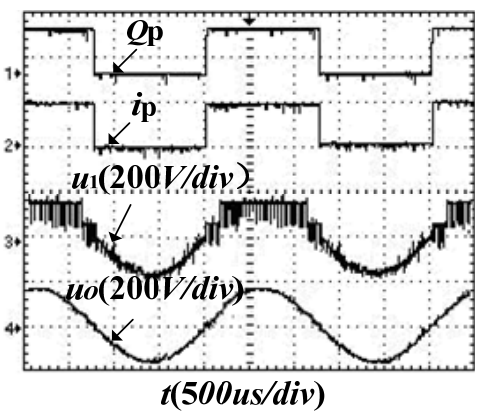
Fig. 11(c) and (d) reveal the waveforms at the full-load condition. Q_p, indicates the positive or negative features of u_o.



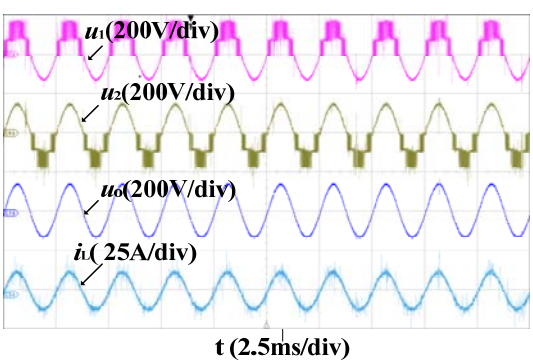
(a)



(b)



(c)



(d)

Fig. 11. (a), (b) no-load waveforms of experiment and (c), (d)full-load waveforms of experiment.

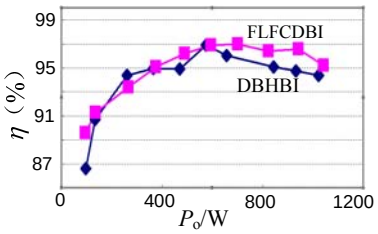


Fig. 12. Efficiency curves.

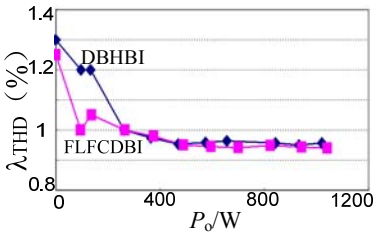


Fig. 13. THD curves.

i_p indicates the positive or negative features of i_L. *ch*3 of Fig. 11(c) and *ch*1 of Fig. 11(d) are the pole voltage u_1, and *ch*4 of Fig. 11(c) and *ch*3 of Fig. 11(d) are the output voltage u_o. The waveforms of Q_p and i_p indicate that voltage has the same phase as the current. The four sections of u_1 are even, the point of zero of u_1 is correct, and balancing of the voltage is realized. The experimental waveforms are in accordance with the simulated waveforms.

In order to compare it with the FLFCDBI, a prototype of the dual buck half bridge inverter (DBHBI) had been built. It had the same input, output and rated power as the FLFCDBI.

The differences between them are the parameters of the output filter capacitor and filter inductors: C_f=22μF, L_1=L_2=400μH. Efficiency curves are shown in Fig. 12, and the FLFCDBI was shown to be more efficient. The total harmonic distortion (THD, using the symbol λ_{THD}) of the output voltage u_o was shown in Fig. 13. The λ_{THD} values of the two inverters were similar. The performance of the FLFCDBI was better, and as mentioned above in the analysis, the volume of the filter was reduced.

VII. Conclusion

In this paper, a theoretical analysis, simulations and experiments verified that the FLFCDBI maintained the merits associated with the DBI. Merits such as having no shoot-through problems, no parasitic diode reverse-recovery time, and functioning in the half cycle work modes, are achieved for the five-levels of the output voltages. In addition, the balancing of the voltage of the flying-capacitors was also achieved. Compared with the traditional multilevel inverter, the inverter is more reliable and is suitable for the aeronautics and astronautics field with its demand for high power. In addition, it promises a good application future in the field of reactive compensation, motor drives, new energy power generation, high-power supplies, active filters, etc. Furthermore, the input and the output share the same ground. Therefore, three FLFCDBI are convenient for interfacing with the same input DC source to construct a three-phase system. The three-phase FLFCDBI, and the single-phase FLFCDBI, has the merits of no shoot-through problem, non-body-diode reverse recovery problem and half-period work mode compared with the traditional three-phase half bridge flying capacitor clamped inverter.

Acknowledgment

This work was supported in part by the National Nature Science Foundation of China under Grant 51407089.

References

[1] F. Z. Peng, “A generalized multilevel inverter topology with self voltage balancing,” *IEEE Trans. Ind. Appl.*, Vol. 37, No. 2, pp. 611-618, Mar./Apr. 2001.

[2] J. Rodríguez, J. S. Lai, and F. Z. Peng, “Multilevel inverters: A survey of topologies, controls, and applications,” *IEEE Trans. Ind. Electron*., Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[3] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. E. H. Benbouzid, “Hybrid cascaded H-bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications,” *IEEE Trans. Ind. Electron*., Vol. 57, No. 3, pp. 892-899, Mar. 2010.

[4] C. Cecati, F. Ciancetta, and P. Siano, “A multilevel inverter for photovoltaic systems with fuzzy logic control,” *IEEE Trans. Ind. Electron*., Vol. 57, No. 12, pp. 4115-4125, Dec. 2010.

[5] M. F. Escalante, J. C. Vannier, and A. Arzande, “Flying capacitor multilevel inverters and DTC motor drive applications,” *IEEE Trans. Ind. Electron*., Vol. 49, No. 4, pp. 809-815, Aug. 2002.

[6] P. W. Sun, C. Liu, J. S. Lai, and C. L. Chen, “Cascade dual buck inverter with phase-shift control,” *IEEE Trans. Power Electron.*, Vol. 27, No. 4, pp. 2067-2077, Apr. 2012.

[7] X. M. Yuan and I. Barbi, “Fundamentals of a new diode clamping multilevel inverter,” *IEEE Trans. Power Electron.*, Vol. 15, No.4, pp. 711-718, Jul. 2000.

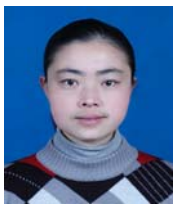
[8] W. Yang, F. Hong, and C. H. Wang, “A Novel Dual Buck Half Bridge Five-level Inverter,” in *Proc. the Chinese Society of Electrical Engineering*, Vol. 31, No. 24, pp. 19-25, 2011.

[9] M. B. Smida and F. B. Ammar, “Modeling and DBC-PSC-PWM control of a three-phase flying-capacitor stacked multilevel voltage source inverter,” *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2231-2239, Jul. 2010.

[10] S. Jin and Y. R. Zhong, “Novel three-level SVPWM algorithm considering neutral-point control and narrow-pulse elimination and dead-time compensation,” in *Proc. the Chinese Society of Electrical Engineering*, Vol. 25, No. 6, pp. 60-66, Jun. 2005.

[11] S. R. Minshull, C. M. Bingham, D. A. Stone, and M. P. Foster, “Compensation of Nonlinearities in Diode-clamped

Multilevel Converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2651-2658, Aug. 2010.
[12] D. L. Liu, R. B. Wu, and Y. Zhang, "Inverter dead time compensation of zero current clamping based on fuzzy control," in *Transactions of China Electrotechnical Society*, Vol. 26, No. 8, pp. 119-124, 2011.
[13] L. Liu and M. G. Deng, "A new approach of dead-time compensation for voltage-fed PWM inverter," *in 2011 International Conference on Electric Information and Control Engineering*, pp. 1039-1042, Apr. 2011.
[14] F. Gao, J. H. Yuan, D. Li, P. C. Loh, and H. L. Gao, "Dead-time elimination and zero common mode voltage operation of neutral-point-clamped inverter," in *8th International Conference on Power Electronics and ECCE Asia*, pp.2880-2885, May/Jun. 2011.
[15] B. B. Lazhar, "On the compensation of dead time and zero-current crossing for a PWM-inverter-controlled AC servo drive," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 5, pp. 1113-1117, Oct. 2004.
[16] D. S. Zhou and D. G. Rouaud, "Dead-time effect and compensations of three-level neutral point clamp inverters for high-performance drive applications," *IEEE Trans. Power Electron.*, Vol. 14, No. 4, pp. 782-788, Jul. 1999.
[17] G. L. Wang, D. G. Xu, and Y. Yuet, "A novel strategy of dead-time compensation for PWM voltage-source inverter," in *23rd Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 1779-1783, Feb. 2008.
[18] M. Liu and F. Hong, "FPGA controlled dual buck half bridge three-level inverter," in *Proc. the 2012 9th International Bhurban Conference on Applied Sciences & Technology (IBCA5T)*, pp: 83-86, Jan. 2012.
[19] C. H. Zhu, F. H. Zhang, and Y. G. Yan, "A novel split phase dual buck half bridge inverter," in *Applied Power Electronics Conference and Exposition*, Vol. 2, pp. 845-849, Mar. 2005,.
[20] M. Liu, F. Hong, and C. H. Wang, "Three-level dual buck inverter with coupled-inductance," in *Asia-Pacific Power and Energy Engineering Conference*, pp. 1-4, Mar. 2010.
[21] Z. L. Yao, L. Xiao, and Y. G. Yan, "Control strategy for series and parallel output dual-buck half bridge inverters based on DSP control," *IEEE Trans. Power Electron*., Vol. 24, No. 2, pp. 434-444, Feb. 2009.
[22] F. Hong, M. Liu, B. J. Ji, and C. H. Wang, "A Capacitor Voltage Buildup Method for Flying Capacitor Multilevel Inverters," in *Proc. the Chinese Society of Electrical Engineering*, Vol. 32, No.6, pp. 17-23, 2012.
[23] F. Hong, R. Z. Shan, H. Z. Wang, and Y. G. Yan, "A novel dual buck inverter with integrated magnetic," in *Transactions of China Electrotechnical Society*, Vol. 22, No. 6, pp. 76-81, 2007.
[24] P. Lezana, R. Aguilera, and D. E. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Trans. Ind. Electron*., Vol. 56, No. 6, pp. 1839-1846, Jun. 2009.
[25] A. Shukla, A. Ghosh, and A. Joshi, "Flying-capacitor-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter," *IEEE Trans. Ind. Electron*., Vol. 57, No. 7, pp. 2249-2261, Jul. 2010.
[26] J. Liu and Y. G. Yan, "Novel current mode controlled bi-buck half bridge inverter," *Journal of Nanjing University of Aeronautics & Astronautics*, Vol. 35, No. 2, pp. 122-126, 2003.



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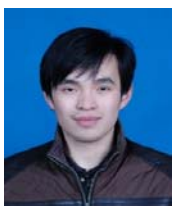

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