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# Modulation, Harmonic Analysis, and Balancing Control for a New Modular Multilevel Converter

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## Abstract

The modular multilevel converter (MMC) has been receiving increased attentions in recent years. The new modular multilevel converter is a derivative topology from the traditional MMC in which the number of sub-modules (SMs) necessitated by each phase can be reduced by one. This paper presents a phase-shifted carrier pulse-width modulation (PSC-PWM) for the new MMC with an optimal phase-shifted angle to suppress the harmonics of the output voltage. Further, the harmonic features when the capacitor voltage of the middle SM is selected as two different values are also investigated. Moreover, in order to avoid introducing an unnecessary dc offset current at the ac terminals of the new MMC, a novel capacitor voltage balancing scheme is proposed by adjusting the amplitude of the reference signals rather than the offset. Finally, the validity and effectiveness of the proposed modulation and balancing schemes have been verified by experimental results based on a three-phase prototype of the new MMC.

**Key words:** Modular multilevel converter (MMC), Phase-shifted carrier modulation, Voltage balancing

## I. INTRODUCTION

Due to the rapid growth of electricity consumption and large-scale utilization of renewable energy, multilevel converters are playing increasingly important roles in industrial applications due to their advantages in terms of high efficiency, low EMI noise, good harmonic features, and the ability to withstanding high voltage via low-voltage devices [1]-[10]. In 2000, a generalized multilevel converter was proposed, as shown in Fig. 1(a), which presented a generalized concept for multilevel converters [5]. Many of the existing multilevel converters (e.g., the well-known neutral-point clamped converter (NPC) and the flying-capacitor (FC) converter) were derived from this topology [6]-[10].

Another recently introduced multilevel converter called the modular multilevel converter (MMC) is depicted in Fig. 1(b), which is cascaded by a series of half-bridge sub-modules (SMs). Compared with other multilevel converters, the MMC shows higher modularity and scalability and can be applied to very high-voltage applications (i.e. HVDC) [11], [12].

In addition, in [9] and [10], a new multilevel topology (see Fig. 1(c)) was proposed by conserving the shadowed devices in Fig. 1(a). This topology was referred to as a new MMC (N-MMC) by the authors, and the only difference between it and the traditional MMC is the introduction of a middle SM. As a result, compared with the traditional MMC, the N-MMC is able to save one SM per phase while providing the same output voltage. However, due to the employment of the middle SM, the symmetry between the upper-arm and lower-arm SMs is no longer satisfied. The modulation schemes and capacitor voltage balancing methods used in the traditional MMC [11]-[20] are not applicable to the N-MMC. In [9] and [10], a phase-disposition carrier PWM (PD-PWM) as well as a voltage

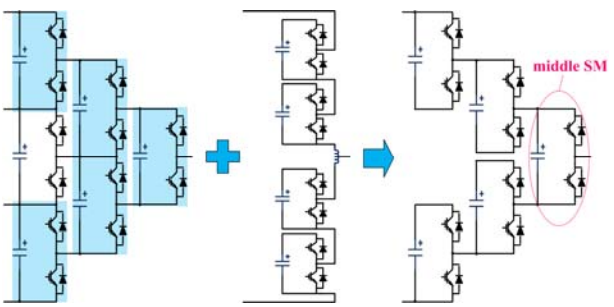


Fig. 1. Relationship of three multilevel converters: (a) Generalized multilevel converter, (b) Traditional MMC, and (c) New MMC.

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balancing method based on a sorting algorithm were proposed.

However, it has to be admitted that there are still some flaws:

- The switching frequencies of each SM are not identical under the PD-PWM, which leads to unequal distribution of the losses and heat dissipation among the semiconductors.
- The sorting calculations lead to a very heavy computational burden for the digital controller especially when the number of SMs is large.
- As a result of the balancing method, the middle SM may superpose a harmful dc offset current on the ac terminals.

Therefore, this paper proposes a novel phase-shifted carrier (PSC) modulation scheme for the N-MMC, with the advantages of optimized harmonic features and evenly distributed switching frequency and power losses. Moreover, a novel capacitor voltage balancing control scheme is further presented for the PSC-PWM, in which the unwanted dc offset current can be avoided. In addition, the complexity of the control system can be reduced since the centralized sorting calculation is replaced by a series of individual proportional controllers.

The rest of this paper is organized as follows. The mathematical model of the N-MMC is reviewed in Section II. A PSC modulation scheme for the N-MMC is presented in Section III. Section IV explains the proposed capacitor voltage balancing scheme. Experimental results conducted on a downscaled prototype are included in Section V. Finally, Section VI concludes this paper.

## II. Basic Operating Principles of the N-MMC

### A. Topology Description

The circuit configuration of a three-phase N-MMC is shown in Fig. 2. Each of its phases comprises $2N$+1 identical SMs: $N$ upper-arm SMs, $N$ lower-arm SMs, and one middle SM, which are connected through two buffer inductors $L$. Each SM contains a capacitor and two insulated-gate bipolar transistors (IGBT) $S_1$ and $S_2$. Consequently, each SM has two working states: the ON-state, when $S_1$ is switched on and $S_2$ is switched off; and the OFF-state, when $S_2$ is switched on and $S_1$ is switched off.

### B. Mathematical Model

A circuit diagram of phase $A$ of the N-MMC is shown in Fig. 2. It is similar to phase $B$ and phase $C$. $u_{oj}$ is the output voltage of phase $j$ ($j \in \{A, B, C\}$), $i_{oj}$ is the phase current, and $E$ is the dc-link voltage. $u_{uj}(i)$ and $u_{wj}(i)$ ($i \in \{1, 2, \ldots N\}$) represent the output voltage of the $i$-th SM in the upper arm or the lower arm, respectively. $u_{uj}$, $i_{uj}$ and $u_{wj}$, $i_{wj}$ represent the voltages and currents of the upper arm and the lower arm, respectively. Note that a single coupled inductor is used for the analysis in Fig. 2, in which no equivalent inductor appears at the ac terminal compared to the case of two separate inductors [19]. As a result, the actual output voltage can be

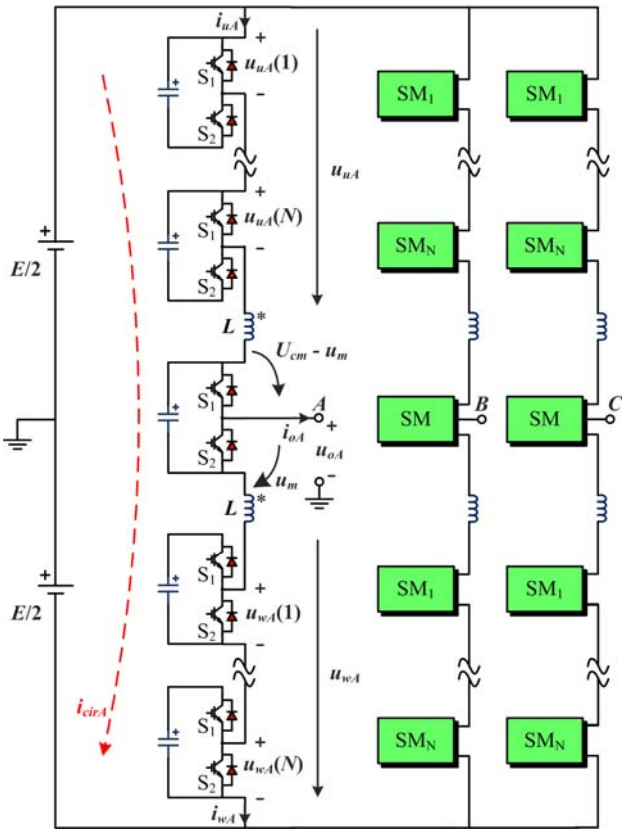



Fig. 2. Circuit configuration of the new MMC (N-MMC).

accurately derived in default of the voltage drop across the equivalent inductor. In each SM, the capacitor voltages of the upper-arm SMs and lower-arm SMs are equal to $U_c$. However, when the capacitor voltage of the middle SM is $U_{cm}$, there is a constraint as follows:

$$NU_c + U_{cm} = E\,. \tag{1}$$

Then the following equations can be obtained by Kirchhoff's voltage law:

$$L\frac{di_{uj}}{dt} + M\frac{di_{wj}}{dt} = \frac{E}{2} - u_{uj} - u_{oj} - U_{cm} + u_m \tag{2a}$$

$$L\frac{di_{wj}}{dt} + M\frac{di_{uj}}{dt} = \frac{E}{2} - u_{wj} + u_{oj} - u_m \tag{2b}$$

$$u_{uj} = \sum_{i=1}^{N} u_{uj}(i) \tag{3a}$$

$$u_{wj} = \sum_{i=1}^{N} u_{wj}(i) \tag{3b}$$

where $L$ is the self-inductance, and $M$ is the mutual inductance between the upper-arm SMs and the lower-arm SMs ($M$=$L$).

Hence, the expressions (1)–(3) can be derived as:

$$u_{oj} = \frac{1}{2}\left(u_{wj} - u_{uj}\right) + u_m - \frac{1}{2}U_{cm}\,. \tag{4}$$

In addition, $i_{cirj}$ is defined as the circulating current, which circulates through both the upper and lower arms and can be given by:

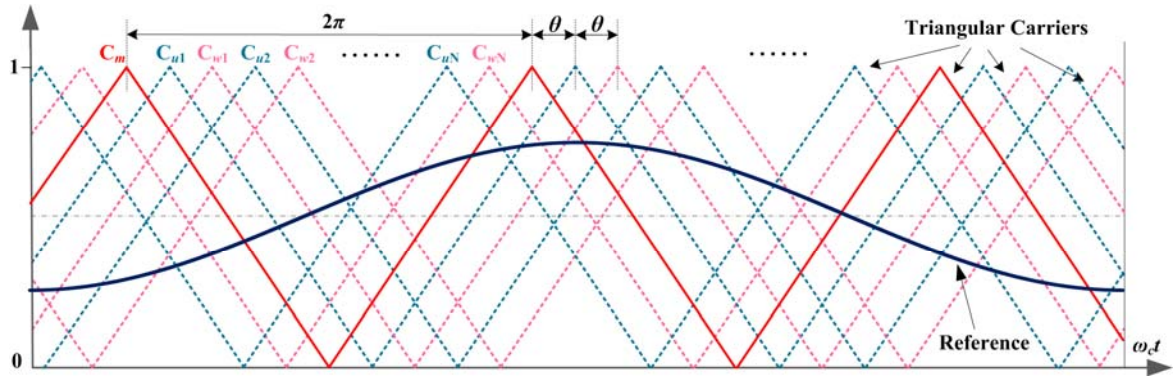



Fig. 3. Phase-shifted Carrier pulse width modulation (PSC-PWM) for the N-MMC.

$$i_{cirj} = \frac{1}{2}\left(i_{uj} + i_{wj}\right) \tag{5}$$

Ideally, the phase current $i_{oj}$ would be split equally between these two arms, and the arm currents can be expressed as:

$$i_{uj} = i_{cirj} + \frac{1}{2} i_{oj} \tag{6a}$$

$$i_{wj} = i_{cirj} - \frac{1}{2} i_{oj} . \tag{6b}$$

Moreover, by combining expressions (2) and (5), the dc-loop dynamic equation can be obtained as:

$$4L \frac{di_{cirj}}{dt} = \frac{E}{2} - U_{cm} - u_{uj} - u_{wj} . \tag{7}$$

## III. Proposed PSC Modulation for the N-MMC

The modulation schemes used in traditional MMC are not applicable any more due to the asymmetric structure of the N-MMC. Therefore, the proposed PSC-PWM with an optimal phase-shifted angle will be analyzed in this section. In addition, in order to suppress the harmonics of the phase voltage, the situation will be further discussed when the middle SM capacitor voltage employs 0.5Uc and Uc, respectively.

### *A. Description of the Proposed PSC Modulation for the N-MMC*

The proposed PSC modulation scheme for the N-MMC with $N$ SMs per arm is illustrated in Fig. 3. There are a total of $2N$+1 triangular carriers with a frequency of $f_c$ ($C_m$ for the middle SM, $C_{u1}$–$C_{uN}$ for the SMs in the upper arm, and $C_{w1}$–$C_{wN}$ for the SMs in the lower arm). Each SM is assigned with a particular triangular carrier, so that all of the SMs have the same switching frequency and the semiconductor stresses are evenly distributed. Moreover, the triangular carriers are phase-shifted with respect to each other by the phase-shift angle:

$$\theta = \frac{2\pi}{2N+1} . \tag{8}$$

By choosing the phase angle of the middle SM as

$$\theta_m = 0 \tag{9}$$

the phase angle of the *i-th* ($i$=1, 2…$N$) carrier $C_{ui}$ in the upper arm can be obtained as:

$$\theta_{up}(i) = \frac{2\pi}{2N+1}(2i) . \tag{10}$$

As for the *i-th* carrier $C_{wi}$ in the lower arm, it is:

$$\theta_{lw}(i) = \frac{2\pi}{2N+1}(2i-1) . \tag{11}$$

On the other hand, the reference signal is expressed as:

$$u_{ref} = \frac{1}{2}\left(1 + M\cos\left(\omega_o t + \varphi\right)\right) \tag{12}$$

where $M$ ($0 \le M \le 1$) denotes the modulation ratio, $\omega_o$ is the angular frequency of the output ac voltage, and $\varphi$ is the phase angle. Then, the switching pulses of each of the SMs are generated by comparing the reference signal with the corresponding carrier wave. For the middle SM and the lower-arm SMs, it is in the ON-state when the reference is greater than the carrier, and it is in the OFF-state when the carrier is greater than the reference. In contrast, with respect to the upper-arm SMs, the SM will be in the OFF-state when the reference is higher while it is in the ON-state when the carrier is higher.

Based on a Fourier series analysis [22], the Fourier representation of the output voltage of the middle SM, the upper-arm SMs, and the lower-arm SMs can be expressed as:

$$u_m = \frac{U_{cm}}{2} + \frac{MU_{cm}}{2}\cos(\omega_o t + \varphi) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2U_{cm}}{m\pi}\sin\left[\frac{(m+n)\pi}{2}\right]$$
$$\times J_n\left(\frac{Mm\pi}{2}\right)\cos\left[m\omega_c t + n(\omega_o t + \varphi)\right] \tag{13a}$$

$$\times J_n\left(\frac{Mm\pi}{2}\right)\cos\left[m\left(\omega_c t + \theta_{up}(i)\right) + n(\omega_o t + \varphi)\right] \tag{13b}$$

$$u_{lw}(i) = \frac{U_c}{2} + \frac{MU_c}{2}\cos(\omega_o t + \varphi) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2U_c}{m\pi}\sin\left[\frac{(m+n)\pi}{2}\right]$$
$$\times J_n\left(\frac{Mm\pi}{2}\right)\cos\left[m\left(\omega_c t + \theta_{lw}(i)\right) + n(\omega_o t + \varphi)\right] \tag{13c}$$

where $\omega_c$ is the angular frequency of the triangular carriers, $m$ is the harmonic order of the carrier wave, $n$ is the harmonic

order of the reference wave, and $J_n(x)$ refers to the Bessel function of the order $n$ and the argument $x$.

### B. Harmonics of the Output Voltage when Ucm=0.5Uc

When the capacitor voltage of the middle SM is set as $0.5U_C$, substitution of (13) into (4) leads to:

$$u_{oj}=\frac{2N+1}{4}MU_c\cos(\omega_o t+\varphi)+\sum_{k=1}^{2N+1}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{U_c}{m\pi}\sin\left[\frac{(m+n)\pi}{2}\right]\times J_n\left(\frac{Mm\pi}{2}\right)\cos\left[m\left(\omega_c t+\frac{(k-1)2\pi}{2N+1}\right)+n(\omega_o t+\varphi)\right] \quad (14)$$

where according to (1), $U_c$ can be derived as:

$$U_c=\frac{2E}{2N+1}. \quad (15)$$

Furthermore, since:

$$\sum_{k=1}^{2N+1}\cos\left(\xi+\frac{m(k-1)2\pi}{2N+1}\right)=0 \text{ , if } m\neq h(2N+1),\ h=1,\ 2,\ 3\ \ldots, \quad (16)$$

all of the switching harmonics of $u_{oj}$ will be eliminated except those at $2N+1$ multiples of the carrier frequency and their sideband components, that is:

$$u_{oj}=\frac{ME}{2}\cos(\omega_o t+\varphi)+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2E}{(2N+1)m\pi}\times\sin\left[\frac{((2N+1)m+n)\pi}{2}\right]J_n\left(\frac{(2N+1)Mm\pi}{2}\right)\times\cos\left[(2N+1)m\omega_c t+n(\omega_o t+\varphi)\right]. \quad (17)$$

Equation (17) indicates that with the switching frequency of $f_c$ to each of the SMs, the equivalent switching frequency of the output voltage of the N-MMC can increase to $(2N+1)f_c$, leading to a significant reduction in the filter size.

Although the best harmonic features can be achieved when $U_{cm}$ is selected as half of $U_c$, the drawback is that the output voltage capability of the middle SM is not fully utilized. Therefore, this case is applicable when the dc-link voltage $E$ is lower than the rated value.

### C. Harmonics of the Output Voltage when Ucm=Uc

Alternatively, in order to assure full utilization of the middle SM, its capacitor voltage is set equal to $U_c$. Therefore:

$$U_c=\frac{E}{N+1}. \quad (18)$$

Similarly, the output voltage can be expressed by the Fourier series as (19). Compared to (17), it can be seen that the output voltage in this case contains more harmonic components because the harmonics of the middle SM cannot be completely cancelled out. As a result, harmonics around the $f_c$ frequency and its multiples will appear. Nonetheless, the amplitude of these newly introduced harmonics is relatively small and acceptable, which will only cause a slight deterioration in the output current waveform. This will be confirmed by the simulation and experimental results.

### D. Simulation Results

Figs. 4 and 5 show the simulated waveforms of the N-MMC with two SMs per arm. The simulated parameters include, the fundamental frequency $f$=50Hz, modulation ratio $M$=0.95, buffer inductor $L$=2.5mH, rated capacitor voltage $U_c$=100V, carrier frequency $f_c$=1kHz, and the loads of $R_{load}$=3000Ω, $L_{load}$=3mH. Specifically, to ensure the harmonic features of the proposed PSC-PWM scheme not affected by other factors (such as the capacitor voltage ripple and the capacitor voltage unbalance), an infinite capacitance for each of the SMs is assumed here.

Fig. 4 depicts the output voltage of phase $A$ and its harmonic spectrums when $U_{cm}=U_c$, where the number of voltage levels is seven. In addition, the FFT results show that the voltage harmonics mainly concentrate on frequencies of 1kHz (=$f_c$) and 5kHz (=5$f_c$). On the other hand, with respect to $U_{cm}=0.5U_c$, the simulation results are shown in Fig. 5. Although the output voltage contains only six voltage levels, it should be noted that the voltage waveform is much smoother (without spikes) than that in Fig. 4, and that the harmonic spectrums in this case are mainly around 5kHz (=5$f_c$), leading to better harmonic features. All of these simulation results are in good agreement with the above analyses of the proposed PSC modulation scheme.

## IV. Proposed Capacitor Voltage Balancing Control for the N-MMC

SM capacitor voltage balancing control for the traditional MMC has been widely discussed in the literature [17]-[21]. With respect to the N-MMC, these existing methods are not applicable due to the existence of the middle SM. Reference [10] regulates the capacitor voltage of the middle SM $U_{cm}$ by judging the sign of the output current $i_{oj}$. When $i_{oj}$ is positive and $U_{cm}$ is overly high, the middle SM will be inserted for a longer time to discharge itself. On the other hand, when $i_{oj}$ is positive and $U_{cm}$ is overly low, the middle SM will be bypassed for a longer time to charge itself. Consequently, the dc offset of the output current $i_{oj}$ will be introduced because the balancing method distorts the sinusoidal output of the middle SM, leading to a dc offset current at $i_{oj}$.

$$u_o=\frac{ME}{2}\cos(\omega_o t+\varphi)+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{E}{(N+1)m\pi}\sin\left[\frac{((2N+1)m+n)\pi}{2}\right]J_n\left(\frac{(2N+1)Mm\pi}{2}\right)\cos\left[(2N+1)m\omega_c t+n(\omega_o t+\varphi)\right]+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{E}{(N+1)m\pi}\sin\left[\frac{(m+n)\pi}{2}\right]\times J_n\left(\frac{Mm\pi}{2}\right)\cos\left[m\omega_c t+n(\omega_o t+\varphi)\right] \quad (19)$$

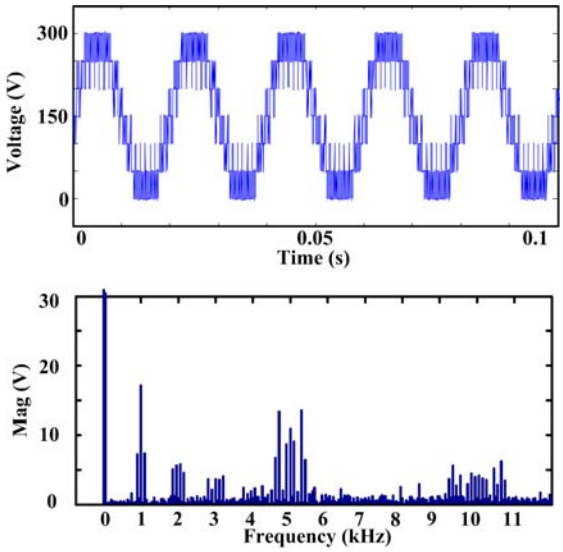



Fig. 4. Simulation waveforms for the output voltage of phase *A* and its harmonic spectrum when $U_{cm}$=$U_c$.

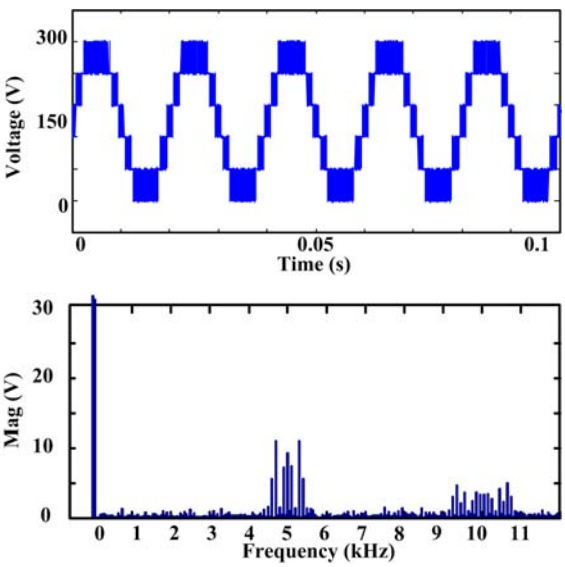



Fig. 5. Simulation waveforms for the output voltage of phase *A* and its harmonic spectrum when $U_{cm}$=0.5$U_c$.

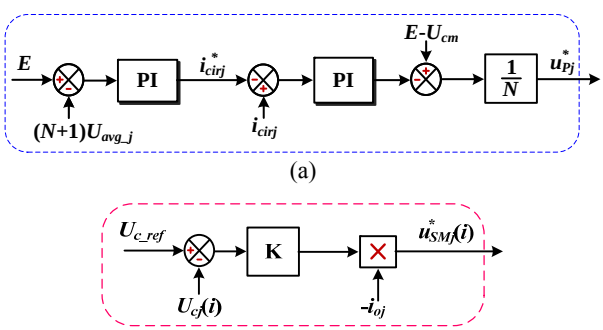



Fig. 6. Block diagram of the proposed balancing scheme: (a) Phase energy balancing control and (b) SM balancing control.

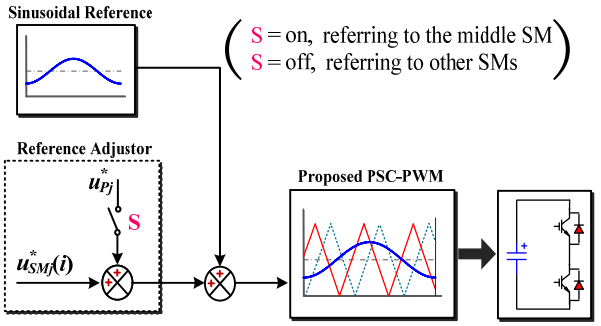



Fig. 7. Implementation of the balancing control scheme under the proposed PSC-PWM.

In order to solve this problem, a novel voltage balancing control scheme is proposed, as shown in Fig. 6. It comprises two controllers: a phase energy balancing controller for the energy stability of each phase; and a SM balancing control for the voltage regulation of each SM capacitor. The phase energy balancing controller forces $(N+1)U_{avg\_j}$ to follow the dc-bus voltage $E$, where $U_{avg\_j}$ is the average capacitor voltage of the $2N$+1 SMs within phase $j$. This process is accomplished by adjusting the inner-loop circulating current $i_{cirj}$. It should be noted that since the circulating current directly flows through the capacitor of the middle SM and the dc-bus, the term of "$E$-$U_{cm}$" is used as a feed-forward compensation at the output of the PI controller.

With respect to the SM balancing controller, it is ensured that the capacitor voltage of each of the SMs is equal to a desired voltage $U_{c\_ref}$ by adjusting its terminal voltage based on the amplitude of the output current $i_{oj}$ rather than the sign of $i_{oj}$ to avoid the introduction of a dc offset. Note that with regard to the upper-arm and lower-arm SMs, $U_{c\_ref}$ is always set as $U_{avg\_j}$. Meanwhile, value of $U_{c\_ref}$ for the middle SM can be chosen as either $U_{avg\_j}$ or 0.5 $U_{avg\_j}$ depending on the settings of the PSC-PWM. Fig. 7 shows the complete implementation of the proposed balancing control scheme combined with the aforementioned PSC-PWM. The sum of the outputs of the phase energy balancing controller $u^*_{Pj}$ and the SM balancing controller $u^*_{SMj}(i)$ are used as voltage adjustments attached to the sinusoidal reference signal in the PSC-PWM.

## V. Experimental Results

### *A. System Configuration*

A downscale three-phase N-MMC prototype is built to verify the effectiveness of the proposed modulation and balancing schemes. The system configuration is shown in Fig. 8, where the N-MMC is operated as an inverter and the dc-bus voltage is obtained by using a three-phase diode rectifier. As shown in Fig. 9, each arm employs two SMs. In other words, there are a total of five SMs per phase. The circuit parameters of the prototype are summarized in Table I.

Fig. 10 shows the control system used for the experiment.

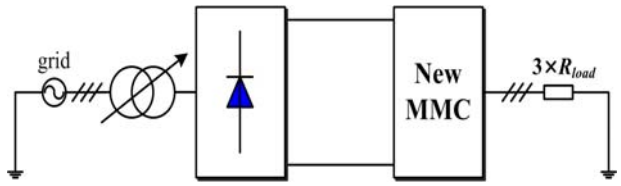


Fig. 8. System configuration used for experiment..

Fig. 9. Photograph of the laboratory setup.

The architecture of a digital signal processor (DSP) plus a field-programmable gate array (FPGA) is adopted as the central controller, where a TMS320F28335 DSP is used to generate the three-phase sinusoidal references while an EP3C25Q240C8 FPGA is adopted to generate the triangular carriers with a phase-shift angle of 72° (=360°/5, as illustrated in Fig. 2). Each of the SMs is controlled by an EPM570T100 complex programmable logic device (CPLD), which receives PWM signals via optical fibers and sends back monitored capacitor voltages. Furthermore, all of the experimental waveforms are acquired through a DL850 scopecorder.

### *B. Operating Performance when the Middle SM Capacitor Voltage is Ucm=Uc*

Fig. 11 presents experimental results when the middle SM capacitor voltage $U_{cm}$ is set as 100V and the dc-bus voltage is $E$=300V. In the steady state, Fig. 11(a) shows the sinusoidal phase current of $i_{oA}$ and the five SM capacitor voltages. It is seen that all five of the capacitor voltages coincide with each other around 100V, which verifies the validity of the proposed capacitor voltage balancing scheme. Fig. 11(b) shows the phase voltage $u_{oA}$. The number of voltage levels of the $u_{oA}$ phase is seven. However, it seems to be blurring due to the existence of voltage spikes. Further, as depicted in Fig. 11(c), the harmonics of $u_{oA}$ are located at the frequencies of multiples of 3kHz (=$f_c$), which confirms the PSC-PWM scheme as analyzed in (17).

Moreover, Fig. 11(d) exhibits the transient-state performance of the proposed capacitor voltage balancing scheme. Firstly, the balancing scheme was intentionally disabled, and it is observed that the capacitor voltages gradually disperse. Then, after re-enabling the SM balancing control scheme, the capacitor voltages quickly converged and they were finally balanced again.

TABLE I
LABORATORY PROTOTYPE SPECIFICATIONS

| Quantity | Value |
|---|---|
| Number of SMs per arm | $N$=3 |
| Rated active power | $P$=300W |
| Rated reactive power | $Q$=0Var |
| Fundamental frequency | $f_o$=50Hz |
| Rated SM capacitor voltage | $U_c$=100V |
| SM capacitance | $C$=1867μF |
| Buffer inductors | $L$=5mH |
| Carrier frequency | $f_c$=3kHz |
| Load resistance | 20Ω |

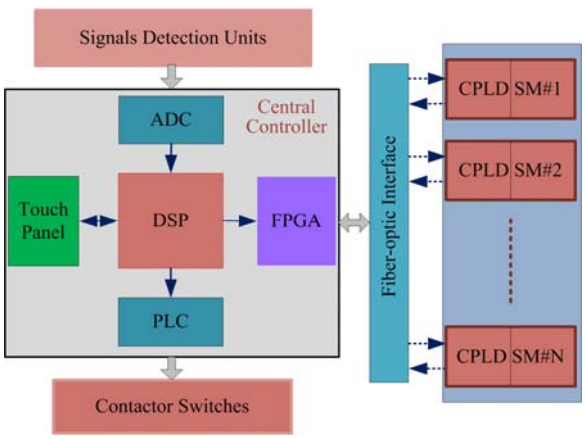
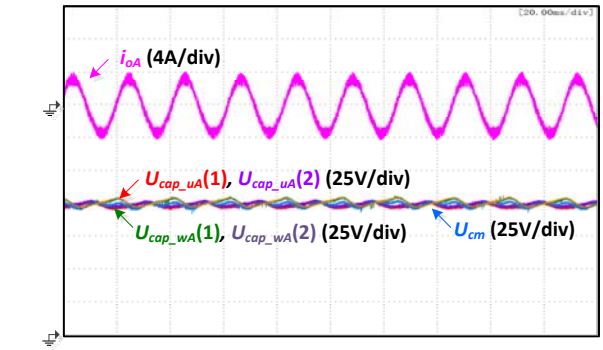


Fig. 10. Controller architecture used for experiment.

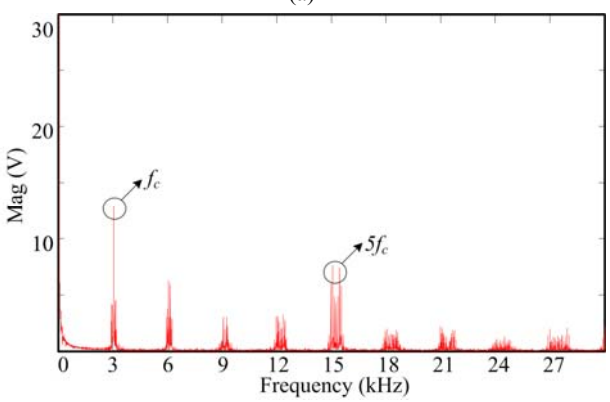
### *C. Operating Performance when the Middle SM Capacitor Voltage is Ucm=0.5Uc*

When the middle SM capacitor voltage $U_{cm}$ is set as half of $U_c$ (i.e., 50V) and the dc-bus voltage is $E$=250V, the corresponding experimental results are illustrated in Fig. 12. The steady-state waveforms are shown in Figs. 12(a) and 12(b), while the transient-state waveform is exhibited in Fig. 12(d).
In the steady state, the phase current $i_{oA}$ and the SM capacitor voltages are presented in Fig 12(a). With the proposed capacitor voltage balancing scheme, both the upper-arm and lower-arm SM capacitor voltages are around 100V, while the middle SM capacitor is well maintained at 50V. Fig. 12(b) shows the phase voltage $u_{oA}$. The number of voltage levels of $u_{oA}$ in this case is six, which is less than the waveform in Fig. 11(b). Nonetheless, $u_{oA}$ here is much smoother than that shown in Fig. 11(b). Fig. 12(c) shows the harmonic spectrum of $u_{oA}$. Compared with Fig. 11(c), it is clear that the magnitudes of all of the harmonics are reduced except for the frequencies around 15kHz (=5$f_c$). Note that the harmonics below 5$f_c$ are not eliminated as desired. This is due to the fact that the voltage balancing control inevitably alters the references of each of the SMs and impairs the results of the PSC modulation. Regardless, the effectiveness of the PSC-PWM can still be demonstrated.

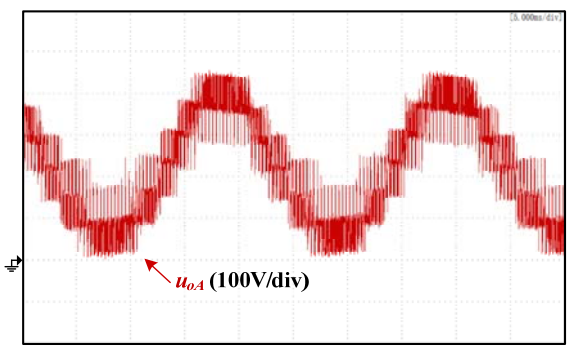
Moreover, the transient-state experimental waveforms are



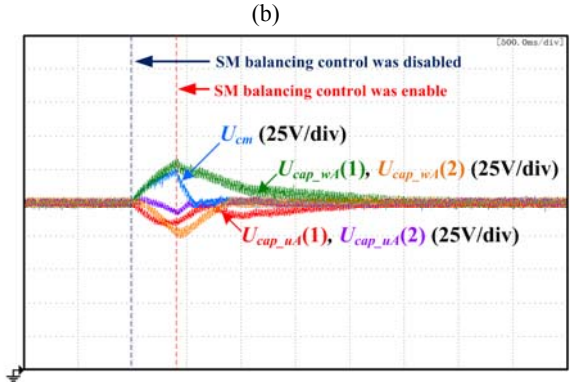

(a)




(c)

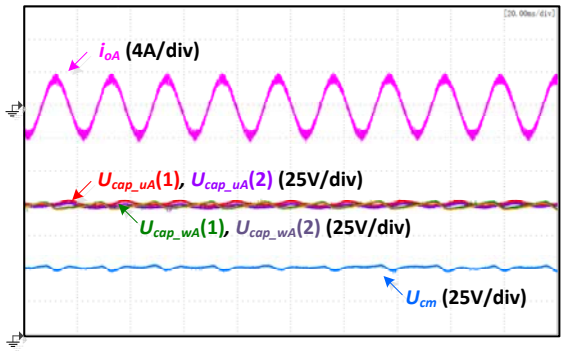



(b)

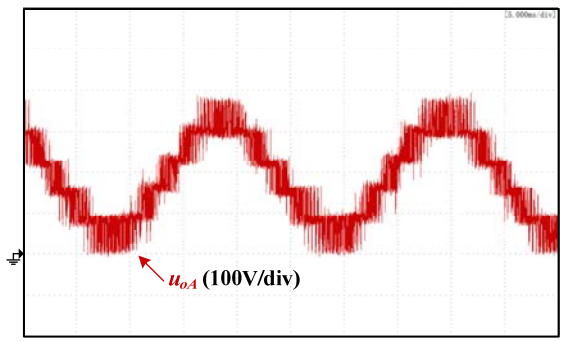



(d)

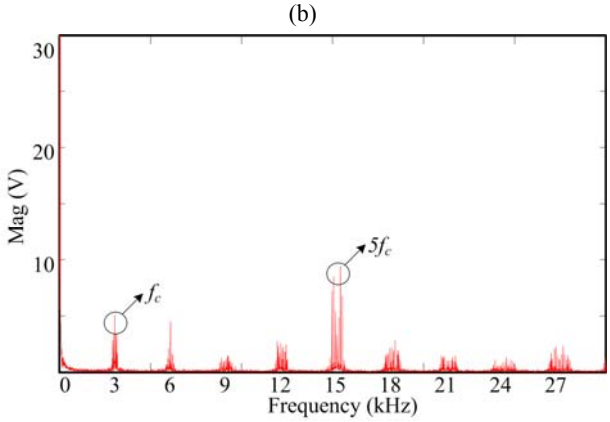
Fig. 11. Experimental waveforms when middle SM capacitor voltage $U_{cm}$=$U_c$: (a) Phase current and capacitor voltages under steady state, (b) Phase voltage under steady state, (c) Harmonic spectrum of the phase voltage, and (d) Capacitor voltages under transient state.



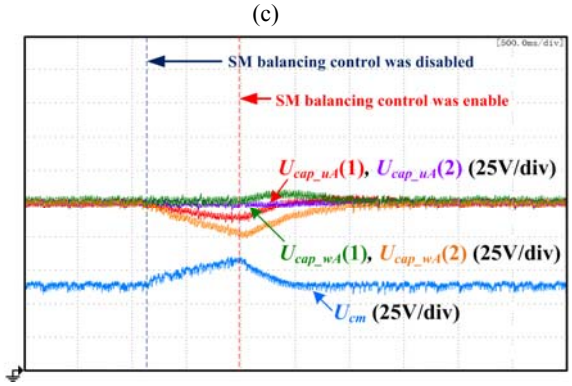

(a)




(b)




(c)




(d)

Fig. 12. Experimental waveforms when middle SM capacitor voltage $U_{cm}$=0.5$U_c$: (a) Phase current and capacitor voltages under steady state, (b) Phase voltage under steady state, (c) Harmonic spectrum of the phase voltage, and (d) Capacitors voltages under transient state.

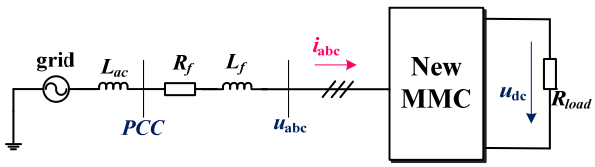



Fig. 13. System configuration used for simulation.

TABLE II
SIMULATION SPECIFICATIONS

| Quantity | Value |
|---|---|
| Number of SMs per arm | $N$=5 |
| Rated active power | $P$=500kW |
| Rated reactive power | $Q$=300kVar |
| Rated *line-line* grid voltage | 2500V(rms) |
| Rated dc voltage | $u_{dc}$=5000V |
| Fundamental frequency | $f_o$=50Hz |
| Rated SM capacitor voltage | $U_c$=850V |
| SM capacitance | $C$=5000μF |
| Buffer inductors | $L$=5mH |
| Carrier frequency | $f_c$=2kHz |
| Load resistance | $R_{load}$=50Ω |

shown in Fig. 12(d), where the SM balancing control was disabled and then re-enabled. This also indicates the good performance of the proposed balancing control scheme.

## VI. FURTHER SIMULATION RESULTS OF THE N-MMC IN GRID-CONNECTED APPLICATIONS

Since one of the most promising applications of multilevel converters is use as a grid-connected converter, a further study of the performance of the N-MMC as a three-phase grid-connected rectifier is provided in this Section. The study is based on a simulation in the MATLAB/Simulink environment, with five SMs per arm. That is, there are a total of eleven SMs per phase, and the capacitor voltage of the middle SM is selected as $U_{cm}=U_c$. The system configuration for the simulation is shown in Fig. 13. Detailed parameters of the simulated circuit and the operating conditions are listed in Table II. It should be noted that since the ac terminals of the N-MMC are clamped by the grid voltages, the harmonic features of the output voltages cannot be tested in this case. Thus, only the control performances are verified.

Fig. 14 presents the simulation waveforms. It can be seen

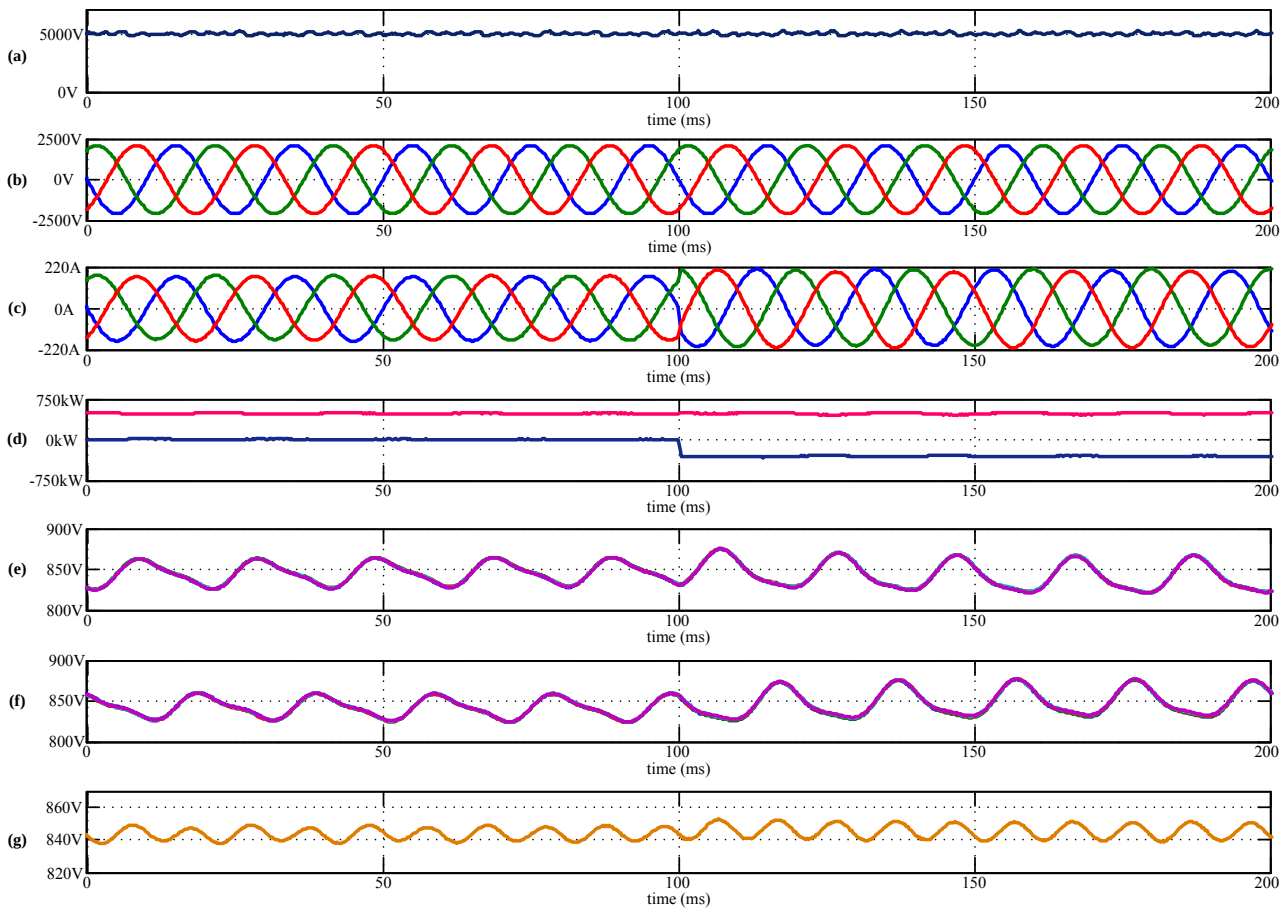



Fig. 14. Simulation results: (a) output dc voltage $u_{dc}$, (b) three-phase grid voltages, (c) three-phase input currents, (d) active power and reactive power, (e) five upper-arm SM capacitor voltages of phase-A, (f) five lower-arm SM capacitor voltages of phase-A, and (g) middle-SM capacitor voltage of phase-A.

that the output dc voltage $u_{dc}$ is well regulated at 5kV, and that the absorbed active power from the grid is 500kW. Initially, no reactive power is required by the N-MMC. Therefore, the input currents are in phase with the grid voltages showing a unity power factor. After $t$=100ms, the 300kVar reactive power is commanded to be sent to the grid. During both the steady states and the dynamic states, the output dc voltage is stable and the input ac currents are well controlled. Moreover, the capacitor voltages are kept well balanced. It can be concluded that the N-MMC is a good candidate for grid-connected applications.

## VII. Conclusion

In this paper, PSC modulation and balancing schemes have been proposed for the N-MMC. The harmonic features of the output voltage are also investigated by Fourier analysis. With the proposed PSC modulation, each of the SMs has the same switching frequency and the semiconductor stresses are evenly distributed. In addition, when the middle SM capacitor voltage employs half of the other capacitor voltage, the harmonics of the output voltage are better than when employing the same voltage with other capacitors. Nonetheless, the amplitude of these newly introduced harmonics is still relatively small and acceptable whether the middle SM adopts half or one of the other capacitor voltage. Furthermore, the balancing control is realized by adjusting the amplitude of the reference signal rather than the offset in order to avoid introducing a dc component in phase current.

Moreover, a three-phase N-MMC prototype was built and tested in the laboratory. Experimental results confirm the validity of the proposed PSC modulation and balancing strategy and show very good static and dynamic performances. Finally, a simulation study is provided to show the effectiveness of the N-MMC as a grid-connected converter.

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## References

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, and S. Kouro, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, Vol. 2, No. 2, pp. 28-39, Jun. 2008.

[2] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, and E. Galvan, "Power-electronic systems for the grid integration of renewable energy sources: a survey," *IEEE Trans. Ind. Electron*., Vol. 53, No. 4, pp. 1002-1016, Jun. 2006.

[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron*., Vol. 54, No. 6, pp. 2930-2945, Dec. 2007.

[4] S. Kouro, M. Malonowski, K. Gopakumar, and J. Pou, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.

[5] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, Vol. 37, No. 2, pp. 611-618, Mar./Apr. 2001.

[6] A. Chen, L. Hu, L. Chen, Y. Deng, and X. He, "A multilevel converter topology with fault-tolerant ability," *IEEE Trans. Power Electron*., Vol. 20, No. 2, pp. 405-415, Mar. 2005.

[7] S. B. Monge and J. N. Apruzzese, "A multilevel active-clamped converter topology—operating principle," *IEEE Trans. Ind. Electron*., Vol. 58, No. 9, pp. 3868-3878, Sep. 2011.

[8] J. N. Apruzzese, S. B. Monge, J. Bordonau, S. Alepuz, and A. C. Prado, "Analysis of the fault-tolerance capacity of the multilevel active-clamped converter," *IEEE Trans. Ind. Electron*., Vol. 60, No. 11, pp. 4773-4783, Nov. 2013.

[9] K Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage fluctuation suppression method of floating capacitors in a new modular multilevel converter," *Energy Conversion Congress and Exposition (ECCE)*, *IEEE*, pp. 2072-2078, Sep. 2011.

[10] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron*., Vol. 60, No. 5, pp. 1943-1954, May 2013.

[11] R. Marquardt and A. Lesnicar, "A new modular voltage source inverter topology," in *Conf. Rec. EPE*, Toulouse, France, pp. 1-10, 2003.

[12] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *Power Tech Conf. Proc. 2003 IEEE Bologna*, Vol.3, No., pp. 1-6, Jun. 2003.

[13] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: a review," *IEEE Trans. Power Electron.*, Vol. 30, No. 1, pp. 37–53, Jan. 2015.

[14] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electron*., Vol. 6, No. 1, pp. 96-107, Jan. 2013.

[15] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carried modulation for modular multilevel converters," *IEEE Trans. Power Electron*., Vol. 30, No. 1, pp. 297-310, Jan. 2015.

[16] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converters," *IEEE Trans. Power Electron.,* Vol. 27, No. 8, pp. 3472-3481, Aug. 2012.

[17] M. Guan and Z. Xu, "Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions," *IEEE Trans. Power Electron.,* Vol. 2, No. 12, pp. 4858-4867, Dec. 2012.

[18] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J. Vannier, and M. Molinas, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillations reduction," *IEEE Trans. Ind. Electron.,* Vol. 60, No. 6, pp. 2360-2371, Jun. 2013.

[19] M. Hagiwara and H. Akagi, "Control and experiment of

pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 7, pp. 1737-1746, Jul. 2009.
[20] K. Shen, J. Wang, D. Zhao, M. Ban, Y. Ji, and X. Cai, "Investigation of capacitor voltage regulation in modular multilevel converters with staircase modulation," *Journal of Power Electronics*, Vol. 14, No. 2, pp. 282-291, Mar. 2014.
[21] A. Antonopoulos, L. Angquist, and and H. P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.* (EPE), Barcelona, Spain, pp. 1-10, Sep. 2009.
[22] Holmes D G and Lipo T A. *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003.

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