JPE 16-1-24

http://dx.doi.org/10.6113/JPE.2016.16.1.227
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Digitally Current Controlled DC-DC Switching Converters Using an Adjacent Cycle Sampling Strategy

Tingcun Wei*, Yulin Wang*, Feng Li*, Nan Chen*, and Jia Wang†

*,†School of Computer Science and Engineering, Northwestern Polytechnical University, Xi'an, China

Abstract

A novel digital current control strategy for digitally controlled DC-DC switching converters, referred to as Adjacent Cycle Sampling (ACS), is proposed in this paper. For the ACS current control strategy, the available time interval from sampling the current to updating the duty ratio, is approximately one switching cycle. In addition, it is independent of the duty ratio. As a result, the contradiction between the processing speed of the hardware and the transient response speed can be effectively relaxed by using the ACS current control strategy. For digitally controlled buck DC-DC switching converters with trailing-edge modulation, digital current control algorithms with the ACS control strategy are derived for three different control objectives. These objectives are the valley, average, and peak inductor currents. In addition, the sub-harmonic oscillations of the above current control algorithms are analyzed and eliminated by using the digital slope compensation (DSC) method. Experimental results based on a FPGA are given, which verify the theoretical analysis results very well. It can be concluded that the ACS control has a faster transient response speed than the time delay control, and that its requirements for hardware processing speed can be reduced when compared with the deadbeat control. Therefore, it promises to be one of the key technologies for high-frequency DC-DC switching converters.

Key words: Adjacent Cycle Sampling (ACS), Digitally controlled DC-DC switching converter, Digital current control algorithm, Digital Slope Compensation (DSC), Sub-harmonic oscillation, Transient response speed

I. INTRODUCTION

On account of its obvious advantages, such as the flexibility to implement complicated control strategies and algorithms, the programmability to realize reconfigurable power systems, faster design process, high power conversion efficiency, robustness to noise, and insensitivity to parameter drifts of components, the digitally controlled DC-DC switching converter has gained a great deal of attention in the fields of power electronics and integrated circuits [1]-[20]. In order to improve the transient response features and to reduce the sizes of the passive filter components (inductor and capacitor), the switching frequency of the DC-DC converter is ever-increased. It is now up to several megahertz (the switching cycle is decreased to several hundred nanoseconds) [3], [4], which makes the available time interval for a digital control loop more critical. As a result, the hardware circuits must have higher processing speeds, which presents great challenges in the design and hardware implementation of digitally controlled high-frequency DC-DC switching converters [5].

It is well known that the transient response performances of a DC-DC switching converter can be effectively improved by adding a current controlled loop (often referred to as an inner loop) on the voltage controlled loop (often referred to as an outer loop) [3]-[5], [11]-[15]. The current controlled loop is based on the ripple of the inductor current. Most current control algorithms make the valley, peak, or average values [6-10] of the inductor current follow a reference signal generated by the outer voltage controlled loop. Depending on the response speed for variations of the inductor current, digital current control strategies can be classified as either deadbeat control [11], [12] or time delay control [13]-[15].

Manuscript received Apr. 20, 2015; accepted Jul. 22, 2015
Recommended for publication by Publication Editor Joung-Hu Park.
†Corresponding author: jwang@nwpu.edu.cn
Tel/Fax: +86-29-88431952, Northwestern Polytechnical University
*School of Computer Science and Engineering, Northwestern Polytechnical University, China

Although the deadbeat control has a fast response speed to variations of the output load, it requires a fast feedback loop processing speed since the available time interval for calculating and updating the duty ratio is less than one switching cycle. This is especially critical in the situation of a small duty ratio for trailing-edge and triangle trailing-edge modulations, and in the situation of a large duty ratio for leading-edge and triangle leading-edge modulations. On the other hand, for the time delay control, the available time interval is increased by one switching cycle when compared with the deadbeat control. This can ensure sufficient time for the calculation and renewal of the duty ratio which in turn relaxes the requirements for the processing speed of the hardware circuits. However, the transient response feature [16], [17] is degraded. Consequently, it is difficult to satisfy the requirements of digitally controlled high-frequency DC-DC switching converters by using the existing digital current control strategies.

In order to relax the contradiction between the processing speed (related to the cost) of hardware circuits and the transient response features, a novel digital current control strategy, referred to as Adjacent Cycle Sampling (ACS), is proposed and studied in this paper. Without a loss of generality, a buck DC-DC switching converter with trailing-edge modulation is taken as an example. Based on the proposed ACS control strategy, the current control algorithms for different control objectives are derived, and their stabilities are investigated. In addition, the elimination method of sub-harmonic oscillation is studied. Finally experimental results are given to verify the theoretical analysis.

The structure of this paper is as follows. In section II, the Adjacent Cycle Sampling (ACS) strategy is proposed after the analysis of the traditional current control strategies. In section III, a digital current control algorithms using the ACS control strategy is derived, where the valley, peak, and average values of the inductor current are used as control objectives. In section IV, sub-harmonic oscillations of the above current control algorithms are investigated and an elimination method is studied. In Section V, experimental results are provided to verify the theoretical analysis. Some conclusions are given in section VI.

II. Adjacent Cycle Sampling Current Control Strategy

Fig. 1 shows the configuration of a digitally current controlled buck DC-DC switching converter. It consists of two analog-to-digital converters (ADCv and ADCi are used to digitize the output voltage and inductor current, respectively), a digital compensator (including a current controller and a voltage controller), and a digital pulse-width modulator (DPWM). The digital control strategy and

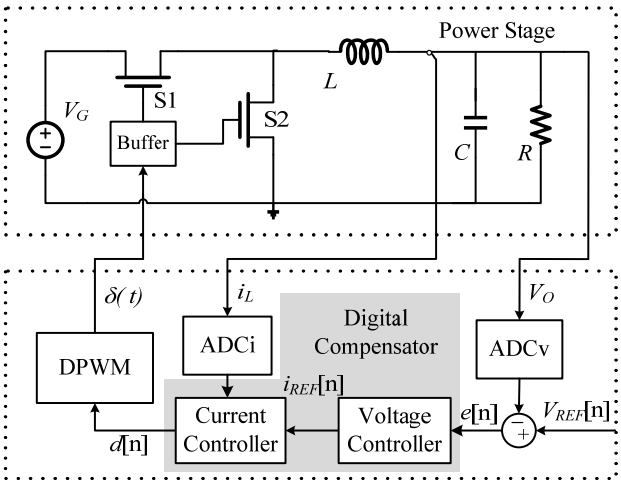


Fig. 1. Digitally current controlled DC-DC switching converter.

algorithm are implemented by the digital compensator. DPWM is used for the conversion of the digital duty ratio to an analog pulse signal. In this paper, a digital current control algorithm using the ACS control strategy is implemented by a current controller. In addition, a digital voltage control algorithm using PID (Proportion-Integration-Differentiation) is implemented by the voltage controller.

As shown in Fig. 1, V_G and V_O are the input and output voltages, respectively; V_{REF}[n] is the digital value of the reference voltage, e[n] is the digital error between the output and reference voltages; i_L is the current flowing through the inductor L; i_{REF}[n] is the target reference generated by the voltage controller in the outer loop; d[n] is the digital duty ratio from the output of the digital compensator; and δ(t) is the analog pulse signal converted by the DPWM from d[n], the duty ratio of which is proportional to d[n]. The pulse signal δ(t) turns the power switches, S1 and S2, on or off to regulate the output voltage. C is the output filter capacitor, and R is the equivalent load resistor.

A. Traditional Current Control Strategies

Without a loss of generality, a DC-DC switching converter with trailing-edge modulation is considered only. Timing diagrams of the three current control strategies, deadbeat control (a), time delay control (b), and ACS control (c), are illustrated in Fig. 2, where T_s is the switching cycle, and d[n] is the duty ratio of the n^{th} switching cycle, the value of which is between 0 and 1. T_d is the available time interval for updating the duty ratio, including the time needed for the ADC's conversion, the compensator's algorithm calculation and the DPWM's conversion.

Fig. 2 (a) shows a timing diagram of the deadbeat control strategy. At the beginning of the n^{th} cycle, or at the end of $(n-1)^{th}$ cycle, the inductor current, i_L[n-1], is sampled. Then the duty ratio d[n] is calculated and updated within the n^{th} cycle. For the deadbeat control strategy, T_d is equal to d[n]T_s, namely the calculating and updating of the duty ratio should

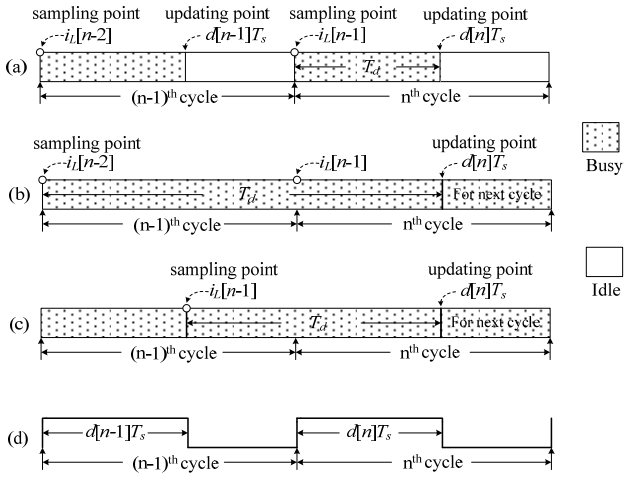


Fig. 2. Timing diagrams of current control strategies: (a) Deadbeat control, (b) Time delay control, (c) ACS control, and (d) Analog pulse signal δ(t).

be completed within $d[n]T_s$, which is always less than one switching cycle. In addition, with a decrease of d[n] and/or T_s, T_d becomes too little to finish the above operations unless the feedback loop has an extremely fast processing speed.

A timing diagram of the time delay control strategy is shown in Fig. 2 (b). The inductor current at the end of the $(n-2)^{th}$ cycle, i_L[n-2], is sampled. Then the duty ratio d[n] is calculated and updated within the n^{th} cycle. The available time interval T_d, from sampling the inductor current to updating the duty ratio, is equal to $(1+d[n])T_s$, which is always larger than one switching cycle. As a result, although the requirement for the loop processing speed can be reduced, the transient response speed is degraded.

B. Adjacent Cycle Sampling Strategy

As shown in Fig. 2 (a), for the deadbeat control, there is some idle time for the hardware circuits in every cycle. The basic idea of the Adjacent Cycle Sampling (ACS) control strategy is to utilize the idle time of the hardware circuits during the previous cycle. This is done to calculate the duty ratio of the present cycle.

Fig. 2(c) shows a timing diagram of the ACS control strategy. The inductor current of the previous cycle, i_L[n-1], is sampled at the falling edge of the pulse signal δ(t) (here for trailing-edge modulation). Then the duty ratio d[n] is calculated and updated based on i_L[n-1]. Therefore, the available time interval T_d is composed of two items: the switch off period of the previous cycle (the idle time of the hardware circuit in the deadbeat control), $(1-d[n-1])T_s$, and the switch on period of the present cycle, $d[n]T_s$. Thus, T_d can be expressed as:

$$T_d = (1-d[n-1])T_s + d[n]T_s \quad (1)$$

Since the two adjacent switching cycles have almost the same duty ratio, namely d[n-1]≈d[n], (1) can be rewritten as:

$$T_d = (1-d[n-1])T_s + d[n]T_s \approx T_s \quad (2)$$

TABLE I
AVAILABLE TIME INTERVAL FOR CALCULATING AND UPDATING THE DUTY RATIO

Modulation mode	Current control strategies		
	ACS control (≈T_s)	Deadbeat control	Time delay control
Trailing-edge	$T_s + (d[n] - d[n-1])T_s$	$d[n]T_s$	$T_s + d[n]T_s$
Leading-edge	$T_s + (d[n-1]-d[n])T_s$	$(1-d[n])T_s$	$T_s + (1-d[n])T_s$
Trailing-triangle	$T_s + (d[n-1]-d[n])T_s/2$	$d[n]T_s/2$	$T_s + d[n]T_s/2$
Leading-triangle	$T_s + (d[n-1]-d[n])T_s/2$	$(1-d[n])T_s/2$	$T_s + (1-d[n])T_s/2$

It can be concluded that, for the ACS control strategy, the available time interval is approximately equal to one switching cycle. In addition, it is independent of the duty ratio d[n]. Therefore, it can be predicted that, the ACS control has a faster transient response speed than the time delay control, and its requirement for the loop processing speed can be reduced when compared with the deadbeat control.

From Fig. 2, it can be observed that for all three kinds of current control strategies, the deadbeat, time delay and ACS control, the sampling time point of the inductor current is located at the beginning of the present cycle, at the end of two cycle before the present cycle, and the falling edge of previous cycle, respectively. Since the ACS control samples the inductor current at a certain point of the adjacent previous cycle, it is referred to as Adjacent Cycle Sampling control.

For a comparison of the above three current control strategies, the available time intervals for calculating and updating the duty ratio are summarized in TABLE I. In addition to the trailing-edge modulation, three other kinds of modulation (leading-edge, trailing-triangle, and leading-triangle) are also included for reference, without verbose analysis.

From TABLE I, it can be observed that, the available time intervals of the deadbeat, ACS and time delay control strategies are less than, approximately equal to, and larger than one switching cycle, respectively. The ACS control strategy is especially suitable for high-frequency DC-DC switching converters owing to its almost constant available time interval.

It should be noted that when duty ratio d[n] gets smaller and smaller, the time interval reserved for the time delay control is approximately equal to one switching period, T_s. This is almost the same as that for the proposed ACS method. However, a transient performance difference between the two methods still exists since their sampling points are different. As shown in Fig. 2, the sampling point of the proposed ACS method is more close to the updating point than that of the time delay control. Therefore, the value of the inductor current estimated by the ACS control law is closer to the actual value of the inductor current when compared with the time delay control.

III. ACS CURRENT CONTROL ALGORITHMS

Fig. 3 shows waveforms of the inductor current and the reference current when the ACS control strategy is used and the valley inductor current is taken as the control objective, where the buck DC-DC switching converter has trailing-edge modulation and works in the continuous conduction mode (CCM). i_p and i_v represent the peak and valley values of the inductor current, respectively.

For the buck DC-DC switching converter shown in Fig. 1, the rising and falling slopes of the inductor current ripples, m_1 and m_2, as shown in Fig. 3, are given as follows.

$$m_1 = (V_G - V_O)/L, \qquad m_2 = V_O/L \tag{3}$$

By utilizing the above rising and falling slopes, and the sampling values of the inductor current and reference current at the falling edge of δ(t) in the previous cycle, it is possible to establish the digital current control algorithms when using the ACS control strategy, for the control objectives of valley, average, and peak inductor currents, respectively.

A. The Valley Current Control Algorithm

The valley current control principle is shown in Fig. 3. In order to control the inductor current to follow the reference current, the valley value of the inductor current in the nth cycle should be equal to the sampling value of the reference current in the (n-1)th cycle. Thus, the following is obtained:

$$i_v[n] = i_{REF}[n-1] \tag{4}$$

From Fig. 3, i_v[n] can be calculated as:

$$i_v[n] = i_v[n-1] + m_1 d[n]T_s - m_2(1-d[n])T_s \tag{5}$$

For the ACS control, since the peak value of the inductor current in the (n-1)th cycle, i_p[n-1], is sampled, it is necessary to express i_v[n-1] in (5) by i_p[n-1]. From Fig. 3, the following relationship between i_v[n-1] and i_p[n-1] can be obtained:

$$i_v[n-1] = i_p[n-1] - m_2(1-d[n-1])T_s \tag{6}$$

By substituting (6) into (5), i_v[n]can be expressed as:

$$\begin{aligned} i_v[n] &= i_p[n-1] - m_2(1-d[n-1])T_s \\ &\quad + m_1 d[n]T_s - m_2(1-d[n])T_s \end{aligned} \tag{7}$$

By substituting (7) into (4) and rearranging the equation, it is possible to obtain the valley current control algorithm as shown in (8).

$$\begin{aligned} d[n] = &-\frac{m_2}{m_1+m_2} d[n-1] + \frac{1}{(m_1+m_2)T_s} \\ &\cdot (i_{REF}[n-1] - i_p[n-1]) + \frac{2m_2}{m_1+m_2} \end{aligned} \tag{8}$$

B. The Average Current Control Algorithm

Fig. 4 shows the ACS control strategy for the average current control, where in order to control the inductor current to follow the reference current, the average value of the inductor current in the nth cycle is impelled to be equal to the sampling value of the reference current in the (n-1)th cycle.

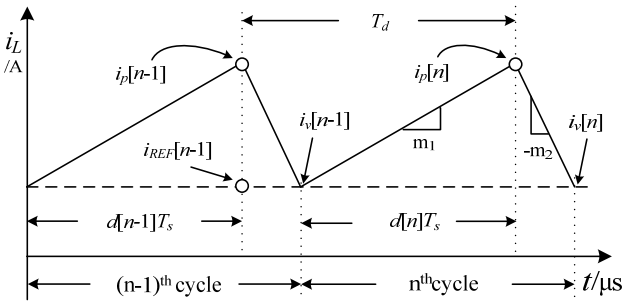


Fig. 3. ACS control strategy for valley inductor current control.

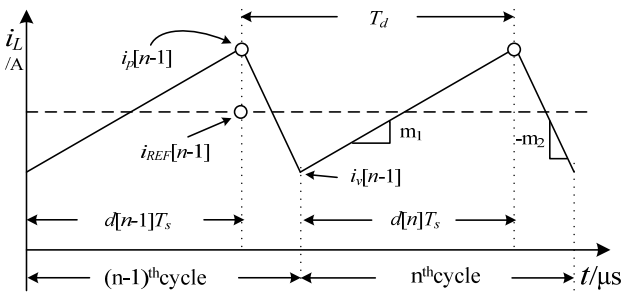


Fig. 4. ACS control strategy for average inductor current control.

Thus, the following equation is obtained:

$$i_{ave}[n] = i_{REF}[n-1] \tag{9}$$

Due to the fact that the inductor current is different during switch on and switch off, the average value of the inductor current in the nth cycle can be calculated based on the subsection integral. Thus, the average value of the inductor current is obtained as:

$$\begin{aligned} i_{ave}[n] &= \frac{1}{T_s}\int_0^{d[n]T_s} (i_v[n-1] + m_1 t)dt \\ &\quad + \frac{1}{T_s}\int_{d[n]T_s}^{T_s} (i_v[n-1] + m_1 d[n]T_s - m_2 t)dt \\ &= i_v[n-1] + (m_1+m_2)d[n]T_s \\ &\qquad \textit{first-order term} \\ &\quad -\frac{1}{2}(m_1+m_2)(d[n])^2 T_s - \frac{1}{2}m_2 T_s \\ &\qquad \textit{second-order term} \end{aligned} \tag{10}$$

The second-order term about d[n] in (10) makes the current control algorithm become complex and difficult to implement by the compensator. Therefore, it is necessary to replace it by other parameters. The ratio of the input and output voltages in the steady-state can be substituted for $(d[n])^2$ in (10). In addition, by using (3), $(d[n])^2$ can be expressed as:

$$(d[n])^2 = \left(\frac{V_O}{V_G}\right)^2 = \frac{m_2^2}{(m_1+m_2)^2} \tag{11}$$

By substituting (11) into (10), it is possible to obtain the expression of the average inductor current as shown in (12).

$$i_{ave}[n] = i_p[n-1] + m_2 d_D[n-1]T_s + (m_1+m_2)d_D[n]T_s - \frac{3m_1m_2+4m_2^2}{2(m_1+m_2)}T_s \quad (12)$$

According to (9) and (12), the average current control algorithm can be derived as shown in (13).

$$d[n] = -\frac{m_2}{m_1+m_2}d[n-1] + \frac{1}{(m_1+m_2)T_s} \cdot (i_{REF}[n-1] - i_p[n-1]) + \frac{3m_1m_2+4m_2^2}{2(m_1+m_2)^2} \quad (13)$$

C. The Peak Current Control Algorithm

Fig. 5 shows the ACS control strategy for the peak current control, where the peak value of the inductor current in the nth cycle is impelled to be equal to the sampling value of the reference current in the (n-1)th cycle.

Thus, the following equation is obtained:

$$i_p[n] = i_{REF}[n-1] \quad (14)$$

The peak value of the inductor current can be calculated by the following equation:

$$i_p[n] = i_p[n-1] - m_2(1-d[n-1])T_s + m_1 d[n]T_s \quad (15)$$

By merging (14) and (15), it is easy to obtain the peak current control algorithm as shown in (16).

$$d[n] = -\frac{m_2}{m_1}d_D[n-1] + \frac{1}{m_1T_s} \cdot (i_{REF}[n-1] - i_p[n-1]) + \frac{m_2}{m_1} \quad (16)$$

So far, the current control algorithms for the three control objectives have been derived for the valley, average, and peak inductor currents, respectively. It is noteworthy that the three current control algorithms have a uniform format in which the duty ratio in the nth cycle can be expressed by a linear combination of the reference current and the peak inductor current in the (n-1)th cycle. Therefore, for a buck DC-DC switching converter with trailing-edge modulation, the current control algorithms with the ACS control strategy can be expressed by the uniform format as shown in (17).

$$d[n] = K_1 d[n-1] + K_2(i_{REF}[n-1] - i_p[n-1]) + K_3 \quad (17)$$

In (17), K_1 is the accumulation factor, which reflects the accumulative effect of the duty ratio of the previous cycle onto that of the present cycle; K_2 is the error coefficient, which reflects the impact of the error between the sampled inductor current and the reference current onto the duty ratio of the present cycle; and K_3 is the offset factor. Here, for the buck DC-DC switching converter with trailing-edge modulation, the control coefficients of the current control algorithms, using the ACS control, K_1, K_2, and K_3, are summarized in TABLE II.

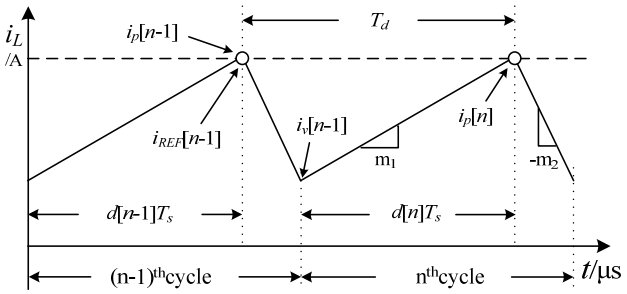


Fig. 5. ACS control strategy for peak inductor current control.

TABLE II
THE CONTROL COEFFICIENTS OF CURRENT CONTROL LAWS USING ACS CONTROL

Control objective	*Control coefficients*		
	K_1	K_2	K_3
Valley current	$-\frac{m_2}{m_1+m_2}$	$\frac{1}{(m_1+m_2)T_s}$	$\frac{2m_2}{m_1+m_2}$
Average current	$-\frac{m_2}{m_1+m_2}$	$\frac{1}{(m_1+m_2)T_s}$	$\frac{3m_2m_2+4m_2^2}{2(m_1+m_2)^2}$
Peak current	$-\frac{m_2}{m_1}$	$\frac{1}{m_1T_s}$	$\frac{m_2}{m_1}$

IV. ANALYSIS AND ELIMINATION OF SUB-HARMONIC OSCILLATION

It is well known that sub-harmonic oscillations may occur in digitally controlled DC-DC switching converters [18-20]. Therefore, it is necessary to investigate the stabilities of above current control algorithms, where the ACS control strategy is used.

A. Analysis of Sub-Harmonic Oscillation

Since the loop bandwidth of a buck DC-DC switching converter is far less than the switching frequency, both the slopes of the inductor current ripple, shown in (3), and the reference current are assumed to be constant in the following analysis.

Fig. 6 shows the mechanism of sub-harmonic oscillations for the ACS peak current control with trailing-edge modulation, where the solid line indicates the steady-state inductor current waveform, and the dotted line shows the inductor current waveform when a perturbation in the peak value, Δi_p[n-1], is added to the steady-state value at the time point of d[n-1]T_s.

According to Fig. 6, the signal value with perturbations is equal to the steady-state value plus a perturbing quantity. Therefore, the following equations can be written:

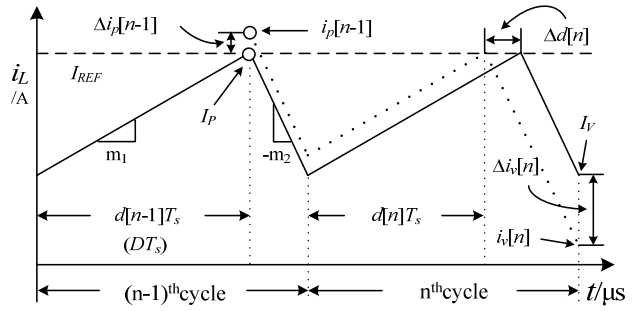


Fig. 6. Sub-harmonic oscillation for the ACS peak current control with trailing-edge modulation.

$$\begin{cases} i_p[n-1] = I_P + \Delta i_p[n-1] \\ i_v[n] = I_V + \Delta i_v[n] \\ d[n] = D + \Delta d[n] \end{cases} \tag{18}$$

Here, I_P, I_V and D are the steady-state values of the peak inductor current, valley inductor current and duty ratio, while Δd[n] and Δi_v[n] are the perturbing-quantities of the duty ratio and valley inductor current in the present cycle, respectively.

It is reasonable to consider that the perturbation of the peak current Δi_p[n-1], which appeared at the time point of d[n-1]T_s, does not affect the duty ratio in the (n-1)th cycle. Therefore, the following relation is obtained:

$$d[n-1] = D \tag{19}$$

Then, by substituting (18) and (19) into (16), and using I_{REF} to replace the reference current, the current control algorithm shown in (16) can be rewritten as:

$$\begin{aligned} D + \Delta d[n] = &-\frac{m_2}{m_1} D + \frac{1}{m_1 T_s} I_{REF} \\ &-\frac{1}{m_1 T_s}(I_p + \Delta i_p[n-1]) + \frac{m_2}{m_1} \end{aligned} \tag{20}$$

By eliminating the steady-state values in (20), it is possible to obtain the perturbing-quantity of the duty ratio of the nth cycle, Δd[n], as shown in (21).

$$\Delta d[n] = -\frac{1}{m_1 T_s}\Delta i_p[n-1] \tag{21}$$

Furthermore, by substituting (18) and (19) into (7) and (21), the relationships between perturbing-quantities of Δd[n], Δi_v[n] and Δi_p[n-1] can be obtained as:

$$\Delta i_v[n] = \Delta i_p[n-1] + (m_1 + m_2)\Delta d[n] T_s \tag{22}$$

$$\Delta i_v[n] = -\frac{m_2}{m_1}\Delta i_p[n-1] = -\frac{D}{1-D}\cdot\Delta i_p[n-1] \tag{23}$$

Then, from (23), the transmissibility of the perturbation η can be derived as:

$$\eta = \frac{\Delta i_v[n]}{\Delta i_p[n-1]} = -\frac{m_2}{m_1} = -\frac{D}{1-D} \tag{24}$$

If the absolute value of η is less than 1, the current control algorithm is stable, and hence no sub-harmonic oscillation phenomena can occur. Thus, according to (24), it can be concluded that perturbations of the inductor current do not lead to sub-harmonic oscillations when the duty ratio does not exceed 0.5 for the ACS peak current control with trailing-edge modulation.

For the ACS valley and average current control algorithms, it is possible to adopt an analysis process similar to the one above to investigate their stabilities. Here only the analysis results are given. The perturbing-quantity of the duty ratio is the same for both the valley and average current control algorithms, as shown in (25).

$$\Delta d[n] = -\frac{1}{(m_1 + m_2)T_s}\Delta i_p[n-1] \tag{25}$$

By merging (22) and (25), it is possible to come to the conclusion that both the perturbing-quantity of the inductor current, Δi_v[n], and the transmissibility of the perturbation, η, are equal to zero. This indicates that for the ACS valley and average current control algorithms, perturbations of the inductor current will not lead to sub-harmonic oscillations for any duty ratio.

B. Elimination of Sub-harmonic Oscillations

In this paper, the digital slope compensation (DSC) method [19], [20] is used to eliminate the sub-harmonic oscillations for the ACS peak current control. As shown in Fig. 7, after the DSC is applied to the reference current, during one switching cycle, the reference current i_{REF} is no longer a constant value, but is a falling straight line with a slope of – m_a (dashed–dotted line).

The control relation for the ACS peak current control with the DSC is changed. It can be expressed as:

$$\begin{aligned} i_p[n] &= I_{REF} - m_a d[n] T_s \\ &= i_{REF}[n-1] - m_a d[n] T_s \end{aligned} \tag{26}$$

Based on (26), it is possible to obtain a new ACS peak current control algorithm by using the derivations in section III. C. This is shown in (27).

$$\begin{aligned} d[n] = &-\frac{m_2}{m_1 + m_a} d[n-1] + \frac{1}{(m_1 + m_a)T_s} \\ &\cdot (i_{REF}[n-1] - i_p[n-1]) + \frac{m_2}{m_1 + m_a} \end{aligned} \tag{27}$$

Furthermore, for the new ACS peak current control algorithm with the DSC, it is possible to derive new expressions for both the perturbing-quantity of the inductor current and the transmissibility of the perturbation by using the derivations in section IV. These are shown as follows:

$$\Delta i_v[n] = -\frac{m_2 - m_a}{m_1 + m_a}\Delta i_p[n-1] \tag{28}$$

$$\eta = \frac{\Delta i_v[n]}{\Delta i_p[n-1]} = -\frac{m_2 - m_a}{m_1 + m_a} \tag{29}$$

In order to eliminate sub-harmonic oscillations, the absolute value of η should be less than 1. From (29) it can be seen that the compensation slope m_a must satisfy the following condition:

$$\frac{m_2}{2} \le m_a \le m_2 \tag{30}$$

Equations (16) and (27) show the ACS peak current control algorithms without the DSC and with the DSC. By comparing (27) with (16), it can be seen that whether the DSC is used or not, the ACS peak current control algorithms are in the uniform format. Therefore, the ACS peak current control algorithm with the DSC can be obtained only by changing the control coefficients of (16) into those of (27). Therefore, there is no need to add any extra slope compensation hardware circuit.

As illustrated in Fig. 7, if the DSC is used and the slope m_a is satisfied with (30), the perturbation of the valley current in the present cycle, $\Delta i_v[n]$, is less than that of the peak current in the previous cycle, $\Delta i_p[n-1]$. Therefore, the perturbation of the inductor current will gradually disappear and eventually recover to its steady-state value. Thus, the sub-harmonic oscillation is eliminated.

V. Experiment Results

To verify the above theoretical analysis of the ACS current control strategies and algorithms, some experiments are carried out using a hardware platform that is based on the structure shown in Fig. 1. In this platform, the digital compensator is implemented by a field programmable gate array (FPGA) from Altera. In addition, the load current is generated by an electronic load instrument N3300A from Agilent. Furthermore, a 9-bit ADCi for sampling the inductor current, an 8-bit ADCv for sampling the output voltage, and an 11-bit DPWM for converting the digital duty ratio into an analog pulse signal, are also used. A buck DC-DC switching converter with trailing-edge modulation operates in the continuous conduction mode (CCM), and the circuit parameters of the power stage are chosen as: V_G=5.0 V, L =2.2 μH, C=2.2 μF, R=2 Ω, and the switching cycle=1 MHz (T_s=1 μs).

The experimental conditions are divided into two cases, 1) case I: duty ratio D=0.36, output voltage V_O=1.8 V, and load current I_L=0.9 A; and 2) case II: D=0.6, V_O=3.0 V, and I_L=1.5 A, while the other circuit parameters are same in both cases as defined above.

Fig. 8 shows the transient response features when the load current is step-changed from 1.9 A to 0.9 A. Here, the ACS current control strategy is used for the three control objectives of valley, peak, and average currents, and the experiment conditions are case I (D=0.36 and V_O=1.8 V). The control coefficients of the current control law for the three current control objectives are summarized in TABLE III.

Fig. 9 shows the amplitude and phase-frequency characteristics of the outer loop gain. The control bandwidth is 100 KHz which is equal to one tenth of the switching frequency, and the phase margin is 83.9 degrees. Fig. 10

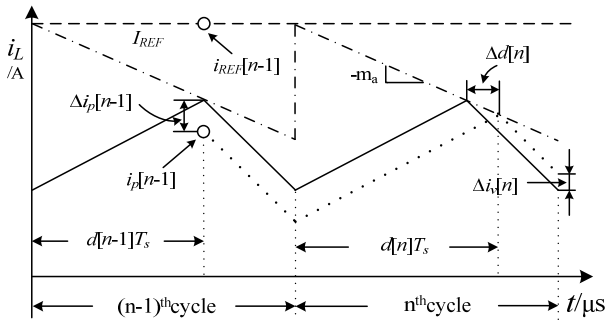
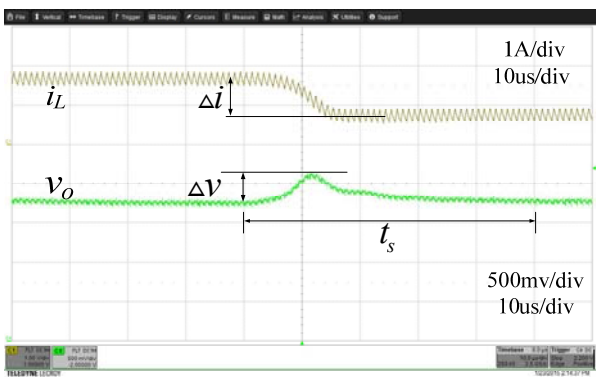
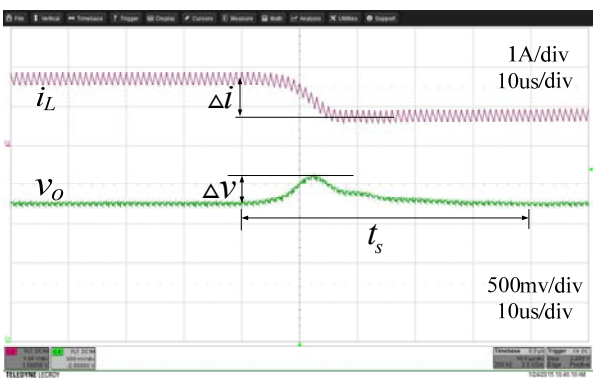


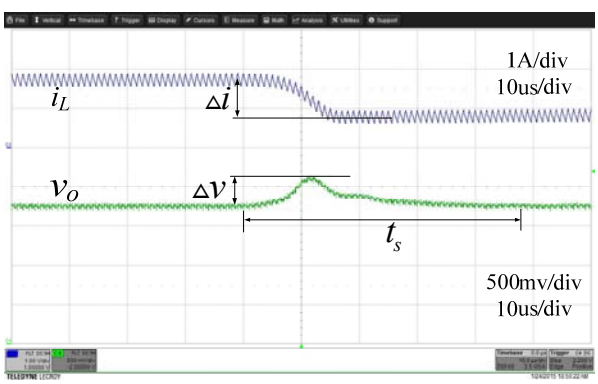
Fig. 7. Elimination of the sub-harmonic oscillation for ACS peak current control with DSC.



(a)



(b)



(c)

Fig. 8 Transient response features of ACS current control strategies for: (a) Valley current control, (b) Peak current control, and (c) Average current control.

TABLE III
CONTROL COEFFICIENTS OF CURRENT CONTROL LAW FOR THREE CONTROL OBJECTIVES

Control objective	*Control coefficients*		
	K_1	K_2	K_3
Valley current	-0.3600	0.4400	0.7200
Average current	-0.3600	0.4400	0.6048
Peak current	-0.3956	0.4835	0.3956

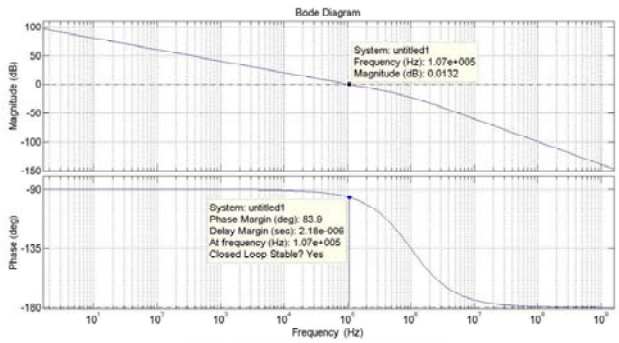


Fig. 9. Amplitude- and phase-frequency characteristics of the outer loop gain.

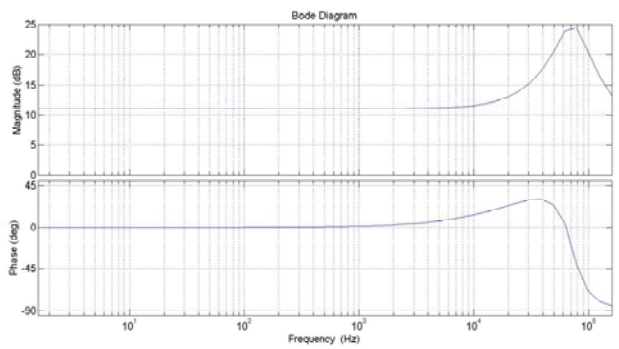


Fig. 10. Amplitude- and phase-frequency characteristics of the inner loop gain for current control simulated by MATLAB.

and Fig. 11 show the amplitude and phase-frequency characteristics of the inner loop gain for the current control using MATLAB and PSIM simulations, respectively. It can be seen that the results of the two simulation match very well, especially in the low-frequency region. This demonstrates the accuracy of the derived model of the current control laws. Since the experiments for the three control objectives are all based on the same outer loop gain and inner loop gain, the above comparison is fair.

It can be seen that, the ACS current control algorithms are all stable, and that the system can generate a well-regulated output voltage. For the transient response features, no overshoot is observed for all three of the control objectives. The transition time, t_s, and the fluctuation voltage, Δv, are summarized in TABLE IV. It can be seen that there is no significant difference in the transient response features for the three control objectives.

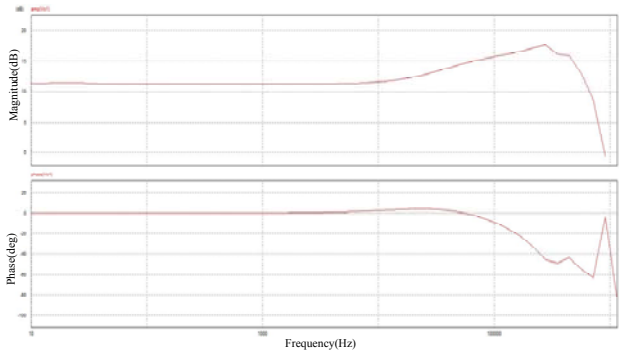


Fig. 11. Amplitude- and phase-frequency characteristics of the inner loop gain for current control simulated by PSIM.

TABLE IV
TRANSIENT RESPONSE OF OUTPUT VOLTAGE WITH ΔI=1A

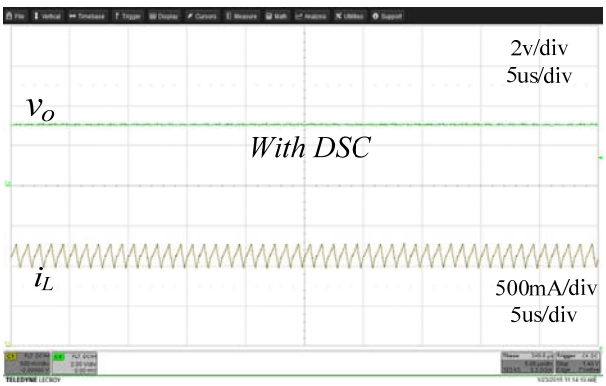
Trailing-edge Modulation	*Control objectives*		
	Valley	*Average*	*Peak*
FluctuationVoltage, Δv	342mV	350mV	340mV
Transition Time, t_s	51μs	47μs	51μs

Fig. 12 (a) and (b) show waveforms of the steady-state output voltage and inductor current using the ACS peak current control, both without and with the DSC, respectively. Here, the experiment condition is case II (D=0.6, V_O=3.0 V, and I_L=1.5 A).

From Fig. 12 (a), it can be observed that in the situation of D=0.6 (D>0.5) and without the DSC, sub-harmonic oscillations occur. As a result, both the output voltage and inductor current are not regulated. However, by using the DSC with m_a=0.75m_2, the sub-harmonic oscillations can be eliminated completely as shown in Fig. 12 (b). The above experimental results verify the sub-harmonic oscillation eliminating method given in section IV.

In order to compare the proposed ACS current control strategy with the traditional deadbeat and time delay current control strategies, the transient response features while using the three current control strategies are measured and compared. Here, the duty ratio is equal to 0.36, and the control objective is the peak value of the inductor current. Fig. 13 shows the measured output voltage and inductor current when the load current is step-changed from 0.9 A to 2.4 A and then back to 0.9 A after 1 ms, where $L1$, $L2$, and $L3$ represent the ACS, deadbeat and time delay current control methods, respectively. From the enlarged waveforms in Fig. 13, it can be observed that, $L1$ nearly overlaps with $L2$, but that $L3$ is obviously delayed compared with $L1$ and $L2$. The transition times of $L1$, $L2$ and $L3$ are 60 μs, 60 μs and 87 μs, respectively. The above experimental results show that the transient response features of the ACS current control are significantly better than those of the time delay current control and the deadbeat current control. This is in accordance with the above theoretical analysis.

(a)



(b)

Fig. 12. Steady-state output voltage and inductor current using ACS peak current control: (a) without DSC and (b) with DSC.

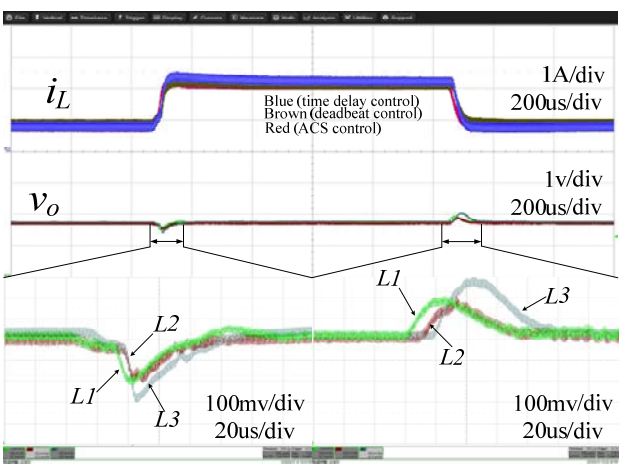


Fig. 13. Measured output voltage and inductor current when using ACS, deadbeat and time delay current control.

It is worth pointing out that since the hardware circuits used in the above experiments have very fast processing speeds, and the duty ratio is relatively large (D=0.36), for the deadbeat current control, calculating and updating the duty ratio can be finished in the present cycle. Therefore, the deadbeat current control has almost same transient response features as the ACS current control. However, with the decrease of the duty ratio and/or the increase of the switching frequency, the transient response features using the deadbeat current control may be degraded unless the processing speed (and cost) of hardware circuit is further increased.

VI. Conclusion

In this paper, the Adjacent Cycle Sampling (ACS) current control strategy, applied for digitally controlled DC-DC switching converters, has been proposed. The available time interval of the ACS current control is approximately equal to one switching cycle. In addition, it is independent of the duty ratio. It was demonstrated by theoretical analysis and experimental results that the ACS control has a faster transient response speed than the time delay control, and that its requirement for loop processing speed can be reduced when compared with the deadbeat control.

A buck DC-DC switching converter with trailing-edge modulation was taken as an example. Digital current control algorithms using the ACS control strategy have been derived for the three control objectives of the valley, average, and peak inductor currents, respectively. The experimental results revealed that there is no significant difference in the transient response features for the three control objectives.

The sub-harmonic oscillations of the above current control algorithms were analyzed. For the ACS peak current control, sub-harmonic oscillations will occur when the duty ratio exceeds 0.5. However, for the ACS valley and average current controls, no sub-harmonic oscillations exit for any duty ratio. Sub-harmonic oscillations occurring in the ACS peak current control can be eliminated using the digital slope compensation (DSC) method, in which the compensation slope m_a must satisfy $0.5m_2 \leq m_a \leq m_2$. The experimental results have verified the theoretical analysis very well.

In this paper, although the ACS digital current control algorithms have only been studied for buck DC-DC switching converters with trailing-edge modulation, the ACS current control strategy can be easily expanded to other structures of DC-DC switching converters, such as boost, buck-boost and multi-phase converters, or expanded to other modulation modes, such as leading-edge, trailing-triangle, and leading-triangle modulations.

Acknowledgment

This research is supported by the National Natural Science Foundation of China (No. 61376034), Shaanxi province science and technology innovation project (No.2015KTZDGY03-03) and Graduate Starting Seed Fund of Northwestern Polytechnical University (No. Z2015138).

References

[1] S. Chunlei, B. C. Walker, E. Zeisel, B. Hu, and G. H. McAllister, "A Highly Integrated Power Management IC for Advanced Mobile Applications," *IEEE Custom Integrated Circuits Conf.(CICC)*, pp. 85-88, Sep. 2006.

[2] B. Sahu and G. A. Rincon-Mora, "A high-efficiency, dual-mode, dynamic, buck-boost power supply IC for portable applications," in *18th Int. Conf. VLSI Design*, pp. 858-861, Jan. 2005.

[3] Z. Tao, X. Jianping, B, and B. Francois, "Analog-to-digital converter architectures for digital controller of high-frequency power converters," in *32nd Annual Conf. Industrial Electronics(IECON)*, pp. 2471-2476, Nov. 2006.

[4] A. Prodic, D. Maksimovic, and R. W. Erickson, "Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter," in *27th Annual Conf. of the Industrial Electronics Society*, Vol. 2, pp. 893-898, Nov./Dec. 2001.

[5] L. Pengfei, D. Bhatia, X. Lin, and R. Bashirullah, "A 90–240 MHz Hysteretic Controlled DC-DC Buck Converter With Digital Phase Locked Loop Synchronization," *IEEE J. Solid-State Circuits,* Vol. 46, No. 9, pp. 2108-2119, Sep. 2011.

[6] M. S. Manoharan, A. Ahmed, and J.-H. Park, "Peak-Valley Current Mode Controlled H-BridgeInverter with Digital Slope Compensation for Cycle-by-Cycle Current Regulation," *Journal of Electrical Engineering and Technology*, Vol. 10, No. 5, pp. 709-718, Oct. 2015.

[7] G. Zhou, J. Xu, C. Mi, and Y. Jin, "Effects of modulations on the sub-harmonic oscillations of digital peak current and digital valley current controlled switching DC-DC converters," in *IEEE. 6th Int. Power Electronics and Motion Control Conf.(IPEMC)*, pp. 1347-1352, May 2009.

[8] H. Siyu and R. M. Nelms, "Comparison of three implementations of digital average current control for DC-DC converters," in *IEEE 40th Annual Conf. Industrial Electronics Society(IECON),* pp. 1337-1342, Oct./Nov. 2014.

[9] G. Zhou, J. Xu, J. Wang, and Q. Mu, "Improved digital average current control of buck converter with dual-edge modulation," in *Int. Conf. Communications, Circuits and Systems(ICCCAS)*, pp.1309-1313, May 2008.

[10] F. Kurokawa and K. Kajiwara, "A novel fast average current mode digital control for DC-DC converter," in *IEEE 9th Int. Conf. Power Electronics and Drive Systems(PEDS),* pp.1143-1148, Dec. 2011.

[11] M. Aime, G. Gateau, and T. A. Meynard, "Implementation of a peak current control algorithm within a field programmable gate array," *IEEE Trans. Ind. Electron.,* Vol. 54, No. 1, pp. 406-418, Feb. 2007.

[12] M. Ferdowsi, "An estimative current mode controller for DC-DC converters operating in continuous conduction mode," *in Proc. IEEE Appl. Power Electron. Conf.*, pp. 4, Mar. 2006.

[13] G. Zhou and J. Xu, "Digital Average Current Controlled Switching DC–DC Converters With Single-Edge Modulation," *IEEE Trans. Power Electron.*, Vol. 25, No. 3, pp.786-793, Mar. 2010.

[14] S. Bibian and J. Hua, "Time delay compensation of digital control for DC switch mode power supplies using prediction techniques," *IEEE Trans. Power Electron.*, Vol. 15, No. 5, pp. 835-842, Sep. 2000.

[15] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 411-419, Jan. 2003.

[16] G. Zhou, J. Xu, Y. Jin, and W. Wang, "Transient performance comparison on digital peak current controlled switching dc-dc converters in DCM with different digital pulse-width modulations," in *IEEE 6th Int. Conf. Power Electronics and Motion Control(IPEMC)*, pp. 315-319, May 2009.

[17] A. Ehrhart, B. Wicht, M. Lin, Y.-S. Huang, L. Yuhuei, and C. Kehorng, "Adaptive pulse skipping and adaptive compensation capacitance techniques in current-mode buck-boost DC-DC converters for fasttransient response," in *IEEE 10th Int. Conf. Power Electronics and Drive Systems(PEDS)*, pp. 373-378, Apr. 2013.

[18] C. Lin and W.-H. Ki, "A circuit-oriented geometrical approach in predicting subharmonic oscillation of dc-dc converters with voltage-mode control," in *IEEE Int. Symp. Circuits and Systems(ISCAS)*, pp. 962-965, Jun. 2014.

[19] T. Grote, F. Schafmeister, H. Figge, N. Frohleke, P. Ide, and J. Bocker, "Adaptive digital slope compensation for peak current mode control," in *IEEE Energy Conversion Congress and Exposition(ECCE)*. pp. 3523-3529, Sep. 2009.

[20] M. Hallworth and S. A. Shirsavar, "Microcontroller-Based Peak Current Mode Control Using Digital Slope Compensation," *IEEE Trans. Power Electron.*, Vol. 27, No. 7, pp. 3340-3351, Jul. 2012.

Tingcun Wei was born in Shaanxi, P. R. China, in 1960. He received his B.S. degree in Electrical and Electronics Engineering from the Xi'an University of Science and Technology, Xi'an, P. R. China, in 1982; his M.S. degree in Electronics and Information Engineering from Northwestern Polytechnical University, Xi'an, P. R. China, in 1988; and his Ph.D. degree in Electrical and Communication Engineering from Tohoku University, Sendai, Japan, in 1999. He is presently working as a Professor at Northwestern Polytechnical University. His current research interests include analog and mixed-signal ASIC/SoC designs, digitally controlled DC-DC converters, flat panel display drivers and controller ICs.

Yulin Wang received his B.S. degree in Microelectronics from Northwestern Polytechnical University, Xi'an, China, in 2013; where he has been working towards his M.S. degree in Power Electronics and Digitally Controlled DC-DC Converters since 2013. His current research interests include the synthesis, modeling, and digital control of switching power converters, and analog and mixed-signal ASIC/SoC designs.

Feng Li was born in 1978. He received his B.S., M.S., and Ph.D. degrees in Computer Science and Technology from Northwestern Polytechnical University, Xi'an, P. R. China, in 2006, 2008, and 2012, respectively. His current research interests include digitally controlled DC-DC switching converters and base-band digital signal processing.

Nan Chen was born in Xi`an, P. R. China, in 1988. She received her B.S. degree in Electronic Information Engineering from Xinyang Normal University, Xinyang, P. R. China, in 2010; and her M.S. degree in Software Engineering from Northwestern Polytechnical University, Xi'an, P. R. China, in 2013; where she has been working towards her Ph.D. degree since 2013. Her current research interests include analog and mixed-signal integrated circuit designs, and power electronics such as digitally controlled DC-DC switching converters and energy harvesting circuits.

Jia Wang received his B.S. and Ph.D. degrees in Computer Science and Technology from Northwestern Polytechnical University, Xi'an, China, in 2006 and 2013, respectively. He received his Ph.D. degree in Instrumentation and Microelectronics from the University of Strasbourg, Strasbourg, France, in 2013. He is presently working an Assistant Professor at Northwestern Polytechnical University. His current research interests include power management ICs, and low noise, low power consumption readout circuits for radiation detectors.