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An Improved SPWM Strategy to Reduce Switching in Cascaded Multilevel Inverters

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Abstract

The analysis of the switch status of each unit module of a cascaded multi-level inverter reveals that the working condition of the switch of a chopper arm causes unnecessary switching under the conventional unipolar sinusoidal pulse width modulation (SPWM). With an increase in the number of cascaded multilevel inverters, the superposition of unnecessary switching gradually occurs. In this work, we propose an improved SPWM strategy to reduce switching in cascaded multilevel inverters. Specifically, we analyze the switch state of the switch tube of a chopper arm of an H-bridge unit. The redundant switch is then removed, thereby reducing the switching frequency. Unlike the conventional unipolar SPWM technique, the improved SPWM method greatly reduces switching without altering the output quality of inverters. The conventional unipolar SPWM technique and the proposed method are applied to a five-level inverter. Simulation results show the superiority of the proposed strategy. Finally, a prototype is built in the laboratory. Experimental results verify the correctness of the proposed modulation strategy.

Key words: Cascaded multi-level inverter, Improved SPWM strategy, Unipolar SPWM, Unnecessary switching frequency

I. INTRODUCTION

In high power applications, a traditional two-level voltage source converter cannot meet the needs of industrial production because of the breakdown voltage of the power switch. Hence, multilevel converters with unique structural features, such as high voltage operating capability, low dv/dt, and good harmonic performance, have received increasing attention in high power applications [1]–[4]. The voltage and power level of a multi-level inverter with a modular design can be flexibly changed by adjusting the number of sub-modules and can be extended to any output level to solve the problems of the traditional two-level and tri-level electromagnetic interferences and high output voltage harmonics [5]. Modular multi-level high-voltage direct current technology has broad application prospects in areas such as new energy access, passive power grid, and asynchronous grid interconnection and has thus received adequate attention from academia and various industries [6], [7]. The cascaded H-bridge (CHB) multi-level converter is a good representative because it features a modular structure, simple control, and other characteristics that are favorable in practical industrial applications.

Modulation technology is the key technology of CHB multilevel converters. In principle, all modulation methods aim to generate trains of pulses with a time average that approximates a target reference waveform at any instant. Thus far, several modulation methods based on the conventional carrier-based sinusoidal pulse width modulation (SPWM) method have been proposed for multi-level inverters [8]; such methods include subharmonic PWM, space-vector PWM, selective harmonic elimination, hybrid modulation methods, and many others [9]–[11]. The carrier phase-shifted (CPS) SPWM is one of the conventional control schemes employed in cascaded multi-level inverters [12], [13]. The work in [14] pointed out that the output power of each unit is balanced with CPS control. However, other modulations cannot achieve such power balance spontaneously, with such case leading to an imbalance in the DC link voltages that are fed to an inverter. These imbalanced voltages, which are represented by ripples in DC links, have a negative effect on output quality because they cause distorted output waveforms with low-frequency harmonics. This

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phenomenon can lead to the degradation of load performance [15], [16], [17]. When CPS-SPWM is employed in the study of the CPS angles of cascaded multi-level inverters, each unit adopts double frequency SPWM such that a PWM pulse generator becomes a requirement of each switching device. However, as the number of cascaded cells in a cascaded inverter increases, the need for a PWM pulse generator increases. This requirement is a significant problem for the digital implementation of CPS-SPWM. The work in [17] aimed to address this problem by introducing a unipolar SPWM to a cascaded multi-level inverter; the method can reduce the required PWM generator by half without altering the system performance. However, conventional unipolar SPWM technologies give rise to unnecessary switch conditions, which cause an increase in cascaded cells.

According to the literature [17], an improved SPWM strategy is proposed in the present work to reduce switching for cascaded multi-level inverters without altering output performance. The simulation and experiment verify the effectiveness of the strategy.

II. CASCADED H-BRIDGE MULTI-LEVEL INVERTER

A. Topology Description

Fig. 1 shows the main circuit configuration of the CHB multi-level converter. The building block of this topology consists of several identical H-bridge cells. The total output voltage is u_0 because all cells are connected in series. Cell-1 single H-bridge can generate three different output voltage levels, namely, $+V_{DC}$, 0, and $-V_{DC}$, by connecting the DC source to the output terminals through the use of various switching combinations of four semiconductor switches.

A five-level cascaded multi-level inverter comprises two separate DC sources and produces five output voltage levels, namely, $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$, and $-2V_{DC}$. Fig. 1 shows a cascaded five-level inverter. The relationship between the DC link voltage and the output voltage for one cell is derived with the switch states, which are listed in Table I.

The five-level inverter utilizes two independent DC sources, which consequently create an output voltage with five levels. In general, if Ns is the number of independent DC sources, then the following relations apply [21]:

$$m = 2Ns + 1 \tag{1}$$

$$N = 2(m - 1) \tag{2}$$

where m is the number of levels and N is the number of switching devices.

B. CPS-PWM Based on Unipolar SPWM

According to the operation principle of CPS-PWM based on unipolar SPWM, the switch tubes of each chopper arm are used to reduce the switching frequency of SPWM. A corresponding triangular carrier wave sequentially removes $2\pi/N$ phase angles. This carrier wave is compared with the same sine modulation wave to produce N groups of PWM pulse signals, which drive the switch tubes of a chopper arm. Each cell output voltage is superimposed to obtain an output voltage waveform.

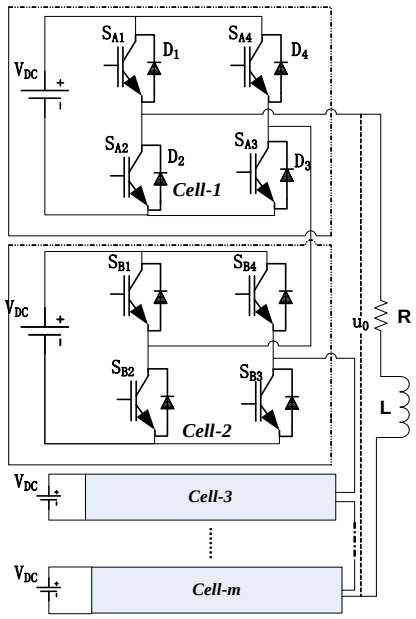

Fig. 1. Single-phase cascaded H-bridge multi-level inverter.

TABLE I
SWITCH STATES OF FIVE-LEVEL H-BRIDGE MULTI-LEVEL INVERTER (FOR TWO CELLS)

Cell-1				Cell-2				Output voltages
S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{B1}	S_{B2}	S_{B3}	S_{B4}	u_0
1	0	1	0	1	0	1	0	$+2V_{DC}$
1	0	1	0	1	0	0	1	V_{DC}
1	0	1	1	0	1	1	0	V_{DC}
1	0	0	1	1	0	1	1	V_{DC}
0	1	1	0	1	0	1	0	V_{DC}
1	0	1	1	0	1	0	1	0
0	1	0	1	1	0	1	0	0
1	0	0	1	1	0	0	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	1	1	0	0	1	1	0	0
1	0	0	1	0	1	0	1	$-V_{DC}$
0	1	1	0	0	1	0	1	$-V_{DC}$
0	1	0	1	1	0	0	1	$-V_{DC}$
0	1	0	1	0	1	1	0	$-V_{DC}$
0	1	0	1	0	1	0	1	$-2V_{DC}$

III. IMPROVED SPWM STRATEGY TO REDUCE SWITCHING

A cascaded multi-level inverter is composed of several single-phase full-bridge inverter cells. Thus, the SPWM strategy for single-phase full-bridge inverters is the foundation of the SPWM strategy for cascaded multi-level inverters. The following discussion refers to Cell-1 shown in Fig. 1 because its operating principle is the same as those of the other cells.

A. Analysis of Discharge Circuit

As shown in Fig. 1, the work of S_{A1} is similar to that of S_{A2}. This study mainly analyzes the working condition of S_{A3}. In a modulation cycle, the inductance current cannot break; hence, when the switch S_{A1} is turned off, switch tube S_{A3} discharges the inductance current, thereby guaranteeing that the load current changes according to the sine law until it reduces to zero. With the reversal of the current direction, S_{A3} does not affect the inverter circuit. Thus, if S_{A3} keeps switching, it causes an unnecessary switch state under a conventional unipolar SPWM. In a cascaded multi-level inverter, the increase in the number of cascaded units results in accumulation.

In addressing the aforementioned problem, this study analyzes the switch state of S_{A3} after the S_{A1} is turned off in a modulation period. When S_{A3} is turned on, the discharge circuit 1 is composed of S_{A3}, D_2, and the load. When S_{A3} is turned off, the discharge loop 2 consists of D_2, D_4, the power supply, and the load. As a result of the turning off of S_{A1}, loop 1 or loop 2 facilitates the discharging of the load current to zero. Therefore, two assumptions are formulated. Hypothesis 1 states that if the discharge circuit only comprises loop 1, then S_{A3} and S_{A4} are turned on simultaneously; as such condition is not allowed in the inverter, assumption 1 is invalid. Hypothesis 2 states that the discharge circuit only comprises loop 2; the following discussion describes the analysis of hypothesis 2.

For the proposed hypothesis 2, the pulse signals of S_{A3} and S_{A1} follow the logic operation shown in Fig. 1.

$$\begin{cases} ugA3' = ugA3 * ugA1 \\ ugA1' = ugA1 \end{cases} \tag{3}$$

ugA3' and *ugA1'* are used instead of *ugA3* and *ugA1*, as shown in Fig. 3.

Fig. 3(b) shows the current waveform of full-bridge inverter from Fig. 2(b), which is compared with the conventional unipolar SPWM under the same conditions.

In a modulation cycle, the discharge process consists of two discharge circuits, which work alternately to make the output current change according to the sine law. Fig. 3b shows that by using the pulse signal shown in Fig. 2b in the inverter shown in Fig. 1, the output current rapidly becomes zero. This effect is explained as follows. With S_{A1} and S_{A3} in shutdown states, the entire discharge circuit only comprises loop 2. S_{A3} and D_2 fail to form loop 1 together with loop 2 to guarantee the change in the output current according to the sine rule. As a result, the output current waveform emerges in the case depicted in Fig. 3(b). Thus, when S_{A1} is turned off, S_{A3} cannot remain in the off state.

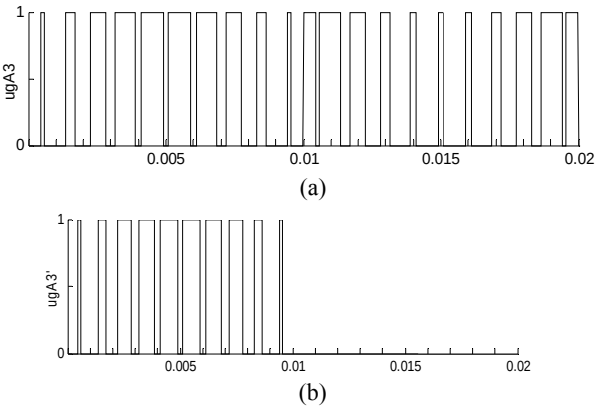

Fig. 2. S_{A3} pulse signal under the two hypotheses.

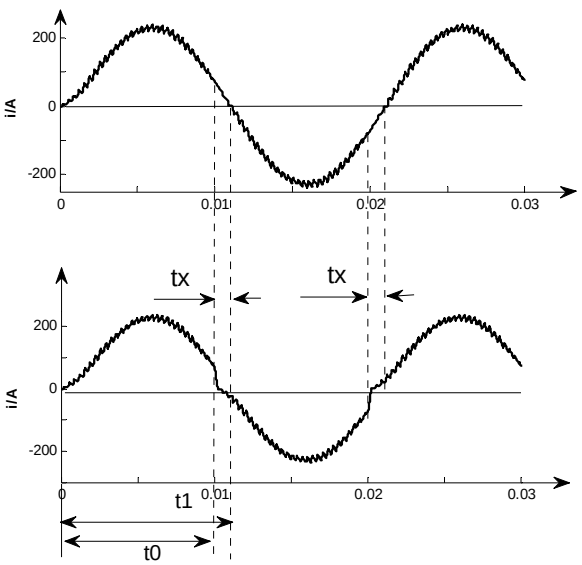

Fig. 3. Comparison of output current waveforms.

In view of the problem that arises from hypothesis 2, the following improvement is implemented. During a modulation period, the pulse signals of S_{A1} and S_{A2} remain unchanged. When S_{A1} is turned off, the S_{A3} pulse signal remains with the conventional unipolar SPWM until the load current is decreased to zero. Then, S_{A3} is turned off until the arrival of the next cycle. This process ensures that the two discharge circuits work alternately to realize the changes in output current in accordance with the sine law while reducing the switching frequency. This modulation strategy is proposed for cascaded multi-level inverters to minimize switching. Fig. 4 shows the operating principle based on the improved SPWM (for two cells).

As shown in Fig. 4, the inductor current is reduced to zero after tx when S_{A1} is turned off. Then, S_{A3} is turned off until the arrival of the next cycle.

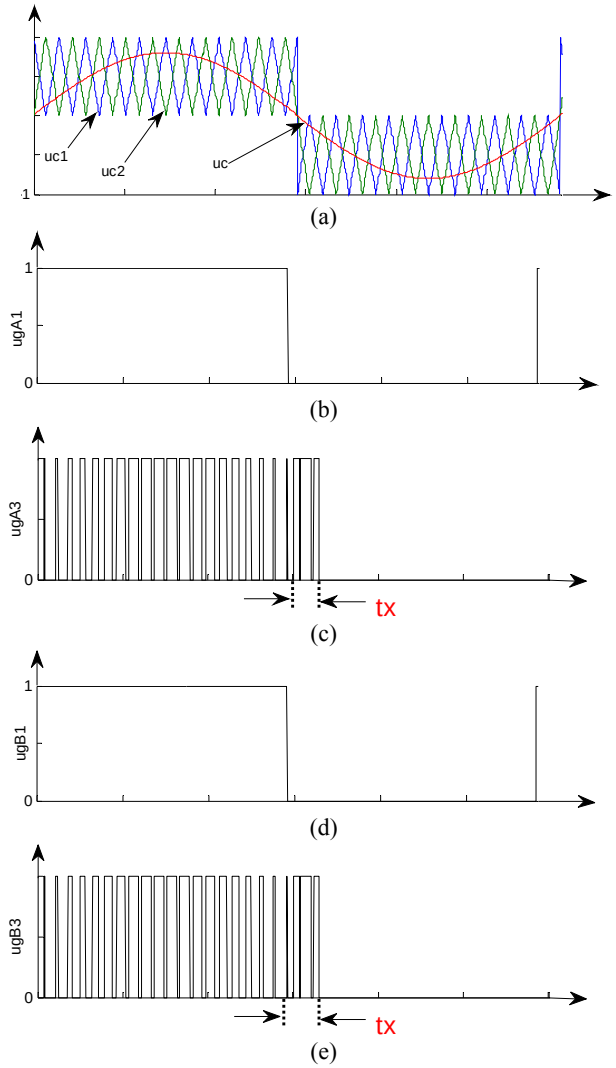

Fig. 4. Operating principle based on improved SPWM.

B. Calculation of Load Discharge Time tx

In Fig. 4, *tx* is the load discharge time. When S_{A1} is turned off, the load discharge time *tx* needs to be calculated. The following describes the calculation of *tx*.

Given a passive linear load, the fundamental component I_{01} lags the fundamental voltage U_{01}, and the phase difference is

$$\varphi = \arctan \omega L_0 / R_0 \tag{4}$$

In the analysis of Fig. 2, when S_{A1} is turned off, the load voltage is zero. Thus, at this time, the load current value I_0 can be determined by Equation (2). This time is defined as the zero time, and the acquired current is an initial current I_0.

When S_{A3} is turned on, the discharge circuit 1 discharges the inductance current. The loop equation is

$$L\frac{di}{dt_a} + iR = 0 \tag{5}$$

The following can then be obtained:

$$i = I_0 e^{-\frac{R}{L}t_a} \tag{6}$$

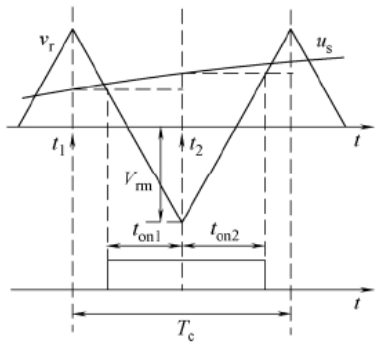

Fig. 5. Pulse generation method based on irregular sampling.

When S_{A3} is turned off, the discharge circuit 2 discharges the inductance current. The loop equation is

$$L\frac{di}{dt_b} + iR + U = 0 \tag{7}$$

The following can then be obtained:

$$C = i_0 + \frac{U}{R} \tag{8}$$

where i_0 is the output current value of the load after a circuit discharge.

$$i = C * e^{-\frac{R}{L}t_b} - \frac{U}{R} \tag{9}$$

t_a and t_b are the discharge times of the single circuits 1 and 2, respectively. The calculation of the single discharge loops 1 and 2 is the same as that of the width of the S_{A3} pulse. The pulse generation method based on irregular sampling is shown in Fig. 5.

The setting for the modulation function is

$$us = \sin(\omega t + \varphi) \tag{10}$$

*U*m—the modulation amplitude,

$\omega 1$—the angular frequency of the modulation wave,

ϕ—the initial phase angle of the modulation wave.

The carrier ratio is F = ωc/ω1 ≥ 1, the modulation ratio is M = Um/Vrm, and ωc is the angular frequency of the carrier wave.

According to Fig. 5, the pulse width t_{on} can be obtained easily. Then,

$$t_{on} = t_{on1} + t_{on2} \tag{11}$$

$$\begin{cases} t_{0n1} = \dfrac{Ts}{4}[1 + M\sin(\omega t_1 + \varphi)] \\ t_{0n2} = \dfrac{Ts}{4}[1 + M\sin(\omega t_2 + \varphi)] \end{cases} \tag{12}$$

According to (7), (9), (11), and (12), the total discharge times *Ta* and *Tb* of the discharge circuits 1 and 2 can be calculated, respectively. The total discharge time *tx* is

$$tx = Ta + Tb \tag{13}$$

In an internal modulation cycle, the switching frequency of a single cascaded unit is reduced by the switch of the chopper arm.

$$P = 2(1 - \frac{tx + \frac{Ts}{2}}{Ts}) * 100\% \quad (14)$$

where P is the percentage reduction in switching frequency in comparison with that in the case of a conventional unipolar SPWM. Ts is the modulation period $tx \le Ts/2$.

As shown in Equation (14), the switching frequency greatly decreases in comparison with that under the conventional unipolar SPWM.

To prevent the phenomenon in which the inductor current cannot be fully discharged to zero because of limited time, *tx* can be calculated up to a large value, that is, the load current value must be calculated up to the zero-crossing point or until a negative value is reached. Doing so guarantees that the load current is discharged to zero completely.

The pulse waveforms of S_{A3} and S_{A4} under the proposed method are obtained from the following logical formula:

$$\begin{cases} ugA3' = ugA3 * ugx \\ ugA4' = ugA4 * ugx' \\ ugA1' = ugA1 \\ ugA2' = ugA4 \end{cases} \quad (15)$$

Here, *u*g1′, *u*g2′, *u*g3′, and *ug4′* are used instead of *ug1, ug2, ug3,* and *ug4,* respectively.

ugx is a square wave signal whose period is Tx and duty cycle is

$$D = \frac{Tx/2 + tx}{Tx} \times 100\% \quad (16)$$

ugx′ is a square wave signal whose phase advance *ugx* is 180°.

IV. Simulation Analysis and Experimental Verification

A. Simulation Analysis

To verify the effectiveness of the proposed method, simulations are performed by using Matlab/Simulink. The single-phase CHB, which comprises two cells and five output voltage levels, is built to compare the proposed method and the conventional unipolar SPWM. Each DC source voltage is 600 V. The carrier frequency for both modulation methods is 2 kHz. The complete parameters for the simulation system are listed in Table II.

Fig. 6 shows the switch pulse of the chopper arm, output voltage waveform, and spectrum under the conventional unipolar SPWM. Fig. 8 illustrates the switch pulse of the chopper arm (the switch state of the chopper arm is the same as that under the conventional unipolar SPWM), output voltage waveform, and spectrum under the proposed method. We can calculate tx = 0.002. Figs. 6(a) and 7(a) show the switch states of the chopper arm with two topologies. The switch frequency of the chopper arm in the proposed method is reduced by 40% in comparison with that under the conventional topology. Figs. 6(b) and 7(b) show that the

TABLE II
Simulation Parameters

Output frequency	50 Hz
Switching frequency	2 kHz
Output voltage level	5
Load resistance	10 Ω
Output filter inductance	20 mH

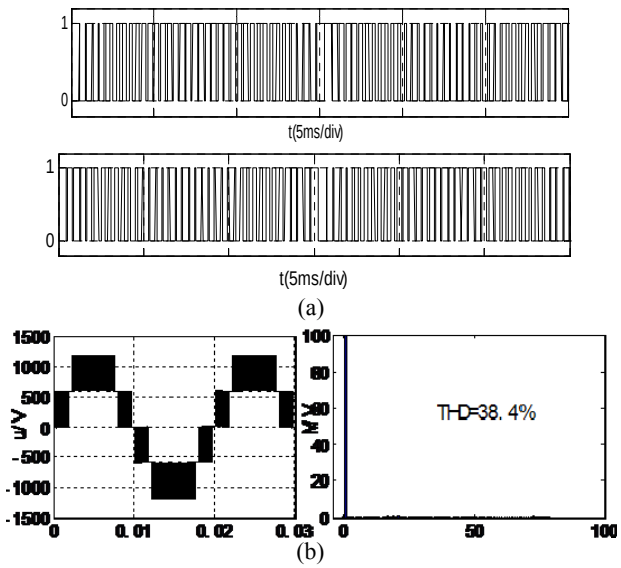

Fig. 6. Output voltage waveform and spectrum under the conventional unipolar SPWM modulation.

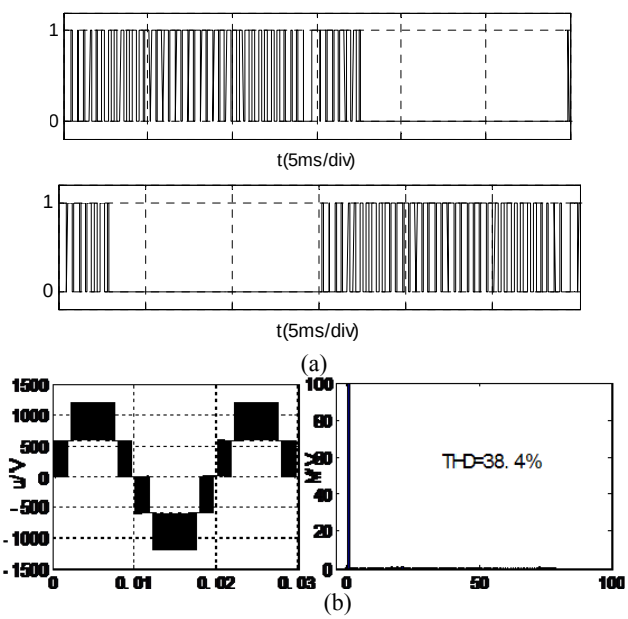

Fig. 7. Output voltage waveform and spectrum under the improved SPWM.

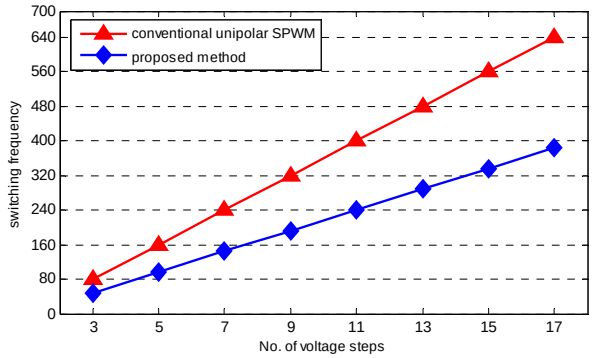

Fig. 8. Comparison of switching frequency.

Fig. 9. Prototype of single-phase inverter.

output voltage waveform and total harmonic distortion (THD) are equal under the two modulation modes.

According to Equation (14), we compare the switching frequencies of the chopper arm under the two modulation modes in a modulation cycle, with the switch states of the chopper arm kept constant. Fig. 8 shows that the switching frequency under the proposed method is less than that under the conventional topology and that the gap becomes obvious as the voltage steps increase. Notably, the output performance remains unchanged.

Figs. 6, 7, and 8 show that the simulation results are consistent with the theoretical analysis. Thus, the simulation verifies the correctness and effectiveness of the proposed method.

B. Experimental Verification

To verify the correctness of the proposed method, a laboratory prototype of a low-voltage single-phase inverter is set up (Fig. 9). The setup mainly comprises two prototype platforms: a single-phase CHB with two cells and the control and drive platform. The TMS320F2812 DSP chip serves as the main chip. The conventional unipolar SPWM method and the proposed method are applied to the prototype, and their output results are compared. The experimental parameters are as follows: the DC supply voltage is 60 V, modulation ratio is 0.8, switching frequency is f = 3 kHz, load resistance is 100 Ω, and inductance is 10 mH. The DSP sampling data are imported into the Matlab workspace, and the experimental

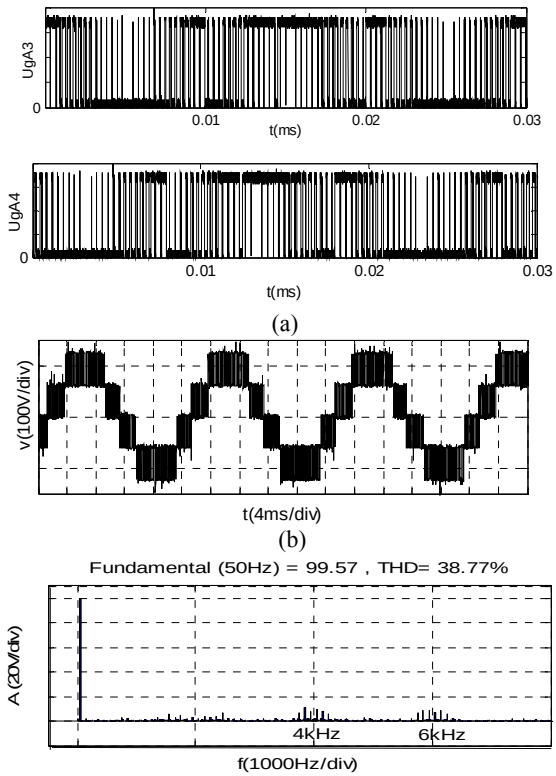

Fig. 10. Waveform and spectrum under the conventional unipolar SPWM.

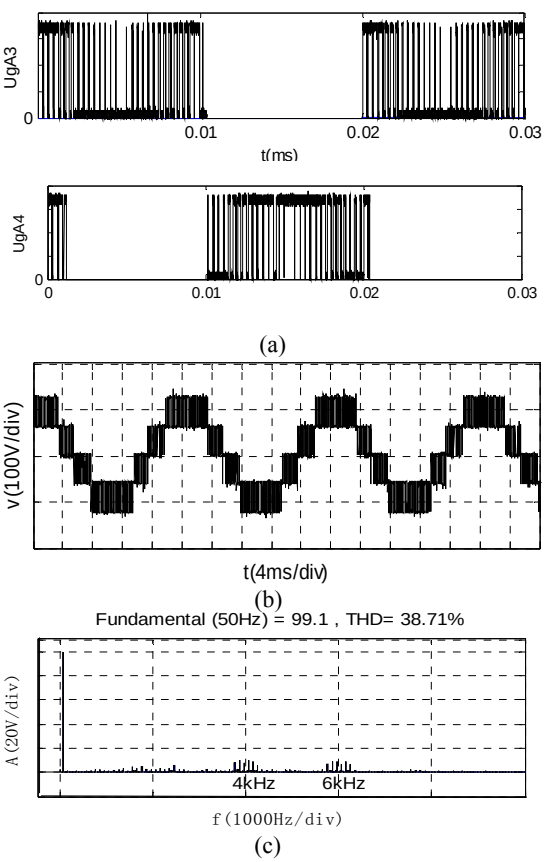

Fig. 11. Waveform and spectrum under the improved SPWM.

waveforms are obtained.

Fig. 10 shows the pulse signal of the chopper arm on Cell-1, the experimental waveforms of the conventional unipolar SPWM, and the spectrum of the output voltage.

Fig. 11 shows the pulse signal of the chopper arm on Cell-1 (the switch state of the chopper arm is the same as that under the conventional unipolar SPWM), experimental waveforms of the proposed approach, and spectrum of the output voltage.

Fig. 11(a) shows a reduction in switching in the modulation cycle by approximately 49%. According to Equation (14) and the experimental parameters, tx = 0.0001 s, and P = 49.5%.

As indicated in the comparison of Figs. 10 and 11, the THDs of the output voltage under the two modulation modes are 38.77% and 38.71%, which show good agreement with the theoretical analysis and simulation results. The experimental results show that the proposed method can reduce switching frequencies without altering the output performance. The experimental results verify the validity of the proposed method.

V. Conclusion

An improved SPWM strategy is proposed to reduce switching for a cascaded multi-level inverter and thereby address the problem of unnecessary switching under the conventional unipolar SPWM method. The proposed strategy mainly focuses on the switch states of a chopper arm at each cascaded unit and eliminates redundant switching. Moreover, the proposed method significantly reduces switching frequencies without altering the output performance of cascaded multi-level inverters. As indicated by the simulation and experimental results, the proposed modulation decreases the switching frequency by approximately 49% in comparison with the value under the conventional unipolar SPWM. Therefore, the effectiveness of the proposed modulation strategy is verified.

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