JPE 16-2-16

http://dx.doi.org/10.6113/JPE.2016.16.2.553
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Design and Implementation of an FPGA-based Real-time Simulator for a Dual Three-Phase Induction Motor Drive

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Abstract

This paper presents a digital hardware implementation of a real-time simulator for a multiphase drive using a field-programmable gate array (FPGA) device. The simulator was developed with a modular and hierarchical design using very high-speed integrated circuit hardware description language (VHDL). Hence, this simulator is flexible and portable. A state-space representation model suitable for FPGA implementations was proposed for a dual three-phase induction machine (DTPIM). The simulator also models a two-level 12-pulse insulated-gate bipolar transistor (IGBT)-based voltage-source converter (VSC), a pulse-width modulation scheme, and a measurement system. Real-time simulation outputs (stator currents and rotor speed) were validated under steady-state and transient conditions using as reference an experimental test bench based on a DTPIM with 15 kW-rated power. The accuracy of the proposed digital hardware implementation was evaluated according to the simulation and experimental results. Finally, statistical performance parameters were provided to analyze the efficiency of the proposed DTPIM hardware implementation method.

Key words: Device simulation, Field-programmable gate array, Multiphase drive, Real-time simulation

I. INTRODUCTION

Recently, digital hardware implementations of real-time simulators have been widely performed in several research fields. In particular, the design and development of power electronic devices and electrical drives have greatly benefited from the advances associated with real-time simulation techniques [1]–[4]. In electrical drive applications, the controller stage is typically subjected to several cycles of testing and redesigns before prototyping. The testing and redesign processes are conducted using an expensive facility equipped with power converters, electrical motors, sensors, switchgears, and other test equipment. The highly active research area in this field is justified in terms of implementation costs. Real-time simulators can accurately and efficiently model electrical drives and provide an alternate means for testing controller performance in hardware-in-the-loop (HIL) configurations [5]–[8]. This approach substantially reduces costs, human resources, power consumption, and the required physical space while providing immunity to damages in cases of controller malfunction [9]–[11]. Real-time simulators have been proven to be viable for several electrical motors and drives, such as permanent magnet synchronous motors [12], brushless DC motors [13], and three-phase induction motors [14].

In the present work, a novel implementation of a real-time simulator of a dual three-phase induction machine (DTPIM) is developed by employing a discrete version of the mathematical model using a state-space representation. The most suitable option in terms of cost is to implement the simulator using a standard PC. However, this approach does

Manuscript received May 9, 2015; accepted Nov. 1, 2015
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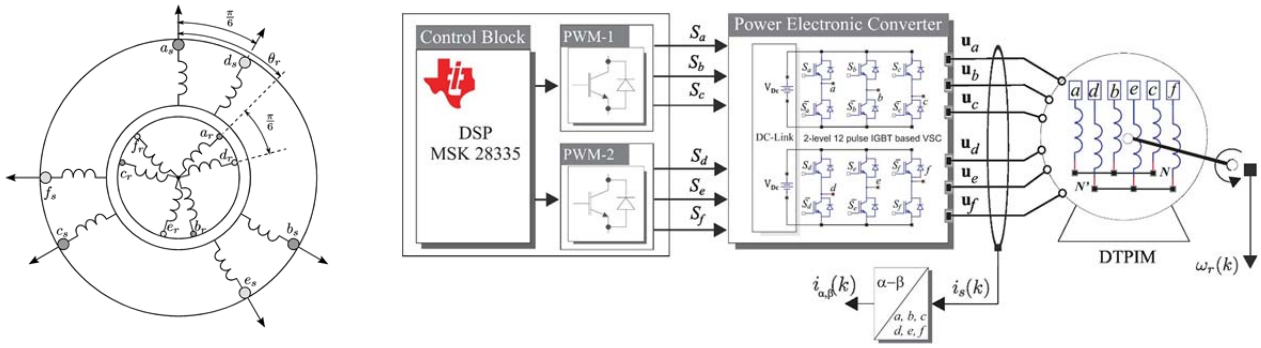


(a) Cross section of an asymmetrical DTPIM.

(b) General scheme of an asymmetrical DTPIM drive.

Fig. 1. Winding configuration and feed topology of an asymmetrical dual three-phase induction machine.

not allow real-time simulations, which are required to test the controller in the HIL configuration. Using a field-programmable gate array (FPGA) evaluation board for this purpose is advantageous because most of the required I/O interfaces for the HIL configuration can be integrated directly and are controlled by the FPGA. Furthermore, real-time requirements can be easily fulfilled by exploiting the parallelism capabilities of the FPGA while development cost can be greatly decreased by programming the FPGA in high-level development languages, as well as by using resources such as intellectual property (IP) blocks. Finally, FPGAs facilitate the extension of the implementation for future releases of the simulator. Given all these reasons, FPGAs are regarded as adequate candidates for implementing the real-time part of the simulator, whereas relaying in a standard PC is suitable for storage and non-real-time operations. In this study, we select a Xilinx SP605 evaluation board, which includes a Spartan-6 FPGA, to facilitate the implementation of I/O interfaces.

Real-time simulation results are validated experimentally using a 15 kW DTPIM test bench. Therefore, this work constitutes a starting point for testing different types of controllers applied to the DTPIM in an HIL configuration. The remainder of this paper is organized as follows. Section II introduces the mathematical model of the DTPIM on the basis of the vector space decomposition (VSD) approach. Section III presents the details of the hardware and software implementation of the real-time simulator. Section IV provides the details and characteristics of the experimental test bench. In addition, this section includes a comparison of the results obtained by the real-time simulator and those obtained through a MATLAB/Simulink model and via experimental tests that quantify the statistical performance parameters. Finally, Section V summarizes the concluding remarks.

II. THE DPTIM MATHEMATICAL MODEL

Multiphase machines are well recognized as an attractive alternative to conventional three-phase machines in several industrial applications (more-electric aircraft, electric and hybrid vehicles, ship propulsion, and wind power systems), which require high overall system reliability and reduction in total power (current) per phase [15]–[17]. One of the most widely discussed topologies is the asymmetrical DTPIM with two sets of three-phase stator windings that are spatially shifted by 30 electrical degrees and isolated neutral points (Fig. 1(a)). The DTPIM is a continuous system, which can be described by a set of differential equations. The model of the system can be simplified by using VSD theory [18]. This theory enables the transformation of the original six-dimensional space of a machine model into three two-dimensional orthogonal subspaces in stationary reference frames (α–β), (x–y), and (z_1–z_2) by means of a 6×6 transformation matrix and using an amplitude invariant criterion. This matrix, **T**, is defined as

$$\mathbf{T}=\frac{1}{3}\begin{bmatrix} 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix}. \quad (1)$$

According to the VSD approach, electromechanical energy conversion variables are mapped in the (α–β) subspace while the current components in the (x–y) subspace represent the supply harmonics of order $6n\pm1$ (n = 1, 3, 5, …) and only generate losses. The voltage vectors in the (z_1–z_2) subspace are zero because of the isolated neutral point configuration [19]. Moreover, the DTPIM is supplied with a two-level 12-pulse insulated-gate bipolar transistor (IGBT)-based voltage-source converter (VSC) and a Dc-link (VDc), as shown in Fig. 1(b). The VSC exhibits a discrete nature with 2^6=64 different switching state vectors defined by six switching functions, which correspond to six inverter legs [S_a,

S_d, S_b, S_e, S_c, S_f], where $S_{a-f} \in \{0,1\}$. The different switching state vectors and VDc voltage define the phase voltages, which can in turn be mapped to the (α–β)–(x–y) space according to the VSD approach [20], [21]. To represent the stationary reference frame (α–β) in a rotating reference frame (d–q), a rotation transformation can be used. This transformation matrix, $\mathbf{T}_{dq}$, is represented as

$$\mathbf{T}_{dq} = \begin{bmatrix} \cos(\theta_r) & \sin(\theta_r) \\ -\sin(\theta_r) & \cos(\theta_r) \end{bmatrix} \tag{2}$$

where θ_r is the rotor angular position referred to the stator, as shown in Fig. 1(a).

The dynamic behavior of the DTPIM can be modeled using a state-space representation as follows [22]:

$$\frac{d[\mathbf{x}]_{4\times1}}{dt} = [\mathbf{A}]_{4\times4}[\mathbf{x}]_{4\times1} + [\mathbf{B}]_{4\times4}[\mathbf{u}]_{4\times1} \tag{3}$$

where $[\mathbf{u}]_{4\times1}=[u_{\alpha s}, u_{\beta s}, 0, 0]^T$ is the input vector, $[\mathbf{x}]_{4\times1}=[i_{\alpha s}, i_{\beta s}, i_{\alpha r}, i_{\beta r}]^T$ is the state vector, and $[\mathbf{A}]_{4\times4}$ and $[\mathbf{B}]_{4\times4}$ are the parameter matrices that characterize the dynamics of the electrical drive. The set of state variables described above is defined as

$$[\mathbf{A}]_{4\times4} = \begin{bmatrix} -c_2R_s & c_3\omega_rL_m & c_3R_r & c_3\omega_rL_r \\ -c_3\omega_rL_m & -c_2R_s & -c_3\omega_rL_r & c_3R_r \\ c_3R_s & c_4\omega_rL_m & -c_4R_r & -c_4\omega_rL_r \\ c_4\omega_rL_m & c_3R_s & c_4\omega_rL_r & -c_4R_r \end{bmatrix} \tag{4}$$

$$[\mathbf{B}]_{4\times4} = \begin{bmatrix} c_2 & 0 & -c_3 & 0 \\ 0 & c_2 & 0 & -c_3 \\ -c_3 & 0 & c_4 & 0 \\ 0 & -c_3 & 0 & c_4 \end{bmatrix} \tag{5}$$

where R_s and R_r are the stator and rotor resistance, respectively; ω_r is the rotor angular speed; and L_s, L_r, and L_m are the stator, rotor, and magnetizing inductances, respectively. Furthermore, the constants c_i (i=1,2,3,4) are defined as:

$$c_1 = L_sL_r - L_m^2, \quad c_2 = \frac{L_r}{c_1}, \quad c_3 = \frac{L_m}{c_1}, \quad c_4 = \frac{L_s}{c_1}. \tag{6}$$

The proposed mathematical model can be discretized using the Euler method. Thus, the prediction of the state vector for the sample ($k+1$) calculated at sample time (k), namely, $\hat{\mathbf{x}}_{(k+1|k)}$, can be expressed as

$$\hat{\mathbf{x}}_{(k+1|k)} = [\mathbf{I} + T_m\mathbf{A}_{(k|k)}]\mathbf{x}_{(k|k)} + T_m\mathbf{B}\mathbf{u}_{(k|k)} \tag{7}$$

where T_m is considered the sampling time and $\mathbf{I}$ is the identity matrix. Moreover, for a machine with P pairs of poles, the electromagnetic torque (T_e) of the drive can be modeled by the following equation:

$$T_e = 3\frac{P}{2}\left(\psi_{\beta r}i_{\alpha r} - \psi_{\alpha r}i_{\beta r}\right) \tag{8}$$

where $\psi_{\alpha r}$ and $\psi_{\beta r}$ are the rotor fluxes in the (α–β) subspace.

The relationship between torque and rotor speed can be written as

$$J_i\frac{d}{dt}\omega_r + B_i\omega_r = \frac{P}{2}\left(T_e - T_L\right) \tag{9}$$

where T_L is the load torque, J_i is the machine inertia, and B_i is the viscous friction coefficient. Equs. (8) and (9) can be represented in discrete time with a procedure analogous to the one used for Equ. (7). Therefore, electromagnetic torque and speed evolutions can be represented as a function of the state variables by the following equations:

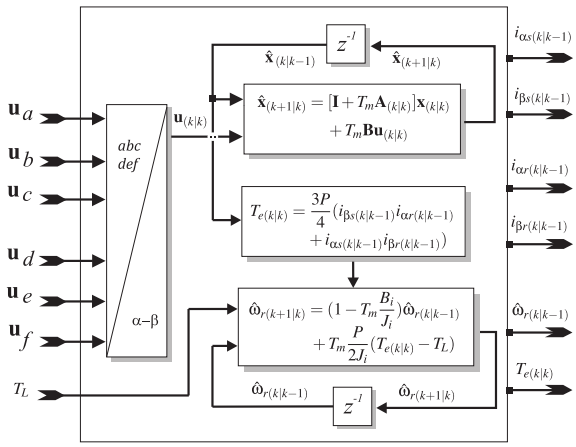
$$T_{e(k|k)} = \frac{3P}{4}\left(i_{\beta s(k|k-1)}i_{\alpha r(k|k-1)} + i_{\alpha s(k|k-1)}i_{\beta r(k|k-1)}\right) \tag{10}$$

$$\hat{\omega}_{r(k+1|k)} = \left(1 - T_m\frac{B_i}{J_i}\right)\hat{\omega}_{r(k|k-1)} + T_m\frac{P}{2J_i}\left(T_{e(k|k)} - T_L\right). \tag{11}$$

The functional block diagram of the discretized DTPIM model is shown in Fig. 2(a). Equs. (7), (10), and (11) are implemented by using basic arithmetic blocks, such as adders, multipliers, and registers, which are used to obtain the necessary time delays. The input variables are the voltages applied to the stator windings ($\mathbf{u}_a$, $\mathbf{u}_b$, $\mathbf{u}_c$, $\mathbf{u}_d$, $\mathbf{u}_e$, $\mathbf{u}_f$) and load torque. The output of the functional block diagram could be any of the following parameters obtained through a mathematical manipulation of inputs and/or state variables, which is the most common approach for control applications: electromagnetic torque, rotor angular speed, stator, and rotor currents in a stationary reference frame. The real-time simulator is developed and implemented using the Xilinx SP605 development board, which is shown in Fig. 2(b). This board features a Spartan-6 XC6SLX45T FPGA.

III. Real-Time Simulator Implementation

A simplified scheme of the real-time simulator is shown in Fig. 3, in which the data flow among blocks is represented by arrows. The digital system implements a custom-made processor featuring Harvard architecture with separate data and program memories, program counter, processing unit, input and output modules, and a clocking module. As shown in Fig. 3, the core of the implementation is the control unit. The control unit interconnects, manages, and coordinates the rest of the blocks by reading, decoding, and executing program instructions. Program instructions are stored in program memory and indexed by the program counter. The input module captures pulse-width modulation (PWM) signals through the digital pins of the evaluation board and converts them into floating-point values, which can be operated by the processing unit. The processing unit is capable of performing sums and products and is used to implement Equs. (7), (10), and (11). The operands employed by the processing unit are read from the data memory, which enables their simultaneous reading in a single clock cycle. Data memory can also store the results provided by the



(a) DTPIM input and output signals.

(b) SP605 Xilinx evaluation board.

Fig. 2. Implementation characteristics of the real-time simulator.

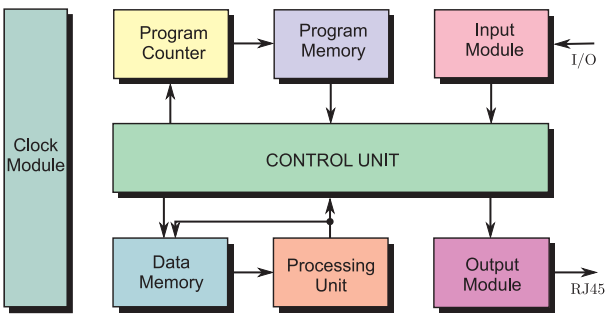


Fig. 3. Block diagram of the real-time simulator architecture.

processing unit. The output module provides the PC with the values of the state vector, as well as the input voltages for each clock cycle. Finally, the clock module aims to generate all the clock signals required by the different blocks of the real-time simulator.

The details of each block are as follows:

- The **Data Memory** capacity is 512 32-bit wide words, whereas the **Program Memory** can store 512 36-bit wide words; both memories are implemented using random access memory (RAM) blocks embedded in the FPGA. This approach eases the scaling of the memory for future implementation releases. As data and program instructions are stored in different memories (Harvard architecture), the program instructions and associated data are read in a single clock cycle.
- The **Program Counter** is implemented as a nine-bit synchronous up-counter capable of addressing 512 **Program Memory** positions. It features a load function, which allows it to perform branch operations.
- The **Processing Unit** is used for data manipulation and addition and multiplication operations. Floating-point arithmetic is employed to increase the dynamic range of the operations performed by the processing unit and to facilitate the comparison of the results with those obtained by means of simulation in the MATLAB/Simulink environment. An efficient implementation is assured by using the LogiCORE IP Floating-Point Operator from Xilinx [23].
- The **Input Module** allows for the conversion of binary signals representing PWM voltages generated by the Dc-link to floating-point values for data manipulation.
- The **Output Module** implements a Gigabit–Ethernet communication link, which is used to send the values of the state vector $\hat{\mathbf{x}}_{(k|k-1)}$ and input voltages ($\mathbf{u}_a$, …, $\mathbf{u}_f$) for external storage; this block is based on the LogiCORE IP Tri-Mode Ethernet MAC provided by Xilinx [24]. A Gigabit–Ethernet link is used considering that it achieves high data rates and is more widely available than other technologies, such as the Peripheral Component Interconnect Express and the Serial Advanced Technology Attachment.
- Finally, the **Clock Module** generates the main and **Output Module** clocking signals, whose periods are 20 and 8 ns, respectively; this module is implemented by using the LogiCORE IP Clocking Wizard [25].

ALGORITHM I
IMPLEMENTATION OF THE MATHEMATICAL MODEL

Initialize constants
loop
  Store values of voltage inputs
  Compute values of system inputs $u_{(k|k)}$ at instant k
  Compute torque at instant k, $T_{e(k|k)}$, by using Eq. (10)
  Compute the prediction of the state variables for the instant $k + 1$ by using Equs. (7) and (11)
  Update state variables for the next iteration
  Wait for the next sampling instant
end loop

The developed program code implements Algorithm 1. This algorithm can be implemented by means of addition, multiplication, and branch instructions, as well as some instructions for storing and reading data from memories, transferring data to buffers of the output module, and acquiring data present in the digital input pins.

From a software point of view, the Xilinx ISE Design Suite

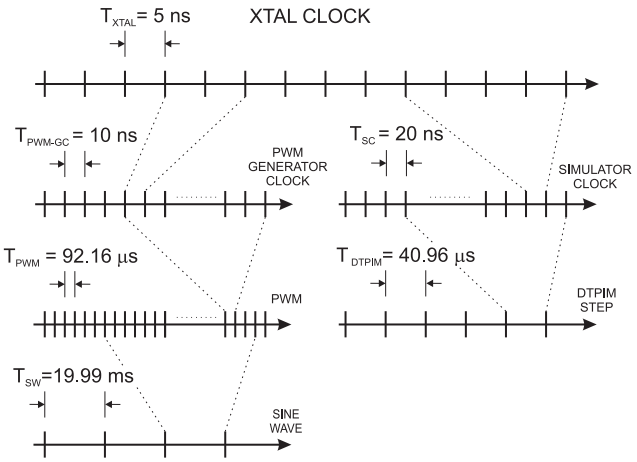


Fig. 4. Real-time simulator timing resolution.

environment is used during the design, test, and implementation phases. The integrated development environment (IDE) ISE constitutes the main development tool, whereas the ISE simulator (ISim) is for testing and debugging purposes. In addition, all functional blocks are developed by combining pieces of very high-speed integrated circuit hardware description language (VHDL) code and Xilinx IP blocks.

The real-time simulator architecture consists of multiple processes running at different rates. Fig. 4 represents the relationship among the different rates used. The evaluation board provides a main differential clock of 200 MHz, which feeds a phase-locked loop (PLL) to derive the clock signals of 100 and 50 MHz for the PWM generator and real-time simulator, respectively. In the PWM generator, a 50 Hz sine wave varies the duty cycle of a 10.8 kHz PWM carrier to obtain the VSC voltage for the simulation. Similarly, the hardware simulation of the DTPIM model is executed with a simulation step of 40.96 µs (24.4 kHz). Despite the fact that the simulation can run at frequencies as high as 100 kHz, the simulation step is selected to match the sampling rate of the measurement instruments.

IV. Experimental Results

A. Experimental Setup Overview

A commercial three-phase induction machine with three pairs of poles, 72 slots, and 15 kW-rated power is rewound to obtain an asymmetrical dual three-phase winding (with two isolated neutral points) with the same pairs of poles and rated power as the original three-phase machine. Conventional blocked rotor and no-load test procedures are applied to determine experimentally the electrical and mechanical parameters of the DTPIM. The obtained values are presented in Table I. Two three-phase Semikron SKS 35F B6U+E1CIF+B6CI21V VSC modules are used to generate six-phase stator voltages. The VSC modules are fed in parallel by a three-phase grid of 380 VRMS, and the internal

TABLE I
Electrical and Mechanical Parameters

Parameter	Dual Three-phase Induction Machine		
	Symbol	Value	Unit
Stator resistance	R_s	0.62	Ω
Rotor resistance	R_r	0.63	Ω
Stator inductance	L_s	0.2062	H
Rotor inductance	L_r	0.2033	H
Magnetizing inductance	L_m	0.0666	H
System inertia	J_i	0.27	kg·m^2
Viscous friction coefficient	B_i	0.012	kg·m^2/s
Nominal frequency	f_a	50	Hz
Load torque	T_L	0	N·m
Pair of poles	P	3	–
	Rated Values		
Rated rotor speed	ω_n	970	rpm
Rated current[1]	i_n	2.50	A
Full load torque	T_n	146.11	N·m

[1]Current per phase

rectifiers generate a DC voltage of 585 V. A hardware timer based on the LM555 device operating in monostable mode is implemented to control the internal pre-charge circuit of the SKS 35F converter modules.

The implementation of the control system is based on the digital signal processor (DSP) TMS320LF28335 manufactured by Texas Instruments and the Technosoft MSK28335 board, which comprises 12 PWM outputs. PWM outputs are configured to achieve a 10 kHz carrier frequency. Stator currents are measured using Hall effect sensors (LA55P from LEM). The analog-to-digital converters of the Technosoft board, which comprises 16 parallel channels, are used to capture the measured signals. On the other hand, the mechanical speed is measured by employing a Hengstler RI 58-O digital incremental encoder with a resolution of 10,000 pulses per revolution and the eQEP peripheral of the DSP. The digital inputs and outputs of the control board are galvanically isolated with the ISO7230CDW isolator manufactured by Texas Instruments to preserve system integrity. Fig. 5 shows the scheme of the experimental setup used to validate the real-time hardware simulator of the DTPIM. To quantify the performance of the real-time simulator, a PLL software implementation is employed in the estimation of the stator current angle (θ_r). The block diagram of the proposed PLL scheme is shown in Fig. 6.

The output of the PLL scheme provides the current angle value that is employed to calculate the stator current in a rotating reference frame (i_d –i_q) using the transformation matrix shown in Equ. (2). The statistical performance parameters (with stator current evolution in a rotating

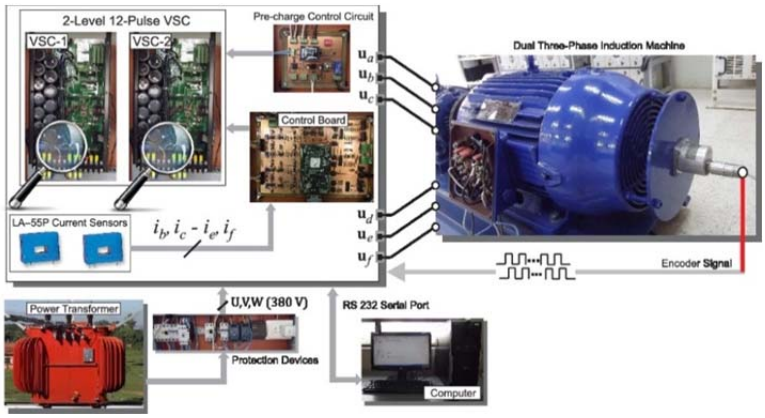


Fig. 5. Start-up characteristics of stator current.

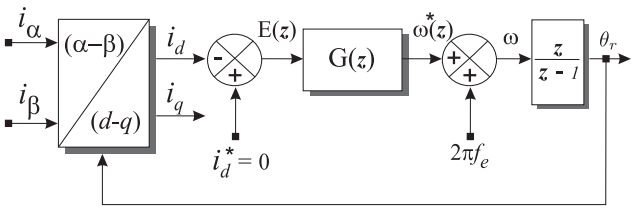


Fig. 6. Block diagram of a PLL with specialdesign of the compensator.

reference frame as a reference) across three different cases are evaluated and compared. The cases involve a real-time hardware simulator based on the FPGA device, DTPIM model based on a MATLAB/Simulink simulation environment, and a real DTPIM.

B. PLL Software Implementation

Fig. 6 shows that the dynamic performance of the proposed PLL is highly influenced by the compensator G(z). Considering that the reference signal is the stator current in d axis and given that the loop gain includes an integral term, θ_r

must track the constant component of the reference signal with zero steady-state error. However, to ensure zero steady-state error, the loop gain must include at least two integrators. Therefore, G(z) must include at least one integral term, that is, one pole at z = 1. The other poles and zeros of G(z) are determined mainly by the closed-loop bandwidth requirements of the PLL and stability indices, such as phase margin and gain margin, according to the procedure described in [26]. Considering that G(z) is controllable, the transfer function can be expressed in the following controllable canonical form:

$$\mathbf{x}_{(k+1|k)} = [\mathbf{F}]_{5\times5}[\mathbf{x}_{(k|k)}]_{5\times1} + [\mathbf{D}]_{5\times1}e_{(k|k)} \tag{12}$$

$$\omega^*_{(k+1|k)} = [\mathbf{C}]_{1\times5}[\mathbf{x}_{(k|k)}]_{5\times1} \tag{13}$$

where the matrix $[\mathbf{F}]_{5\times5}$ and the vectors $[\mathbf{D}]_{5\times1}$ and $[\mathbf{C}]_{1\times5}$ define the dynamics of the PLL compensator [G(z)], whose set of state variables (Fig. 7) is as follows:

$$[\mathbf{F}]_{5\times5} = \begin{bmatrix} 2.5 & -2.2 & 0.9 & -0.2 & 0.01 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{14}$$

$$[\mathbf{D}]_{5\times1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{15}$$

$$[\mathbf{C}]_{1\times5} = \begin{bmatrix} 1.7 & -5.7 & 8.1 & -5.8 & 1.6 \end{bmatrix}. \tag{16}$$

This state-space realization is in controllable canonical form because the resulting model is guaranteed to be controllable. As the control enters a chain of integrators, it can move every state (Fig. 7).

The proposed PLL architecture is implemented by using the TMS320LF28335 DSP with consideration of floating-point arithmetic and 10 kHz sampling frequency. The PLL algorithm is executed as an interrupt service routine (ISR), which is triggered by one of the general-purpose timer circuits available on the chip. The same timer also triggers the simultaneous acquisition of input signals with sampling interrupt. As the on-chip A/D converters achieve a rapid conversion rate (approximately 106 ns of conversion time), input data are made available at the beginning of the ISR with negligible time delay. Immediately after the A/D conversion, the current components in the stationary reference frame (α–β) are calculated at each sampling time from the measured phase stator currents (i_{bs},i_{cs},i_{ds},i_{fs}) by using Equ. (1).

Fig. 8 shows the stator current angle evolution obtained experimentally by using the proposed PLL architecture when the DTPIM is fed with electrical frequency voltages (f_e) of 40 Hz. In the figure, the angle evolves from 0 to 2π during a single period of the stator current wave. The result is also observed to be satisfactory even when the stator currents in the stationary reference frame are distorted because of electrical noise.

C. DTPIM Real-Time Simulator Performance

The performance of the real-time simulator is analyzed and

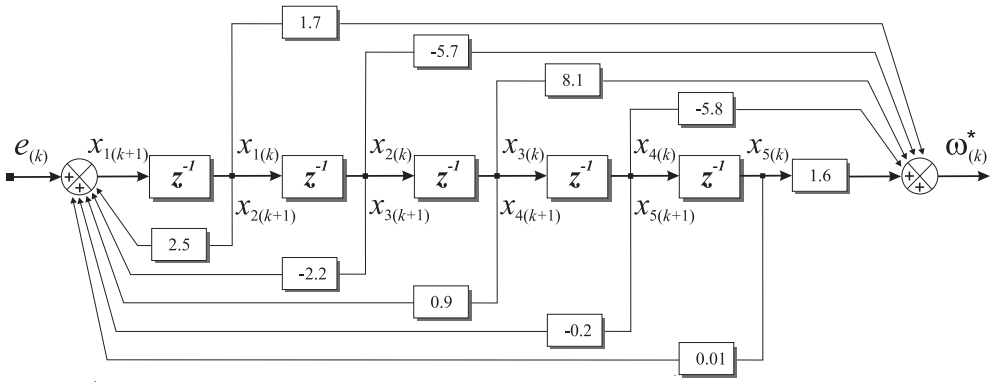


Fig. 7. Block diagram representation of G(z) transfer function on controllable canonical form.

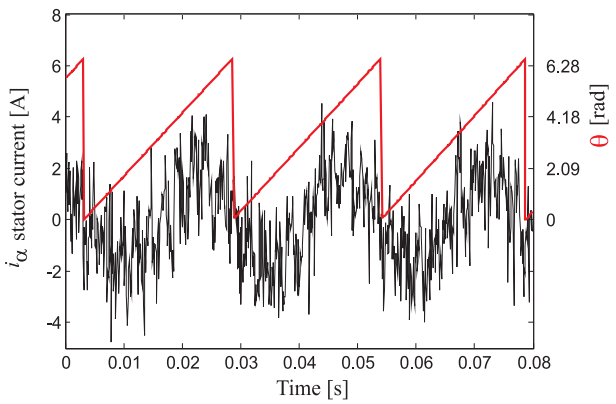


Fig. 8. Stator current angle evolution obtained experimentally by using the proposed PLL with a specially designed compensator.

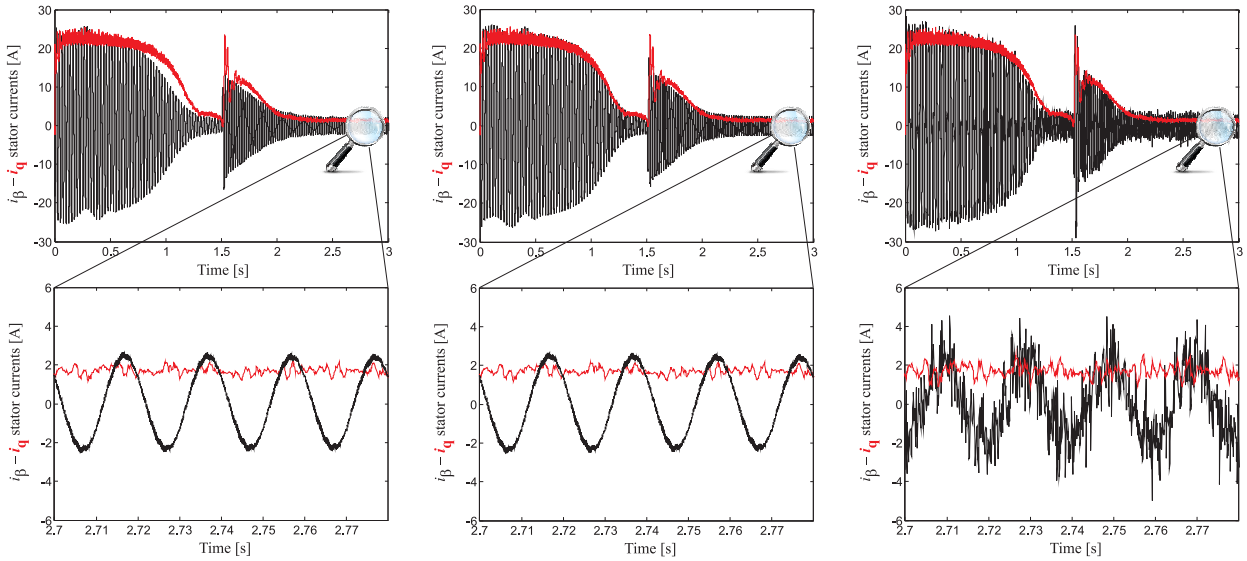
validated using the experimental setup and a DTPIM MATLAB/Simulink model, in which a fourth-order Runge–Kutta numerical integration method is applied to compute the evolution of the state variables step by step in the time domain. Table I shows the electrical and mechanical parameters of the asymmetrical DTPIM, which are considered during the implementation of the real-time simulator. The accuracy of the real-time simulator is evaluated under no-load conditions.

Fig. 9 shows the start-up characteristics of the stator current when a VSC supplied with 585 V of Dc-Link is considered and when a sinusoidal modulation index of 0.275 and a frequency of 50 Hz are applied. Fig. 9(a) shows the i_β current evolution of the DTPIM provided by the proposed real-time hardware simulator based on the FPGA. In this case, the VSC, PWM scheme, and AC motor are simulated within the FPGA.

After the real-time simulation, the state variables are sent to the computer through a Gigabit–Ethernet link for analysis. The stator current evolution is compared with the i_d current obtained using the experimental setup to verify the agreement between the real-time simulation results and experimental results, especially with respect to the time constants associated with the DTPIM (start-up speed, steady-state current, etc.). The time constants converge to the values obtained experimentally under transient and steady-state conditions, in which quantifying a steady-state current of approximately 2 A is possible. Fig. 9(b) shows the results obtained using the MATLAB/Simulink model, and Fig. 9(c) shows the results obtained experimentally. These results are compared with the i_d current obtained experimentally. The start-up current evolution converges to a common value for the FPGA-based or MATLAB/Simulink-based simulations, as well as for the experimental setup, with a start-up transient of approximately 1.15 s. After 1.5 s, the reference frequency is changed from 40 Hz to 50 Hz while the modulation index is kept constant at 0.275. Fig. 10 shows the rotor speed evolution for the three cases previously analyzed. The results provided by the FPGA-based simulator and MATLAB/Simulink model under steady-state conditions converge to the values obtained experimentally using a motor with three pairs of poles and 50 Hz of nominal frequency (1,000 rpm).

Fig. 11 shows the power spectral density of the $i_{\beta s}$ stator current measured experimentally and depicted in Fig. 9(c). The switch mode operation effect of the converter caused by the PWM modulation technique is noticeable. Specifically, clusters of high-order harmonics appear in the frequency spectra of the converter currents at multiples of the switching frequency. Regardless of the control method employed, the harmonics generated by the fast-switching PWM converter introduce a significant amount of distortion in the range beginning at the switching frequency [27].

Statistical performance parameters, such as covariance, standard deviation (SD), and mean squared error (MSE), are used to evaluate the accuracy of the results provided by the real-time simulator, taking as reference the results obtained through simulations and by means of experimental tests. The envelope of the fundamental frequency component of the stator currents in the stationary reference frame can be calculated using the Hilbert transform (HT) method. This envelope detection method involves creating analytic signals of the stator current using the HT method. An analytic signal is a complex signal, whose real part ($i_{\alpha s}$) is considered the original signal and the imaginary part ($ji_{\beta s}$) is the HT of the



(a) Stator current ($i_{\beta s}$) obtained using a real-time simulation environment.

(b) Stator current ($i_{\beta s}$) obtained using MATLAB/Simulink simulation environment.

(c) Stator current ($i_{\beta s}$) obtained by experimental tests.

Fig. 9. Start-up characteristics of stator current.

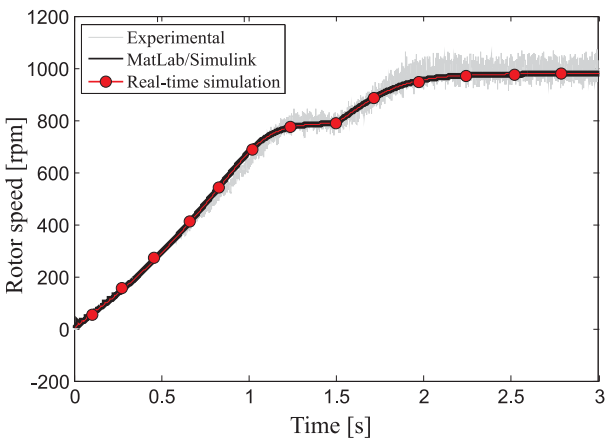


Fig. 10. Transient rotor speed evolution.

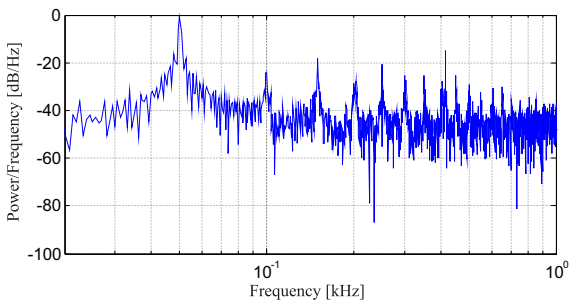


Fig. 11. Power spectral density of the $i_{\beta s}$ stator current.

original signal. A discrete-time analytic signal ($\hbar(k)$) can be defined as follows:

$$\hbar(k) = i_{\alpha s}(k) + j i_{\beta s}(k) . \quad (17)$$

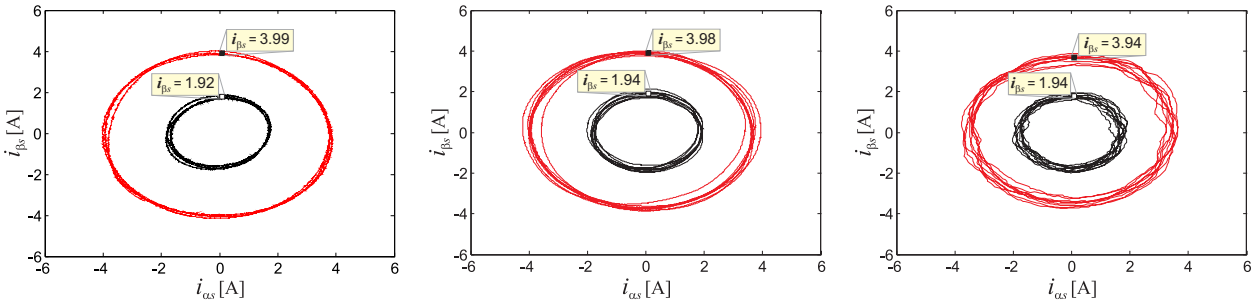
The envelope of the signal can be determined by computing the modulus of the analytic signal from the following equation:

$$\left|\hbar(k)\right| = \sqrt{\left[\sum_{k=0}^{n} i_{\alpha s}(k)\right]^2 + \left[\sum_{k=0}^{n} i_{\beta s}(k)\right]^2} . \quad (18)$$

The above equation can be used to determine the envelope evolution of the stator current, which is used to evaluate the aforementioned statistical performance parameters. With this analysis, we can determine the degree of dispersion of the stator current envelope with respect to the value obtained experimentally through the PLL software implementation (shown in red color in Fig. 9).

The statistical relationship between the curves (i_{qs} and stator current envelope) and the MSE are analyzed under steady-state conditions. Table II details the results of the three different DTPIM implementation methods considered in Fig. 9. Note that the obtained covariance results are positive. These results show a linear dependence between the i_{qs} current obtained through the PLL implementation and the stator current envelope obtained by means of the HT method. The results tend to show similar behaviors across the three cases. Moreover, the low SD values shown in Table II indicate that the data points in steady-state conditions tend to be very close to the mean values of the i_{qs} current. The MSE values are used for comparative purposes. Note that the obtained MSE results are similar and close to 1 A for the three cases. These results show the good behavior of the real-time hardware simulator.

Further analysis is conducted to examine the performance of the real-time simulator under different test conditions. For example, a change in the modulation index from 0.275 to 0.481 is considered at t = 1.5 seconds, along with a constant voltage frequency of 40 Hz. Fig. 12(a) shows the trajectory of



(a) $i_{\alpha s}$vs.$i_{\beta s}$ current obtained using a real-time simulation environment.

(b) $i_{\alpha s}$vs.$i_{\beta s}$ current obtained using a MATLAB/Simulink simulation environment.

(c) $i_{\alpha s}$vs.$i_{\beta s}$ current obtained by experimental tests.

Fig. 12. Real-time simulator $i_{\alpha s}$vs.$i_{\beta s}$ characteristics.

TABLE II
PERFORMANCE ANALYSIS

Parameter	Statistical Performance Parameters		
	Covariance	SD	MSE
Real-time simulation	1.95×10^{-26}	1.087	1.132
MATLAB/Simulink	1.60×10^{-26}	1.025	1.064
Experimental	5.23×10^{-26}	1.004	1.030

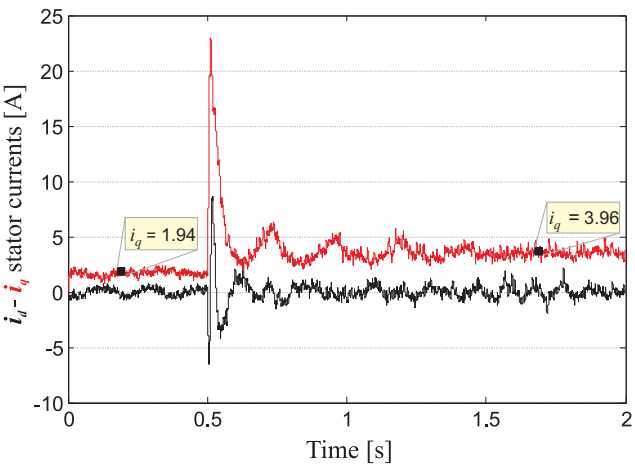


Fig. 13. Stator current evolution in a rotating reference frame.

current evolutions in two planes (α–β) considering at least four current periods in a steady-state operation, in which the effect of the change in the modulation index in the reference voltages can be observed. Fig. 12(b) shows the results obtained using the MATLAB/Simulink model, and Fig. 12(c) shows the experimental results. As in the previous case, the simulated current converges to the values equivalent to those obtained experimentally and exhibits a similar dynamic behavior. These results prove the good behavior of the real-time simulator.

Finally, Fig. 13 shows the stator current evolution in the rotating reference frame (d–q) obtained with Eq. (2) using the angle values calculated by the PLL software implementation. The steady-state current values converge to the values shown in Fig. 12 before and after the change applied in the modulation index from 0.275 to 0.481, with the values being close to 2 and 4 A, respectively. These results show the good behavior of the proposed real-time simulator applied to the DTPIM.

V. CONCLUSION

Multiphase induction motor drives have emerged in recent years for different applications, especially those that require high power and reliability. These applications are still evolving and thus require a constant evaluation of the new constraints associated with power electronics, magnetic saturation, and control systems. Major studies will require the use of flexible and scalable real-time simulators.

This paper introduced a DTPIM real-time simulator implemented by using an FPGA-based development board. First, the mathematical model of the multiphase machine was introduced. Second, the details of the implementation (hardware and software) were presented. To validate the results obtained by the FPGA-based simulator, an experimental test bench was designed. In addition, the obtained results were compared with those provided by a MATLAB/Simulink model under no-load conditions. An error close to zero was obtained for the results generated by the FPGA-based simulator and MATLAB/Simulink model. These results were consistent with the experimental results, thereby validating the behavior of the implemented real-time simulator in terms of accuracy. The obtained results constitute the starting point for the development of test systems, which involve multiphase (more than three phases) electrical motors in HIL configurations and thus entail minimal costs, human resources, power consumption, and physical space.

ACKNOWLEDGMENT

The authors would like to thank the Paraguayan Government for the economic support they provided through the CONACYT grant 14-INV-097 (research Project) and the research stay grants under the program “Programa de Vinculación de Científicos y Tecnólogos,” PROCIENCIA, with references 14-VIN-008 (2014 call) and PVCT 15-13

(2015 call). In addition, they wish to express their gratitude to the anonymous reviewers for their helpful comments and suggestions. This work was also funded by MINECO of Spain; the FEDER funds of the E.U. under Grants 2012/287, TEC2013-47141-C4-1-R, and FPU12/0439; and by the Fundación Carolina of Spain.

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