Development of a Novel 30 kV Solid-state Switch for Damped Oscillating Voltage Testing System

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Abstract

This paper describes the design and development of a novel semiconductor-based solid-state switch for damped oscillating voltage test system. The proposed switch is configured as two identical series-connected switch stacks, each of which comprising 10 series-connected IGBT function units. Each unit consists of one IGBT, a gate driver, and an auxiliary voltage sharing circuit. A single switch stack can block 20 kV-rated high voltage, and two stacks in series are proven applicable to 30 kV-rated high voltage. The turn-on speed of the switch is approximately 250 ns. A flyback topology-based power supply system with a front-end power factor correction is built for the drive circuit by loosely inductively coupling each unit with a ferrite core to the primary side of a power generator to obtain the advantages of galvanic isolation and compact size. After the simulation, measurement, and estimation of the parasitic effect on the gate driver, a prototype is assembled and tested under different operating regimes. Experimental results are presented to demonstrate the performance of the developed prototype.

I. INTRODUCTION

Partial discharge testing is one of the most effective ways to assess the on-site insulation of power cables [1]. The common methods include the DC voltage test, AC voltage test, very low frequency test, and damped oscillating voltage (DOV) test. The conditions of the DC voltage test are completely different from the normal cable operation environment, and the test process causes damage to specimens; hence, this method is not recommended for the partial discharge testing of power cables. The very low frequency test stresses cables using low frequency (0.1 Hz) voltage, which provides different stress distributions from the AC voltage and tends to be destructive. Although the AC voltage test is considered the best method, the test AC transformer is bulky and heavy because the length of the tested cable can extend to several kilometers and thus result in a large equivalent capacitance. In the last 20 years, the DOV test system (DOVTS) has been evaluated extensively because of its many advantages, including its small size, light weight, and the similarity of the excitation of partial discharge to power frequency [2]-[4]. The feasibility and practicality of the DOVTS been confirmed. Its most essential component is the high voltage switch (HVS), which should have a compact and flexible design to satisfy on-site testing requirements. Considering the unique working principle of the DOVTS, the HVS should have its own specification and utilization.

Different types of HVS are described in the literature; however, few are considered to be applicable to the DOVTS because of various reasons, i.e., insufficient power rate or switch speed, unstable switching behavior, and large size. A discharge spark gap is used in [5] for its adequate power capability, although its drawbacks are obvious, e.g., short lifespan, uncontrolled switch, and low speed. In view of the progress in the semiconductor industry, the work in [1] recommends a solid-state switch based on thyristors [6], [7], MOSFETs, or IGBTs [8]-[10]. In the last two decades, different types of solid-state switches have been proposed for different applications, such as pulsed power [11], nuclear fusion [12], static synchronous compensator [13], and traction applications [14]. Few of these solid-state switches have

adequate voltage rates that match the requirements of the DOVTS. Moreover, all the above switches are large in size and heavy in weight.

In addition to voltage balancing issues for IGBT series connection applications [15], [16], the development of compact semiconductor switches should focus on new issues, i.e., power supply systems with adequately rated isolation levels, smart size, and parasitic effect caused by the compact structure of these switches. The issues are partially mentioned in [17]-[19], but their solutions or analyses are not feasible with respect to our application.

In the present work, we introduce a novel semiconductor HVS prototype for the DOVTS using series-connected IGBTs. Following a modular design concept, we design the switch to consist of two identical switch stacks based on IGBT switch units, a power supply system, and a synchronous trigger unit. The working principle of this specialized HVS and the detailed configuration of the supply scheme are described. After analyzing the parasitic effects, the switch stack is considered as a comprehensively integrated circuit pan. Finally, we assemble the different parts of the HVS and test its behavior under a 30 kV-rated voltage level. The highlights of the HVS are as follows. The proposed switch uses a loosely inductively coupled power supply scheme that generates sufficient energy and satisfies HV isolation requirements. With the application of the modular concept, the developed switch is small in size and light in weight and is thus easy to transport for on-site testing. The switch could be further developed through a simple series connection to achieve a high-rated blocking voltage.

II.   System Configuration

A. Working Principle of DOVTS and Overall Schematic of the Proposed HVS

The HVS performs the most important function in the testing system. As shown in Fig. 1, the standard DOVTS consists of a high voltage DC (HVDC) source, an HVS, resonant components (air-core inductor and specimen), and a detector. Given the start signal, the specimen, such as a piece of underlaid XLPE cable, is charged by the HVDC source to a preset level, during which the HVS remains turned off. Then, the switch is turned on, and the HVDC source is removed. The specimen is subsequently discharged through a series-connected inductor, thus generating DOV as a result of the series resonance. The generation of the resonant voltage continues up to tens of milliseconds before its damping to zero, after which the switch is turned off and the HVDC source recharges the specimen.

In accordance with the aforementioned working principle of the DOVTS, the design of the proposed HVS should have the following particular considerations:
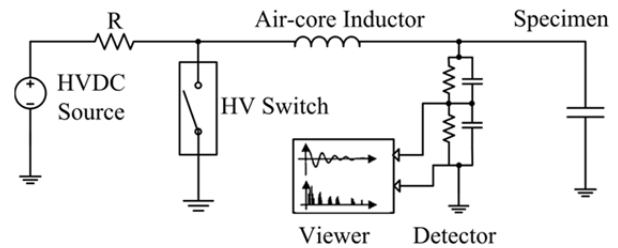

Fig. 1. Standard assembly of the DOVTS.

III. adequate voltage blocking rate and current pass through ability (30 kV and 40 A, respectively);

IV. rapid switching speed to minimize attenuation during the oscillating process (less than 1 μs);

V. compact size and weight for easy transport (less than 10 kg); the switch is under zero current switch mode when powered "on" and is turned "off" when the switch lacks load, which indicates that the severe tail current effect described in [20] can be ignored.

Fig. 2 shows the structure of the proposed HVS and its connection to the DOVTS. The proposed HVS consists of several main assemblies. In 20 kV applications, the switch includes a switch stack, an HV isolation power supply system, and a trigger unit. Two identical series-connected switch stacks are used in 30 kV applications.

Each stack is composed of several series-connected IGBTs and their auxiliary circuits. Owing to voltage balancing methods described in the literature [21]-[25] (i.e., paralleled static voltage sharing resistors and a series of dynamic transient voltage sharing suppressors), each IGBT is rated only for an identical fraction of the full blocking voltage. The proposed power supply system is arranged as a combination of a flyback converter and a front-end power factor corrector to produce sufficient energy with only one or two turns of the coil. The parameter of the power supply system is properly designed with consideration of reliability and simplicity requirements. The ferrite core inductively couples the primary power supply coil and secondary power dissipation coil, which serve as multiple outputs of the HV isolation between each IGBT function unit and voltage adaptation. The trigger unit controls the IGBT units (SUs) through the opto-transmitters. A "start" signal to the trigger unit activates several channels of a light signal synchronously. The opto-receiver on each unit then receives a turn-on signal and activates the controlled IGBT. At the same time, a channel "cut-off" of the light signal is sent to the HVDC source. After a preset duration (several hundreds of milliseconds, depending on the pre-recorded duration of the DOV), the light signal is automatically deactivated, and the SUs are turned off while waiting for another trigger signal.
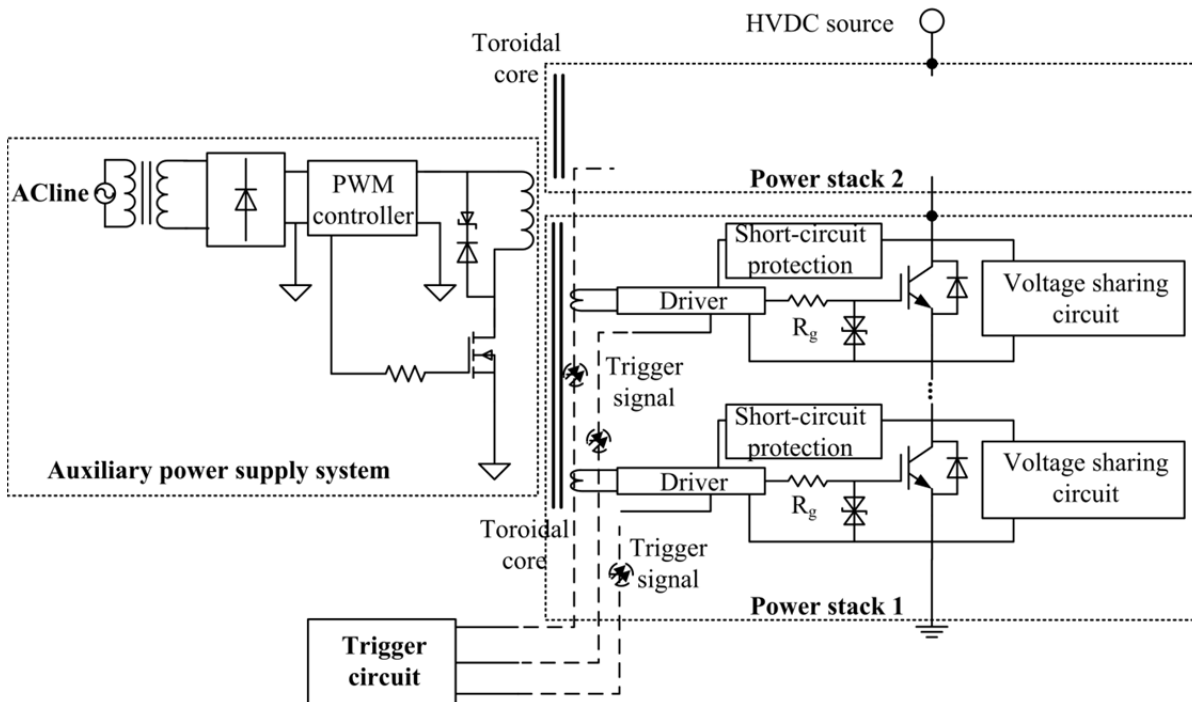
B. Lectotype of the IGBT

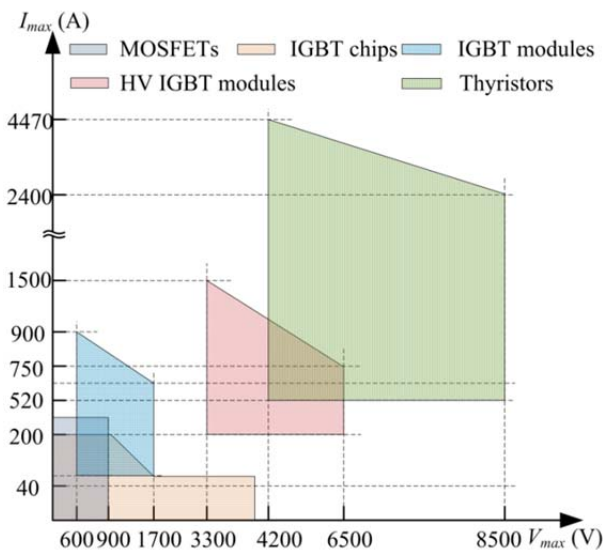Fig. 2. Detailed structure of the proposed HVS.

Fig. 3. Operation range of commercially available semiconductor devices.

Compared with conventional spark gaps, semiconductor devices have many advantages, such as compatibility with digital control systems, fast switching, insensitivity to a harsh environment, and absence of acoustical noise. Moreover, because sparks or electric arcs are not generated during operation, the switches of such devices last long and entail little energy loss. In the present work, we investigated the different types of commercially available devices, namely, MOSFETs, IGBT chips, IGBT modules, and thyristors, in terms of power rate, turn-on speed, size, convenient use, and price. The turn-on speeds of MOSFETs (less than 100 ns) and IGBT chips (less than 500 ns) are much faster than those of IGBT modules (less than 10 μs) and thyristors (less than 30 μs).

Fig. 3 shows the operation range of commercially available semiconductor devices. Regardless of their speed, thyristors have excessive current capability, whereas MOSFETs have limited power rate. With regard to a balance of speed, power rate, size, and price, IGBT chips appear to be the most applicable. In [26], the author recommended the highest rated and lowest number concept. Nevertheless, our selection of device type is based on factors such as economic, lightweight, and easy integration as long as the voltage rate and current capability fit. Let us take two commonly used types of devices as an example. In this example, two 3 kV-rated IGBT chips (IXBF55N300) connected by a string can completely replace the 6.4 kV IGBT module (FZ200R65KF2) in our application, but twice the price of the chip is still much less than one module, let alone the performance. Finally, by using a new IGBT technology, that is, BIMOSFET[TM] [27]-[30], we can raise the voltage blocking capability of conventional IGBT chips to 3 kV without significantly increasing the gate charge and reducing switching speed. As described in [27], [30], this type of IGBT features the advantages of IGBTs and MOSFETs because of its high power rate and switching speed. Moreover, it entails a low gate charge and only requires a compact drive circuit.

The series connection of IGBTs is a solution to the issue of the limited blocking voltage of single devices. The cause of
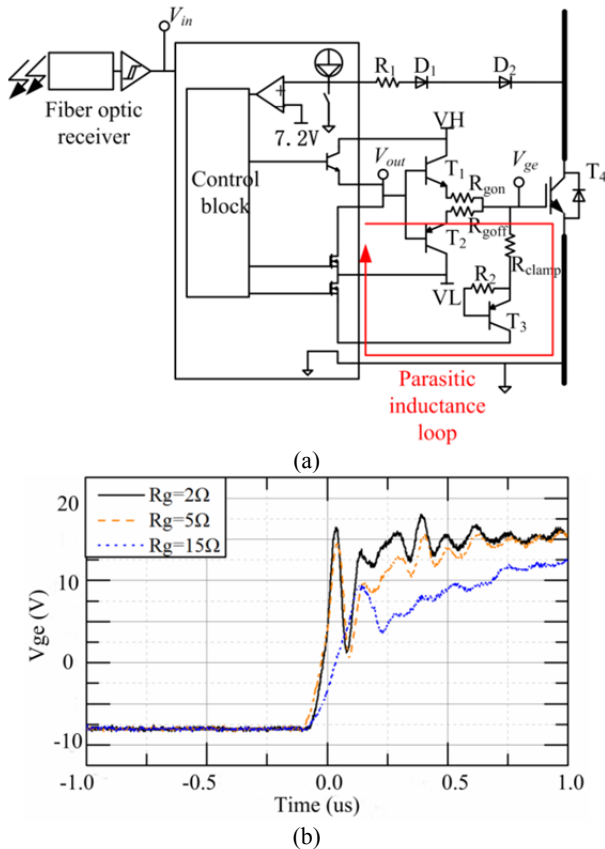
(a)

(b)

Fig. 4. (a) Simplified scheme of the drive circuit of one switch unit and (b) the gate voltage.

and solution to the voltage unbalancing of series-connected IGBTs have been extensively explored in the literature. In [24], the author reviewed different strategies of voltage balancing, namely, active gate control, passive snubber, and voltage clamp circuits. In [26], a hybrid voltage balancing scheme was presented. The influence of parasitic capacitance on voltage sharing was analyzed in [23] and studied further with a numerical approach in [16]. Most studies mainly focused on voltage balancing at turn-off because the tailed current often makes the turn-off process difficult to control. However, in our application, the HVS is turned off after the current and voltage are damped to zero; hence, only the turn-on process needs to be investigated.

C. Drive Circuit and Delay Time Analysis

As shown in Fig. 4(a), a drive circuit is utilized for the selected IGBT. A negative voltage is used during the "off" state to protect the IGBT from the Miller effect. According to the experimental results shown in Fig. 4(b), the gate voltage of the IGBT V_{ge} rings when the gate resistor is too small, whereas the rising edge of V_{ge} becomes too long with a large value of R_g, which indicates the retardation of the switch speed of the IGBT. Finally, we set R_g to 5 Ω to obtain the appropriate gate turn-on voltage. A pair of high-speed push–pull transistors is added to increase the driver current output

TABLE I
DELAY TIME (T$_D$=T2−T1) VARIATION OF EACH IGBT SWITCH
UNIT

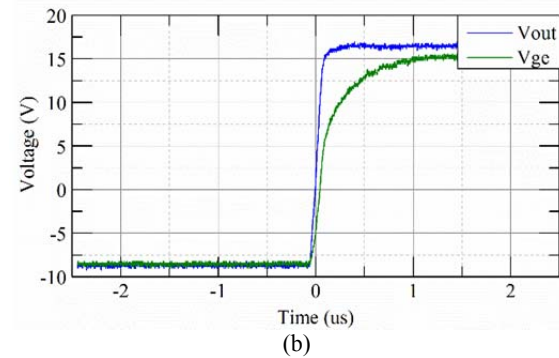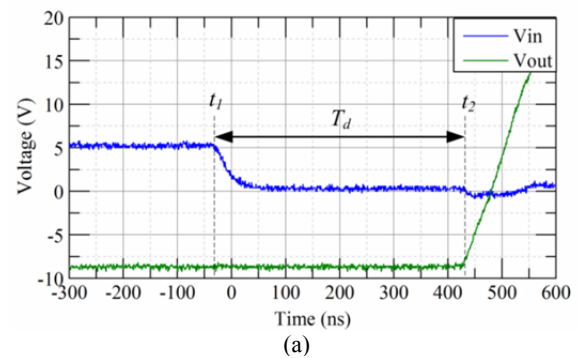| Unit number	Delay time (ns)	
	Stack 1	Stack 2
1	462	457
2	461	460
3	461	461
4	459	460
5	458	458
6	455	459
7	461	461
8	462	462
9	459	462
10	458	461

(a)

(b)

Fig. 5. (a) Delay time between V_{in} and V_{out} and (b) delay time between V_{out} and V_{ge}.

capability. The proper placement of the device and the routing of the printed circuit board (PCB) are considered to avoid stray inductance and the extra parameter spread effect resulting from additional power amplifier circuits. Moreover, the driver is equipped with a desaturation protecting function, which prevents over current in the IGBT chip.

The input to output propagation delay in each gate driver circuit and the spread of device conducting delay must be investigated. First, we used the multi-output fiber transmission system to ensure that the streams of the trigger signal were sent to the IGBT unit at exactly the same time. Second, we chose devices in the same production line, tested each one, and selected those with the least parameter spread.
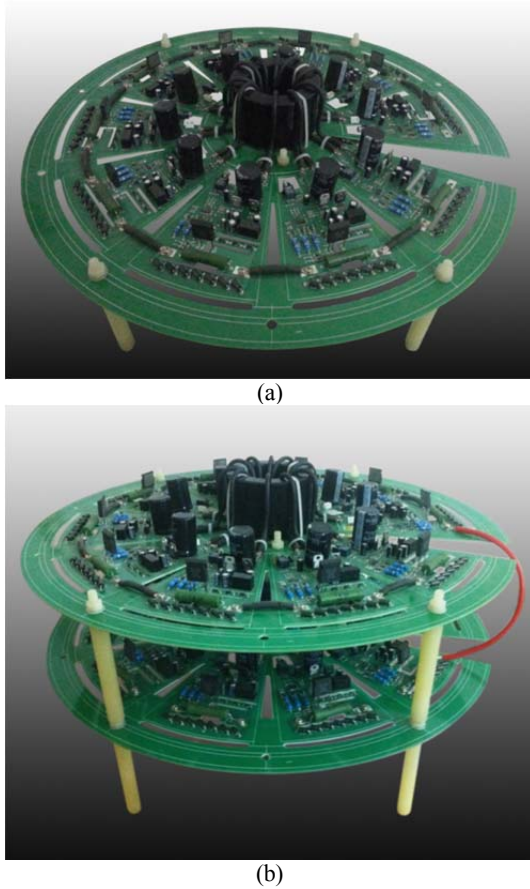
(a)

(b)

Fig. 6. Photographs of (a) a single switch stack and (b) two series-connected switch stacks: ten identical switch units are arranged on one switch stack. Snubbers, IGBT chips, a drive circuit, and secondary sides of the power supply system are successively placed from the outside to the inner side of each switch unit. The toroidal core is placed in the center winded by secondary coils.

After the elaborative placement and routing of the device on the circuit board, the propagation test indicated that the delay of the drive circuits exhibited minimal spread, as shown in Table I. As shown in Fig. 5(a)(b), the drive circuit has an average delay time of approximately 461 ns, and the push–

pull transistors show slight propagation. In our application, these measures reduced the parameter spread of the propagation spread. Thus, the complex gate control method is bulky and expensive.

D. Modular Development of the Prototype

To create a flexible HVS in the assembly, we built the strings of 10 series-connected SUs as stacks, each of which was associated with their accessories based on the module design concept. Therefore, the equipment was constructed as three PCBs: two identical switch stack boards (SSBs) and an auxiliary circuit board (ACB). On the basis of the mechanical connecting relationship, the power supply system comprised two parts: the primary side was the independent ACB, and the core along the multiple secondary sides was placed on the center of the SSB with a direct connection to their supplying SUs. As shown in Fig. 6, each SSB is a disc-type circuit board composed of 10 SUs radially arranged on the pan with a diameter of 60 cm. The fan-shaped gap between the high-side and low-side switch units guarantees an adequate isolation distance and space for passing though the primary side coil. The SSB is hollowed out at the area where the space between the pins is constrictive for HV to avoid surface flashover.

III. DEVELOPMENT OF THE POWER SUPPLY SYSTEM

A. Circuit Topology and Theoretical Analysis

The total number of SUs used for the two SSBs was 20, and the power supply for each SU of 18 V/0.1 A was considered to be adequate. To ensure the compact size of the proposed HVS, the power supply system should involve a simple construction. The multi-output flyback topology is preferred when addressing the HV isolation requirement in a narrow space.

Fig. 7 depicts the proposed power supply circuit. Only one semiconductor switch M_1 is in use, thereby reducing the number of devices and simplifying the control system. The input side transformer Tr_1 is used to step down the voltage
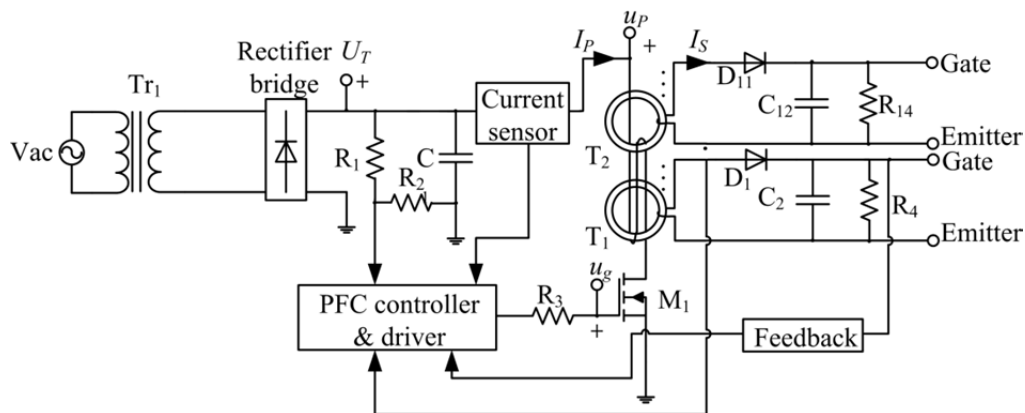

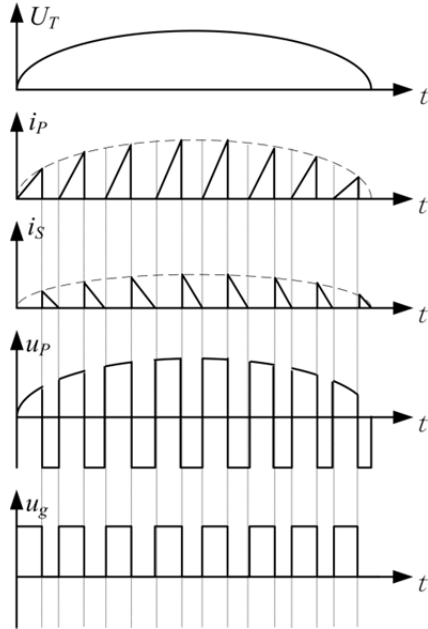Fig. 7. Electric schematic of the proposed power supply circuit.

Fig. 8. Theoretical waveforms of proposed power supply circuit.

from the 220 V AC line to a low-level sinusoid voltage V_{ac}. As mentioned above, each stack is integrated with a core; hence, our power supply scheme comprises two cores, T_1 and T_2, in 30 kV applications involving two series-connected stacks. The two ferrite cores are placed at the center of the two stacks. The primary side winding passes through the two cores and induces energy into each secondary winding for gate driving. Unlike that in a conventional bridge rectifier circuit, the value of C_1 is not very large because it only acts as a filter and not as an energy storage element.

Fig. 8 shows some theoretical waveforms, where U_T is the output voltage of the rectifier bridge, i_P is the primary side current, i_S is the secondary side current, u_p is the primary side voltage, and u_g is the gate voltage of M_1 provided by the controller. The converter works in transient mode with a fixed switching frequency, which means that the switch is immediately turned on as soon as the secondary side current is damped to zero. The controller features two closed loops, an inner current control loop, and an outer voltage control loop. The voltage loop is based on the standard proportional integral controller together with the feedback circuit. The current loop is implemented with a current sensor, which detects the primary side current, and a voltage divider, which is composed of R_1 and R_2 and samples the output voltage of the rectifier bridge as a reference frame. The control targets are identified as a half-sinusoidal enveloped peak value of the primary side current $i_{P(peak)}$ and a constant output DC voltage for each secondary side.

B. High Voltage Isolation between the Loosely Coupled Inductors

The power supply system should provide sufficient energy into each output, be compact in size, and have an adequately
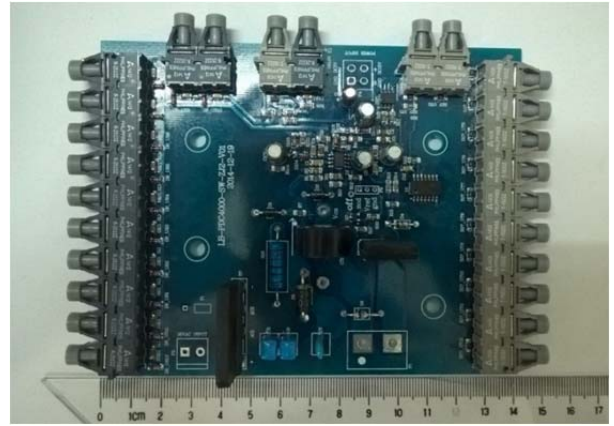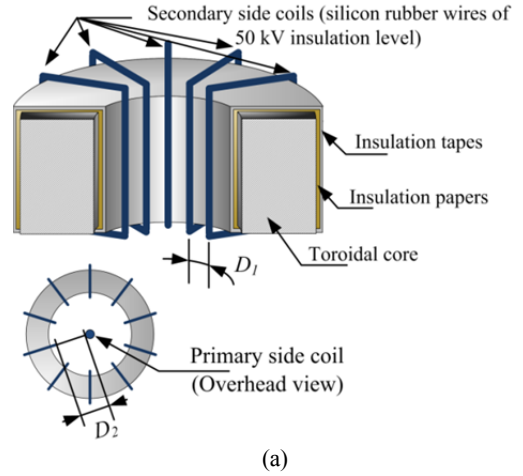

(a)

(b)

Fig. 9. (a) Realization of high voltage isolation and (b) primary side circuit board of proposed power supply circuit.

TABLE II
SPECIFICATION OF THE TOROIDAL CORE

Material		Ferrite
Height (mm)	h	60
Inner diameter (mm)	d	102
Outer diameter (mm)	D	64
Relative flux density	μ_r	2,000
Saturation magnetic flux density (T)	B_s	0.52
Residual magnetic flux density (T)	B_r	0.13

high basic insulation value (BIL). Traditionally, HV isolation is realized by using laminated transformers, whose primary and secondary winding stacks are stacked with interlayer insulation papers [18], [31]. The transformer is clearly bulky in size, and the windings are too close to satisfy the 30 kV BIL requirements in our application even with insulation papers.

In our scheme, the issue is resolved by loosely coupling the primary and secondary side coils through a toroidal core and minimizing the turn of the coils. As mentioned above, consistent with the circular shape of the SSB, the toroidal core can be directly placed in the middle, where all the 10 output coils are wrapped. By using the loosely coupling
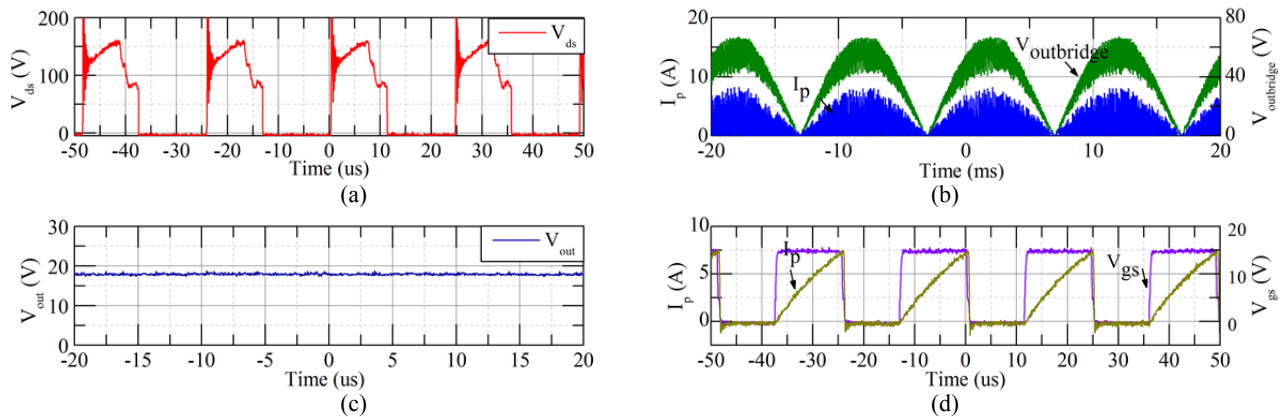
Fig. 10. Key waveforms of the power supply system test with two switch stacks at full load (20 outputs of 18 V, 0.1A): (a) voltage across drain-to-source (V_{ds}) of MOSFET M_1; (b) primary side current I_p and output voltage of rectifier bridge ($V_{outbridge}$); (c) output voltage (V_{out}); (d) detailed I_p and voltage across gate-to-source (V_{gs}) of MOSFET M_1 at $f_{sw(min)}$.

method, the primary side coil passes through the center of the core, and the insulation distance between the primary and secondary side coils is guaranteed. The primary side winding is designed to involve two turns, and the secondary side winding only involves one turn. Hence, the 10 secondary output coils can be juxtaposed on the core instead of being laminated, and the insulation distance is guaranteed.

Inadequate turns of the primary coil cause the primary side inductance to have a relatively low value, inevitably inducing high current peaks $I_{pkp(max)}$. Therefore, the core should be carefully chosen from the commercial types to obtain an adequate reactance value with enough ΔB ($\Delta B = B_s - B_r$, where B_s is the saturation magnetic flux density and B_r is the residual magnetic flux density) in case of saturation. Table II shows the parameters of the chosen toroidal core. The core is bounded by three layers of 0.25 mm insulation papers, with each layer capable of withstanding at least 10 kV breakdown voltage. Then, the papers are taped together and wrapped with the 10 output coils. As shown in Fig. 9(a), the insulation distance of D_1 is measured as 2 cm, and the inner radius of the core D_2 is approximately 5 cm. Moreover, the wires used as the coil are covered by two layers of silicon rubber, and the rated breakdown voltage is higher than 50 kV DC voltage.

C. System Test with Full Load

Finally, the circuit is built with three different parts. The primary side that includes all the devices in front of the primary coil, which provides energy, is placed on an independent circuit board, as shown in Fig. 9(b). Each core is winded by 10 output coils and their auxiliary circuits, and two transformers are separately integrated in the center of the switching stacks. The primary side coil passes through the center of the ferrite cores, coupling the three parts together. After recalculating and refining the other circuit parameters, the primary side coil is reduced to only two turns, and the

secondary side coil is reduced to one turn. All windings are made of silicon rubber-insulated wire rated with 50 kV DC voltage.

The operation condition of the power supply system was tested under full load by adding 10 units of 180 Ω resistors to the output side. The waveforms of the two-stack experiment are presented in Fig. 10. As shown in Fig. 10(c), the output voltage is approximately 18 V as expected. Fig. 10(b) shows that the primary side current I_p is enveloped by a half-sinusoidal-shaped wave and is consistent with the output voltage of the rectifier bridge $V_{outbridge}$. This outcome demonstrates the achievement of the PFC function. Fig. 10(d) shows the detailed I_p and voltage across gate-to-source (V_{gs}) of MOSFET M_1 at $f_{sw(min)}$. We can see that I_p increases as a triangular shape once V_{gs} is +15 V, during which M_1 is turned on, and immediately falls to zero once V_{gs} turns to zero, which indicates that M_1 is turned off. I_p reaches the maximum value at $f_{sw(min)}$; hence, $I_{pkp(max)}$ is read to be almost 7.5 A from Fig. 10(d). At the same time, $f_{sw(min)}$ is approximately 42 kHz, and T_{on} is 14 μs. Fig. 10(a) shows the sharp spike of the rising edge of the voltage across drain-to-source (V_{ds}) of MOSFET M_1, which is due to the resonance effect of the stray inductance of the primary winding and the parasitic capacitance of the MOSFET. In the loosely inductive coupling application of the flyback topology, the number of turns for the primary side coil is only two, and the windings are not tightly mounted on the core; hence, the aforementioned sharp spike is considered inevitable. Even after the addition of the RCD absorption circuit and transient voltage suppressor, the problem is still not perfectly solved.

IV. PARASITIC EFFECT ON GATE VOLTAGE

The effect of stray capacitance between the output coils and parasitic inductance in the emitter of the IGBT during the turn-on process is analyzed, as shown in Fig. 11(a), where L_1

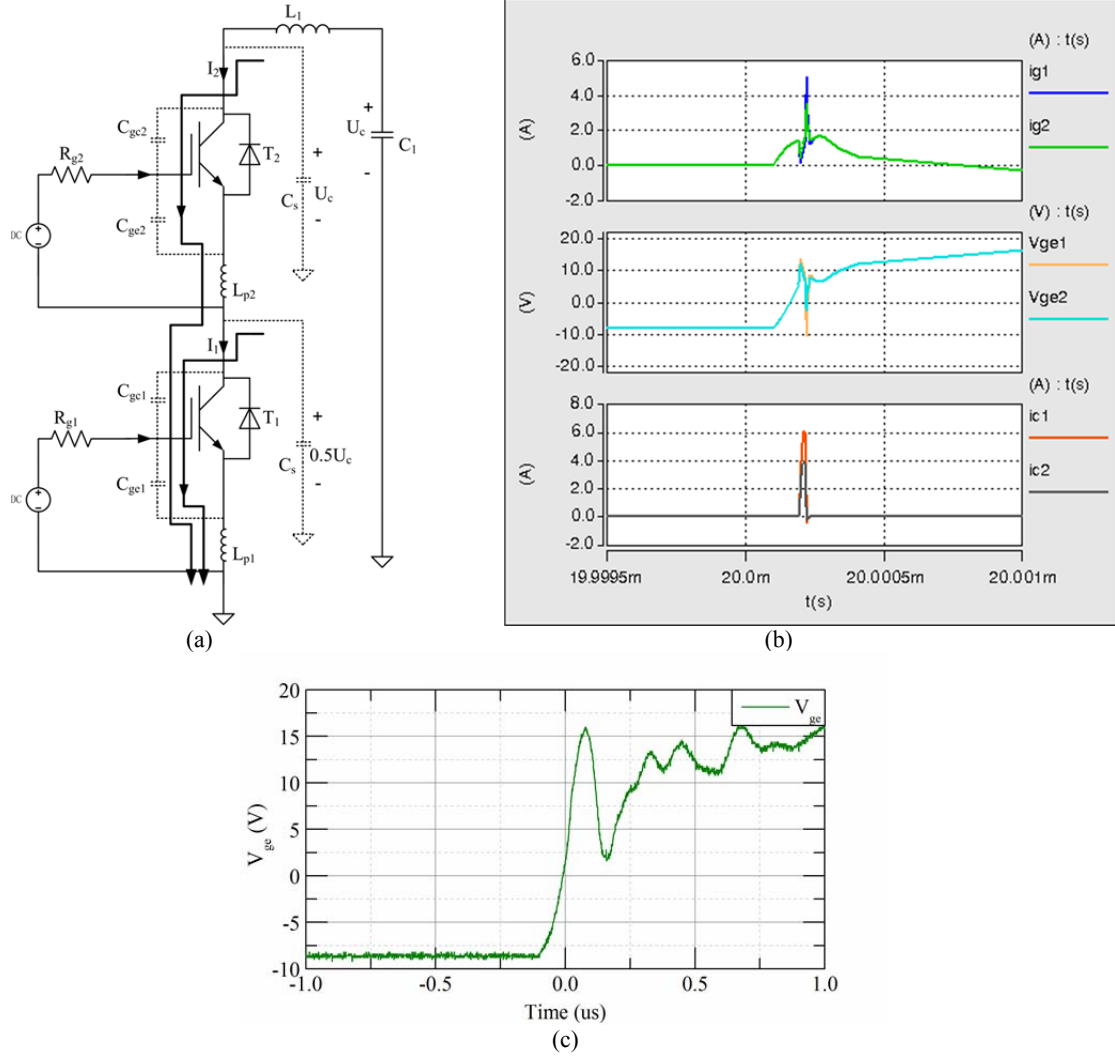(a)   (b)

(c)

Fig. 11. (a) Circuit of parasitic effect analysis. (b) simulation results during turn-on process. (c) gate voltage of the IGBT at the lowest side under 30 kV voltage.

is the air-core inductor and C_1 is the specimen. C_{gc} is the stray capacitance between the gate and the collector of the IGBT T_1 and represents the stray capacitance between two output coils that influences the gate voltage. C_{ge} is the stray capacitance between the gate and the collector, and L_p is the total inner emitter inductance of the IGBT and the parasitic inductance of the gate drive output loop, as shown in Fig. 4(a).

Before turning on the switch, the HVDC source charges C_1 and stray capacitance C_s to the same voltage U_c. As the gate driver output voltage increases, the driver charges C_{ge}. Assuming two devices are synchronously turned on and the voltage balancing method guarantees that the two devices share the same blocking voltage $0.5U_c$, we can obtain the following:

$$\int_{t_0}^{t_0+\Delta t} I_2(t)dt = U_c \cdot C_s \tag{1}$$

$$\int_{t_0}^{t_0+\Delta t} I_1(t)dt = U_c \cdot C_s + \frac{U_c}{2} \cdot C_s \tag{2}$$

where t_0 is the start time, Δt is the duration of the pulse current introduced by the stray capacitance, U_c is the voltage precharged on C_1, and $I_1(t)$ and $I_2(t)$ denote the stray current flowing through the two IGBTs T_1 and T_2 and the parasitic inductor, respectively. We consider the waveform of $I(t)$ as triangular for approximation; from (1) and (2), we can obtain the following:

$$I_{peak2} = \frac{2U_c \cdot C_s}{\Delta t} \tag{3}$$

$$I_{peak1} = \frac{U_c \cdot C_s}{\Delta t} + I_{peak2} \tag{4}$$

where I_{peak1} and I_{peak2} are the peak values of the triangular waves $I_1(t)$ and $I_2(t)$, respectively. We can thus conclude that among the series-connected IGBTs, the lowest side carries the most serious current spike on the gate pole.

This interaction between the stray capacitor and parasitic inductor results in gate voltage ringing. The simulation
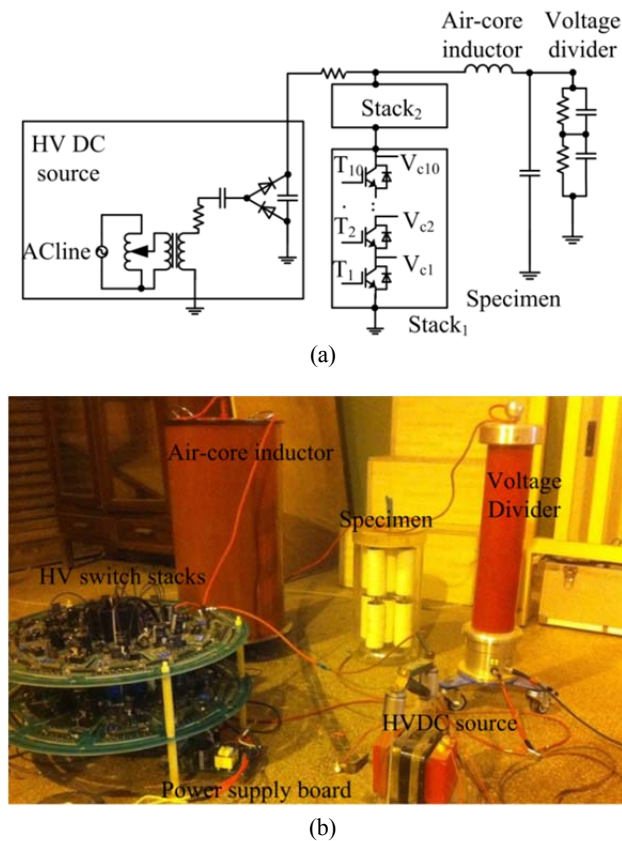
(a)

(b)

Fig. 12. Experiment setup of HVS connected into the DOVTS

results are presented in Fig. 11(b). The proposed HVS comprises numerous series-connected IGBTs that to properly turn on the series-connected IGBT units, the gate voltage, especially that of the lowest side, should be carefully evaluated.

As mentioned above, the circuit board of the switch stack is carefully routed to eliminate parasitic inductance as much as possible. Moreover, the 2 cm insulation distance between the output coils indicates that the stray capacitance C_{gc} is much lower than that of the traditional laminated transformer. Nevertheless, the parasitic effect is considered to be inevitable. After assembling the proposed HVS, we tested its performance under a rated maximum voltage of 30 kV.

Multiple successful turn-on times indicate the reasonably diminished influence of the parasitic effect. Fig. 11(c) shows the gate voltage of the low-side IGBT. The ringing voltage still exists but is negligible.

V. APPLICATION AND EXPERIMENTAL RESULTS

The application-oriented test is performed on the completely built DOVTS at the voltage rate of 30 kV (Fig. 12). The parameters of the testing system are listed in Table III. The air-core inductor is set to 760 mH, and the specimen is a 500 nF CBB capacitor, which is used to substitute the power cable measuring several hundred meters in length. The oscilloscope is a four-channel Tektronix TPS 2024. The switch behavior test is conducted using the HV probe Tektronix P6015A, and the blocking voltage is detected through an independent voltage divider. The input impedance of our HV probe is 100 MΩ; hence, only the collector voltage of the IGBTs on the low-side stack is measured with consideration of the load effect. To decrease the deviation in the turn-on process during the different activation periods of the trigger, each trigger is activated at the same blocking voltage and at the same trigger level. As indicated in Fig. 13(a–c), the collector voltage V_c of the different IGBTs linearly increases, and the turn-on speed is read to be less than 250 ns, which means that the static voltage sharing is generally acceptable. The drop in all V_c happens almost at the same time; hence, all IGBTs are synchronously turned on. Fig. 13(d) shows the measured oscillating voltage on the specimen, which is a perfect damped oscillating waveform. By using (5), which is employed to calculate the oscillating frequency f of the RLC resonant voltage, the following can be obtained:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

where L is the inductance of the air-core inductor and C is the capacitance of the specimen. The oscillating frequency is 258 Hz. Thus, the waveform shown in Fig. 13(d) is consistent with the calculation result.

TABLE III
EXPERIMENTAL PARAMETER CONFIGURATION

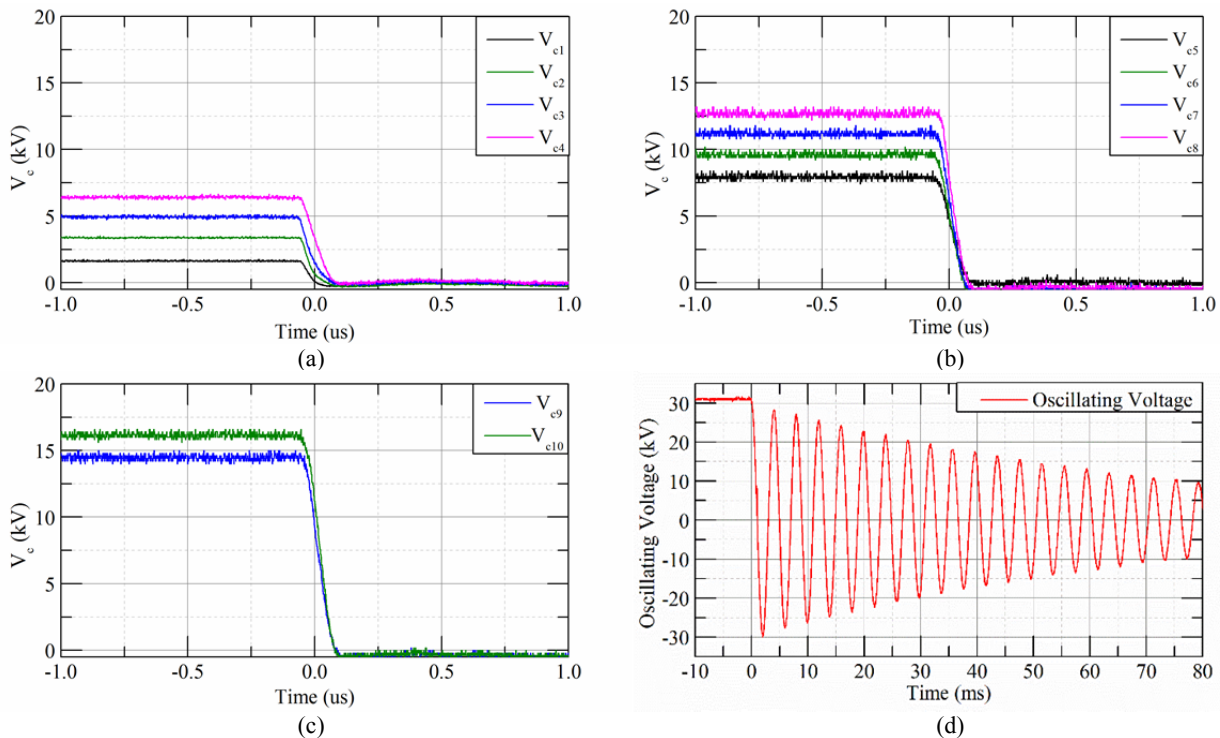| HVDC source	Maximum output voltage	V_{out}	30 kV
Inductor	Inductance value	L	760 mH
	Insulation voltage	V_L	40 kV
Capacitor	Capacitance value	C	500 nF
	Insulation voltage	V_C	54 kV
Proposed HVS	Maximum blocking voltage	U_{max}	30 kV
	Turn-on time	T_{on}	250 ns
Oscilloscope	4 Channels, Tektronix TPS2024		
HV probe	Tektronix P6015A		

Fig. 13. Measurement of two series-connected switch stacks in the DOVTS: (a–c) voltage across collector-to-ground of 10 series-connected IGBTs T1–T10 at 30 kV blocking voltage; (d) 30 kV-rated DOV detected on the specimen.

VI. CONCLUSION

The specification and development of a series-connected IGBT-based solid switch is presented in this paper. By using the modular design concept, the switch is designed to comprise two series-connected switch stacks and a power supply circuit. The two SSBs are loosely inductively coupled with the power supply circuit, thus providing the advantages of flexibility and structural simplicity. These advantages result in a switch with compact size and weight.

The power supply system of a multi-output isolated flyback converter is proposed and tested under full load. This simple structure scheme operates well and provides adequate energy. Finally, a prototype of an optimized HVS is assembled and tested after the evaluation and resolution of possible challenges. Under the proposed operating conditions on a typical DOVTS, the switch works well, and the series-connected IGBTs are almost synchronously triggered. The standard 30 kV-rated DOV on the specimen is also obtained, illustrating that the application of less than 20 kVrms capacitance load tests on the switch is feasible (e.g., 10 kV XLPE power cables).

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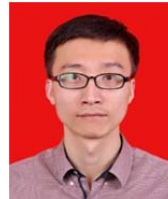
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