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A High-efficiency Method to Suppress Transformer Core Imbalance in Digitally Controlled Phase-shifted Full-bridge Converter

Juzheng Yu*, Qinsong Qian*, Weifeng Sun†, Taizhi Zhang*, and Shengli Lu*

*,†National ASIC System Engineering Research Center, Southeast University, Nanjing, China

Abstract

A high-efficiency method is proposed to suppress magnetic core imbalance in phase-shifted full-bridge (PSFB) converters. Compared with conventional solutions, such as controlling peak current mode (PCM) or adding DC blocking capacitance, the proposed method has several advantages, such as lower power loss and smaller size, because the additional current sensor or blocking capacitor is removed. A time domain model of the secondary side is built to analyze the relationship between transformer core imbalance and cathode voltage of secondary side rectifiers. An approximate control algorithm is designed to achieve asymmetric phase control, which reduces the effects of imbalance. A 60 V/15 A prototype is built to verify the proposed method. Experimental results show that the numerical difference of primary side peak currents between two adjacent cycles is suppressed from 2 A to approximately 0 A. Meanwhile, compared with the PCM solution, the efficiency of the PSFB converter is slightly improved from 93% to 93.2%.

Key words: Approximately digital control, Output rectifier, Transformer core imbalance, Voltage sensor

I. INTRODUCTION

Phase-shifted full-bridge (PSFB) converter is extensively used in medium-power and high-power applications because of its advantages of high efficiency and low electric stress on power devices at the same power level [1]-[4]. Operating in the first and third quadrants of the *B*–*H* curve is an outstanding characteristic of PSFB converters, but easily leads to transformer core imbalance. Transformer core imbalance is normally observed as the unilateral saturation of transformers or excessive electric stress on power devices [5]-[7].

Transformer core imbalance in the PSFB converter is a result of static current offset on the primary side. Current offset is caused by unavoidable unequal on-state resistance of different diagonal power switches, delay of driver circuits, and nonideal PCB parameters [8]. The effect of this imbalance can be reduced by simply adding a DC blocking capacitor to the primary winding of the transformer in engineering applications. However, the blocking capacitor method cannot completely eliminate transformer core imbalance. Moreover, this method has several disadvantages, such as grievous ratio loss, high cost, and low efficiency. In recent years, several new methods are proposed to eliminate the imbalance issue.

A compensation circuit is proposed to reduce transformer core imbalance in an asymmetrically regulated PSFB converter [9]. However, the method is difficult to apply because many external devices are introduced. Moreover, an uncommon asymmetric full-bridge controller that separately controls the phases of diagonal power switches is necessary.

An accurate model and a digital compensator are proposed in [10]. The model is built to analyze the relationship between nonideal parameters and offset current on the primary side. However, the current sensor in the proposed solution leads to extra cost and power loss, which limit the application range.

Given the disadvantages of low efficiency and high material cost in common transformer core imbalance solutions, a high efficiency and simple method is proposed in this study.

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†Corresponding Author: swffrog@seu.edu.cn
Tel.: +86-25-83795811, Fax: +86-25-83795077, Southeast University
*National ASIC System Engineering Research Center, Southeast University, China

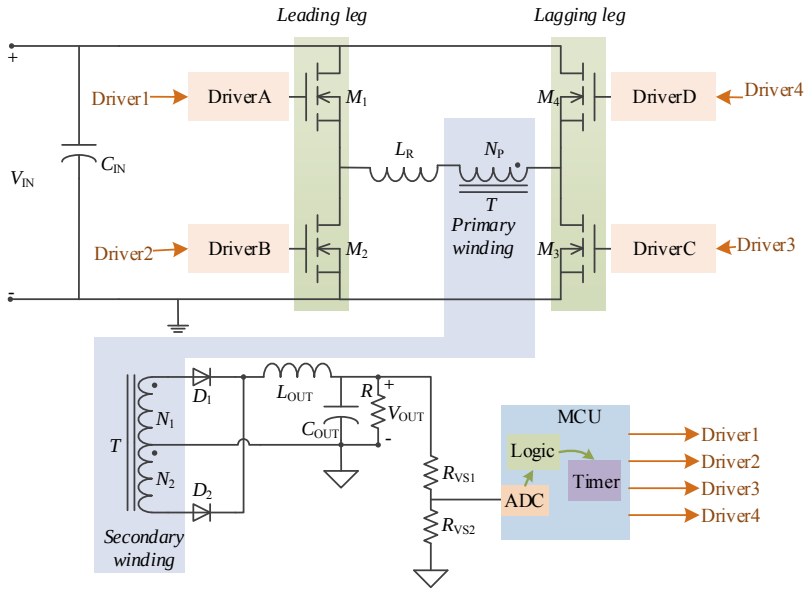

Fig. 1. Basic PSFB converter.

In this study, a transient model is built to analyze the relationship between the imbalance of the magnetic core and cathode voltage of output rectifiers on the secondary side. An approximate control algorithm that eliminates the effect of transformer core imbalance is achieved by a low-cost microcontroller. This paper is organized as follows: In Section II, a conventional PSFB converter is analyzed and simulated to investigate the relationship among the cathode voltage of output rectifiers on the secondary side, primary side current, and magnetic core imbalance. A digital compensator is proposed in Section III, including an external sample circuit and an internal control algorithm. In Section IV, a 60 V/15 A prototype is built and tested to verify the effect of the proposed method compared with conventional PSFB converters.

II. Theoretical Analysis of Transformer Core Imbalance

A. Transformer Core Imbalance in PSFB Converters

A conventional PSFB converter regulated based on a microcontroller is shown in Figure 1. The primary side includes input capacitor C_{IN} and power MOSFETs *M1–M4*. L_R represents the sum of the resonant inductor and leakage inductance of the transformer; N_P represents the primary winding of the transformer; and N_1 and N_2 represent the secondary windings of the transformer. The secondary side consists of output rectifiers *D1–D2*, filter inductor L_{OUT}, and filter capacitor C_{OUT}. R represents the load. Feedback and control components are composed of sample resistors R_{VS1}–R_{VS2} and a microcontroller. The internal ADC module samples the feedback voltage, which is divided by R_{VS1}–R_{VS2} from output voltage V_{OUT}. The function of the logic module is calculating the phase of diagonal transistors. The internal timers output four pulse signals, Driver1–Driver4, based on the logic module. Driver1–Driver4 control V_{GS} of power MOSFETs when amplified by the isolated circuits DriverA–DriverD.

$R_{DS(on)}$ of *M1–M4*, related parasitic parameters of PCB, and delay time caused by isolated drivers cannot be completely equal because of design and manufacturing limitations. The inequality causes a deviation between positive and negative peak currents on the primary side, which leads to inevitable imbalance of the transformer core in the PSFB converter.

Transformer core imbalance is directly decided by the DC offset of the primary current and is affected by several other phenomena. For example, unequal peak values of the primary current also illustrate the imbalance condition of the transformer core, which has been utilized by peak current mode (PCM) control. A current sensor is required to sample the primary current, which increases the material cost and power loss of the PSFB converter.

B. Transformer Core Imbalance Reflexed by a Voltage Signal

Aside from the peak values of the primary current, another phenomenon also causes transformer core imbalance, that is, voltage oscillation ring of the anode and cathode of rectifiers *D1* and *D2* on the secondary side, as shown in Figure 1. Even if *RC* snubbers are paralleled to *D1–D2*, voltage peaks can be detected on the anode and cathode voltages of *D1* during overlapping of *M1* and *M3* or on the anode and cathode voltages of *D2* during overlapping of *M2* and *M4*, as illustrated in Figure 2. Given that the cathode of rectifiers is directly connected, V_K is simulated with primary current I_P instead of voltage of anodes in Figure 2.

In Figure 2, the peak values of I_P and V_K are measured; the

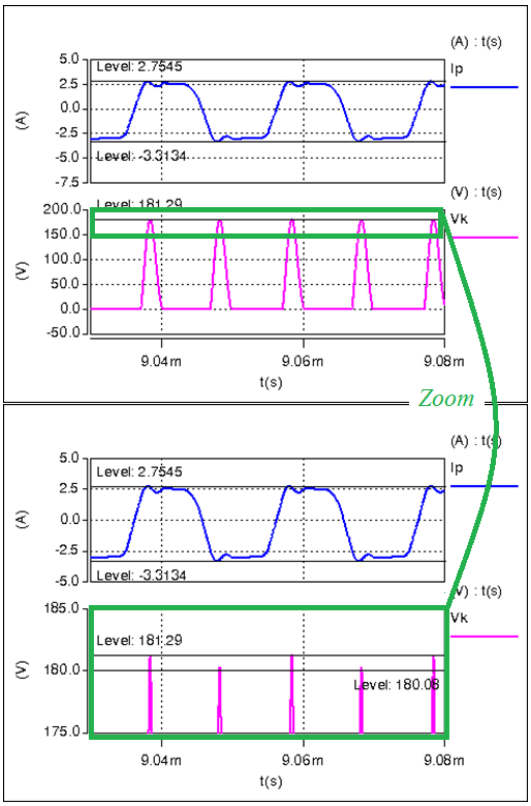

Fig. 2. Simulated waveform of V_K and I_P.

range of V_K is adjusted to show inequality. Unequal peak values of I_P and V_K in a switching cycle are illustrated, which indicate that the voltage signal includes information of the imbalance condition of the magnetic core. Moreover, the relationship between oscillation ring $V_{K(D2)}$ (V_{D2}) and primary current $i_p(t)$ in the PSFB converter without *RC* snubbers is verified, which proves that V_K is infected by I_P.

Confirming whether the relationship remains correct when *RC* snubbers are added is necessary. *RC* snubbers are extensively used to prevent overvoltage stress on *D1* and *D2*. The relationship between V_K and I_P in PSFB converter with *RC* snubbers should be investigated, such that analysis based on V_K can be proven effective.

We let t_1 denote the finish time of the ratio loss procedure, which transfers no energy from the primary side to the secondary side. Figure 3 illustrates the schematic and equivalent circuit of the PSFB converter with *RC* snubbers during the energy transfer procedure from the primary side to the secondary side (defined as t_1–t_2). During t_1–t_2, *M1* and *M3* are on, and the on-state resistances are R_{DS1} and R_{DS3}. Inductors L_R and L_P are charged, and the primary side current $i_P(t)$ can be expressed as follows:

$$i_P(t)=\frac{V_{IN}-i_P(t)\cdot(R_{DS1}+R_{DS3})}{L_R+L_P+K^2L_{OUT}^2}\cdot t+I_P(0)\cdot \tag{1}$$

Secondary current has two parts (Figure 3(a)). The green line denotes that current flows through L_{OUT} to provide output

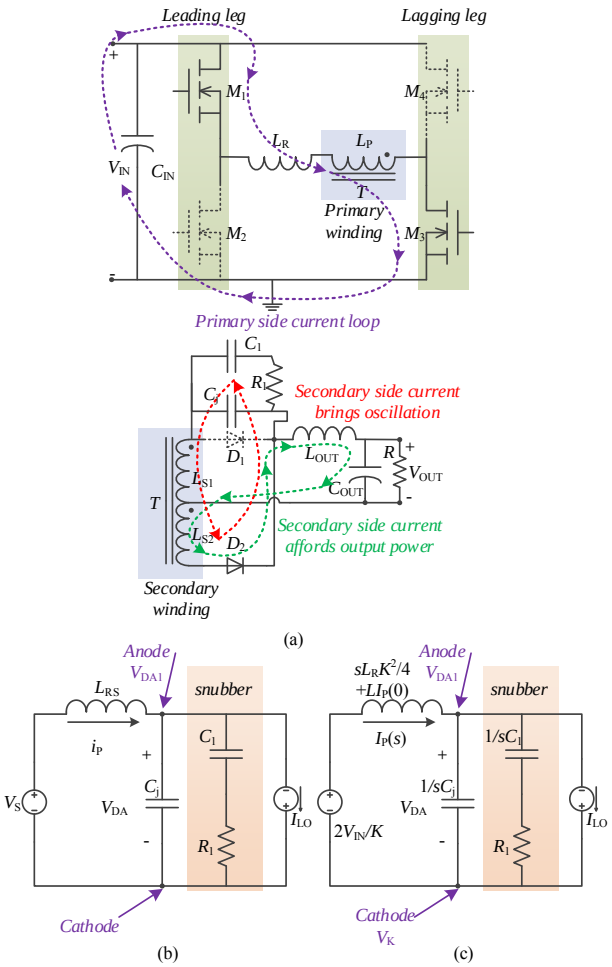

Fig. 3. Equivalent circuit to reflex anode/cathode voltage of secondary side rectifier.

power. L_{OUT} is sufficiently large that L_{OUT}, C_{OUT}, and R can be replaced by constant current source I_{LO} during t_1–t_2. Meanwhile, the red line denotes that current flows through junction capacitance C_j of *D1* and *RC* snubber, which causes resonance of $v_K(t)$ when $i_P(t)$ increases to its peak value. If L_R is converted from primary side to secondary side, then the circuit can be simplified based on the operation principle of the transformer (Figure 3(b)).

By converting inductance L_R and voltage across L_P to the secondary side, the turns ratio can be expressed as $K = (L_P/L_{S1})^{0.5} = (L_P/L_{S2})^{0.5}$, L_R becomes $L_{RS} = K^2L_R/4$, and voltage across the secondary windings is $V_S = 2V_{IN}/K$. By transferring the circuit from the time domain to the complex frequency domain, as shown in Figures 3(b) and 3(c), the voltage across C_j can be calculated as follows:

$$\frac{\frac{2V_{IN}}{K}-V_{DA}+LI_P(0)}{\frac{K^2}{4}sL}=\frac{V_{DA}}{\frac{1}{sC_j}}+\frac{V_{DA}}{\frac{1}{sC_1}+R_1}+I_{LO} \tag{2}$$

(a) Current loop during t_1–t_2

(b) Equivalent circuit in the time domain during t_1–t_2

(c) Equivalent circuit in the complex frequency domain during t_1–t_2

In Equation (2), $I_P(0)$ represents the primary current at t_1. Moreover, if the forward drop of the rectifier is neglected, then $v_K(s)$ in the complex frequency domain can be expressed as follows:

$$v_K(s) = V_{DA}(s) = \frac{-s^2K^2L_RR_iC_iI_{LO} + s\left(\frac{8R_iC_iV_{IN}}{K} - K^2L_RI_{LO} + 4L_RR_iC_iI_P(0)\right) + \frac{8V_{IN}}{K}}{s^3K^2L_RC_jR_iC_i + s^2K^2L_R(C_j + C_i) + s\cdot 4R_iC_i + 4} \quad (3)$$

$v_K(s)$ is a three-order function of variable s according to Equation (3). The initial value of the primary current infects the voltage, which is simulated in the time domain by *Matlab* (Figure 4). Two values of $I_P(0)$ are compared in the same coordinate system, which shows that a higher $I_P(0)$ is equivalent to a higher V_K. A comparison between the simulation results and tested results proves that the shape of the simulated waveform is similar to the tested waveform when the DC value is neglected. This comparison proves that $v_K(t)$ reflexes $i_P(t)$, particularly with the difference between the two directions during one cycle.

According to Figure 4, the theory that V_K is related to I_P is proven, which indicates that the difference in the peak values of V_K in one cycle reflexes the balance condition of the transformer core in the PSFB converter. Magnetization processes in the first and third quadrants of the *B–H* curve are asymmetric; thus, the offset value of the primary side current can be observed, which should be zero in a balanced condition.

Given that the peak value of V_K is directly affected by the primary side current, V_K can be used to acquire imbalance state information of the transformer core. If the transformer core is balanced, then the peak value $V_{K\text{-PEAK(D1)}}$ should be equal to peak value $V_{K\text{-PEAK(D2)}}$ and *D1* and *D2* represent different rectifiers in different phases. According to the simulations, tests, and theoretical analysis described in this section, the difference between $V_{K\text{-PEAK(D1)}}$ and $V_{K\text{-PEAK(D2)}}$ affects the imbalance of the transformer core. The conclusion represents the theoretical foundation of the proposed suppression method.

III. Design of a Digital Phase Compensator

A. Control Algorithm and Program Loop Design

Based on the analysis presented in Section II, a new method that samples V_K as another feedback variable can be proposed. Transformer core imbalance is currently suppressed accurately cycle-by-cycle using PCM. However, in practical applications, serious consequences, such as unilateral transformer saturation or power device failure, are caused by a continuous single-direction imbalance. A current offset in one single-switching cycle causes no harm. Thus, the

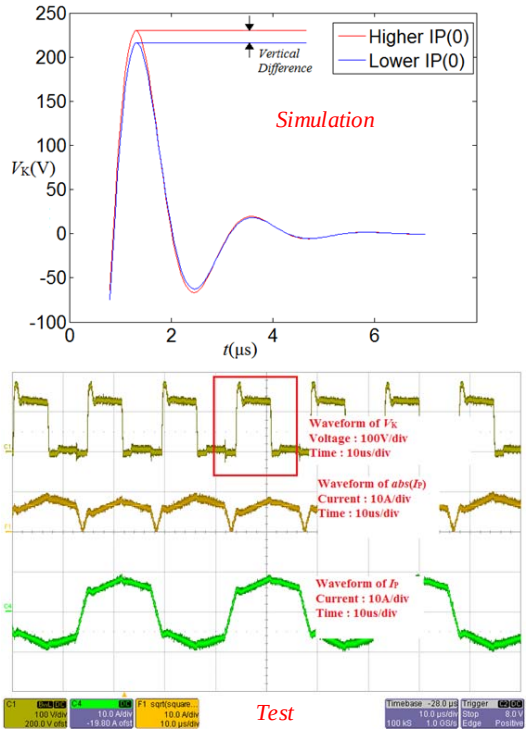

Fig. 4. Simulated time domain waveform of VK compared with the tested waveform.

main idea of suppression in this study is to limit the imbalance range and swing imbalance direction.

If the static offset value of primary side current I_{P_OS} is controlled to alternate between positive and negative, then the average value of I_{P_OS} would be approximately zero during most periods:

$$\frac{1}{n}\sum_{n=0}^{n} I_{P\_OS(n)} \to 0 \cdot \quad (4)$$

In Equation (4), n represents the amount of switching cycles.

Based on the equation, regulating I_{P_OS} with an approximate method is considered to be effective. When the sign of I_{P_OS} changes, the magnetic offset of the transformer can also be controlled to alternate between positive and negative, and the amplitude of imbalance in one switching cycle can be suppressed as well. Although transformer core imbalance occurs during the entire operation procedure, the imbalance is bidirectional and significantly limited; thus, the average value of magnetic flux $\bar{\Phi}$ is also approximately zero in most switching cycles.

According to the analysis, an asymmetric phase regulation method should be applied to maintain a low I_{P_OS} in each cycle. Moreover, the positive or negative sign of I_P cannot be maintained for a long period of time. Thus, the phase difference between *M1–M3* and *M2–M4* should be regulated based on the imbalance state of the transformer core, which is represented by the numerical relationship between the

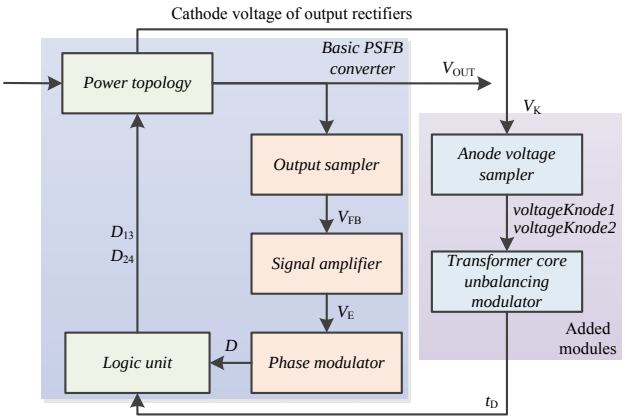

Fig. 5. Control diagram of the proposed solution.

maximum value of $V_{K\text{-}PEAK(D1)}$ and $V_{K\text{-}PEAK(D2)}$ in the proposed solution (Figure 5).

Compared with the PSFB converter with a conventional controller, an external voltage sampler that is used to sense cathode voltage V_K from output rectifiers is inserted to the control loop (Figure 5). Moreover, a few extra algorithm modules are added to the program cycle of the microcontroller in the proposed solution.

In a normal switching cycle, output voltage V_{OUT} of the power topology is sampled by output sampler R_{VS1}–R_{VS2} (Figure 1). The sampled voltage V_{FB} turns into the error signal V_E after being amplified. V_E is the input of the phase modulator, which is used to calculate phase *D*. In a conventional PSFB converter, the phases of *M1–M3* and *M2–M4* output by the microcontroller are equal to *D*. However, the phases of power MOSFETs are not the same as previously mentioned. This issue is one of the main factors of transformer core imbalance; thus, imbalance problems can be solved by deliberate unequal phases of *M1–M3* and *M2–M4*.

Figure 6 shows the procedure of the phase controller. To achieve asymmetric regulation in the proposed solution, the peak values of voltage signal V_K are captured by the internal ADC of the microcontroller and then converted to digital variables *voltageKnode1* and *voltageKnode2* in the sample function. The difference between *voltageKnode1* and *voltageKnode2* reflects the imbalance state of the transformer core in the current cycle. Extra transformer imbalance modulator outputs time variable t_D, which is the other input of the logic unit, except for phase *D*. The function of the logic unit is to generate phases $D_{13(n)}$ and $D_{24(n)}$ based on the current phases $D_{13(n-1)}$ and $D_{24(n-1)}$, calculated phase *D*, and time variable t_D. $D_{13(n)}$ and $D_{24(n)}$ would be assigned to related registers of internal timers to modify the phases of *M1–M3* and *M2–M4* in the subsequent cycle.

Compared with the conventional digital phase controller of the PSFB converter, the proposed digital phase controller inserts different phase calculation functions to the main

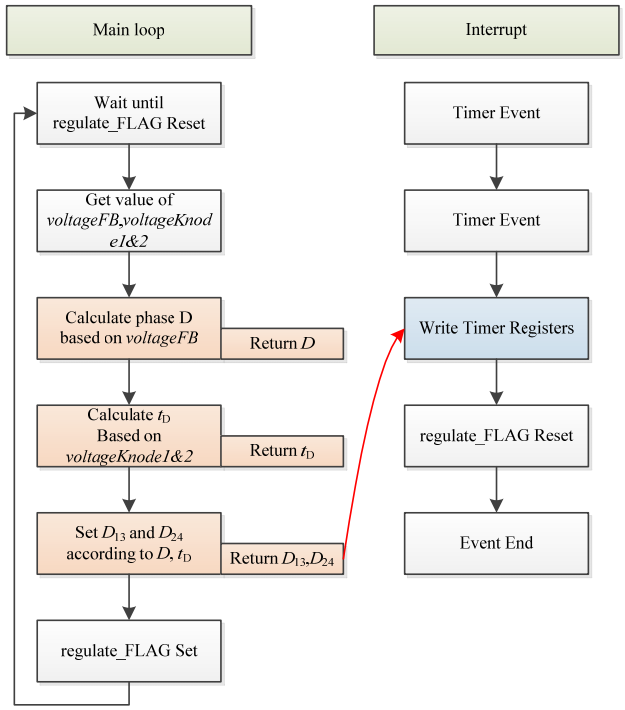

Fig. 6. Procedure of the phase controller.

program loop.

The driver signals of *M1* and *M2* are generated by one of the advanced timers in the microcontroller. These two signals would never be regulated, which indicates that the period, ratio, and dead time of *M1* and *M2* remain constant. The driver signals of *M3* and *M4* are generated by another advanced timer in the microcontroller. They are regulated in program interruptions based on the values of *voltageFB*, *voltageKnode1*, and *voltageKnode2*. Phase *D* of the subsequent cycle is set with an initial value, which is calculated based on the phases and sampled *voltageFB* in the current cycle. In the current cycle, *voltageKnode1* and *voltageKnode2* are also sampled and compared with the obtained magnetic offset condition.

The numerical value of t_D is set to be constant to simplify the control loop; however, the sign of t_D would be positive or negative according to the relationship between *voltageKnode1* and *voltageKnode2*. The phases of *M1–M3* and *M2–M4* in cycle *n* are calculated as follows:

$$\begin{cases} D_{13(n)} = f_1\left(D_{13(n-1)}, D\right) + t_D \\ D_{24(n)} = f_2\left(D_{24(n-1)}, D\right) - t_D \end{cases}. \quad (5)$$

As Equation (5) shows, the phases in the subsequent cycle are related to the phases in the last cycle, the calculated phase in the current cycle, and the imbalance state in the current cycle. If the direction of transformer core imbalance is reflected as $V_{K\text{-}PEAK(D1)} > V_{K\text{-}PEAK(D2)}$, then $I_{PEAK(M1\text{–}M3)} > I_{PEAK(M2\text{–}M4)}$ in the current cycle T_n, and t_D would be negative

to decrease D_{13} and increase D_{24} in the subsequent cycle T_{n+1}. If the direction of transformer core imbalance in T_{n+1} retains the state of T_n, then t_D would again have a negative value and D_{13} in T_{n+2} becomes smaller than D_{13} in T_{n+1}.

Moreover, the sign of t_D would not change until condition $V_{K\text{-}PEAK(D1)} > V_{K\text{-}PEAK(D2)}$ becomes $V_{K\text{-}PEAK(D1)} < V_{K\text{-}PEAK(D2)}$. When $V_{K\text{-}PEAK(D1)} < V_{K\text{-}PEAK(D2)}$ is built in one cycle, the phase controller would change the sign of t_D to build $V_{K\text{-}PEAK(D1)} > V_{K\text{-}PEAK(D2)}$. Thus, a limited transformer core imbalance is achieved, which no longer causes unilateral saturation of the transformer and power device failures.

B. Design of the RC Snubber of Output Rectifiers

The *RC* snubber is used to decrease voltage stress across the rectifier [11]. The purpose of designing the RC snubber is based on power loss and stress margin. Quality factor Q is defined as the reflex oscillation in the *RLC* circuit:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}. \tag{6}$$

In PSFB applications, the oscillation ring should be suppressed to an underdamping state to make our method effective while ensuring that voltage stress is safe for the rectifiers. The value of R_1 can be determined as follows:

$$R_i \le \sqrt{\frac{L_i}{C_j}}. \tag{7}$$

In Equation (7), C_j can be derived from the datasheet and L_i can be calculated as follows:

$$L_i = \frac{1}{K^2}\left(L_R + L_{leak}\right) = \frac{L_R}{K^2}. \tag{8}$$

C_1 is selected in the range of:

$$\frac{L_i I_P^2}{V_{out}^2} < C_1 < \frac{1}{10R_S}\cdot\frac{T_S}{2}. \tag{9}$$

Parameter I_P is the initial value of the primary side current, and T_S represents the period of the PSFB converter. Based on these design considerations, the RC snubber ensures a single ring while the amplitude of the ring is suppressed.

C. Special design of the voltage sensor to sample transformer core imbalance

Program achievement of asymmetric regulation has been proposed; however, the ADC sampler needs special consideration because of difficulty in sampling the peak value of V_K.

To sample a reliable V_K, a digital signal process function is designed in the microcontroller to capture voltage at a specified time. Sampler design has two rules, as follows:

1) According to the errors of the sampler, several different points should be sampled to filter spikes.

2) Several points unavoidably lead to error of the desired point; thus, the start and end times of the sampler should be set properly based on the relationship between PWM driver and V_K waveform.

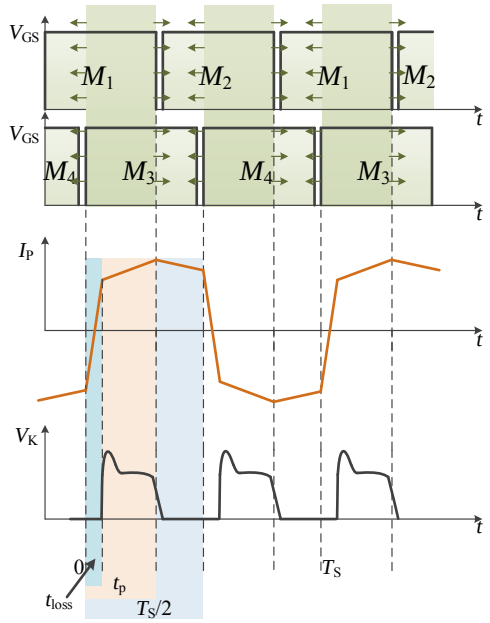

Fig. 7. Waveform of VGS and primary side current.

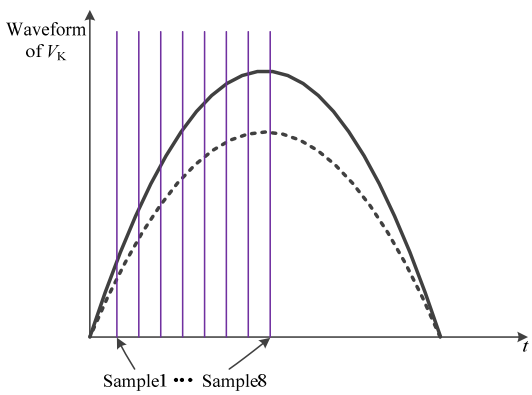

Fig. 8. Digital sample design consideration.

Based on the rules, the special design of the sampler should be considered. Period T_S of the PSFB converter is set by the designer and executed by the MCU, and phase t_P of two diagonal MOSFETs is decided by the MCU. Moreover, duty cycle loss time can be calculated as follows:

$$t_{loss} = \frac{2I_{peak}\left(L_R + L_{leak}\right)}{V_{in}} = \frac{2I_{peak}L_R}{V_{in}}. \tag{10}$$

I_{peak} is the peak value of the primary side current, L_R is the resonant inductance, L_{leak} is the leakage inductance of the transformer, and V_{in} is the input voltage.

According to these settings and calculations, the specific time of the oscillation ring peak is easy to locate; however, sampling the exact value during software execution is difficult particularly because no external sample/hold circuit is added.

Thus, sample consideration in the software should be based on multiple samples; in this case, average value of sampled

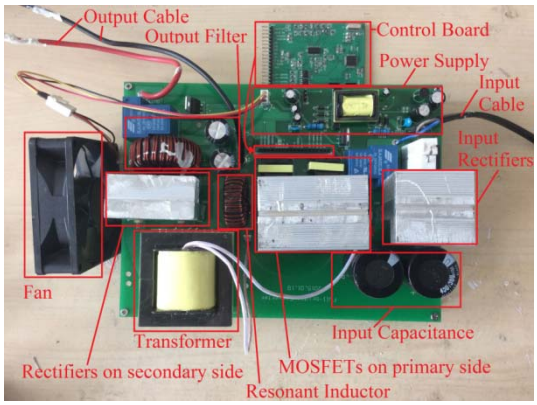

Fig. 9. Photograph of the 60 V/15 A prototype.

points is used to reflex true V_K. The proposed mechanism is to sample several values right after t_{loss} and $T_S/2 + t_{loss}$, as shown in Fig. 7. A higher peak value of V_K indicates a higher sampled value at the corresponding time during the first oscillation ring, such that the accurate average value can be calculated if the sample time is ensured to be sufficiently accurate. Then, these values are averaged to be V_K in the half period, as illustrated in
Fig. 8.

When data V_K [1, …, n] are stored as variables in each phase, an extra process is necessary to generate a reliable variable, which is called the calculating function of t_D:

$$\overline{V}_K = \frac{1}{X}\sum_{x=1}^{X} V_{K(x)} . \tag{11}$$

The average method is the easiest way to process data if point number x in Equation (11) is set as 2^M, such as 4, 8, and 16. The point number should be set according to the cost of the sampler because a large amount of data in the sampling module can easily cause poor loop response. Finally, the number of M is set as 3, such that the average value of V_K can be rapidly calculated.

Based on these considerations, an asymmetric phase controller is developed. Two external resistors are connected between the cathode of the output rectifiers and output ground to divide the large voltage. The divided voltage is one of the analog inputs of the microcontroller. The designed program generates four channels of PWM signal with asymmetric phases to control power MOSFETs. The test results are given in the subsequent section to show the effect of the proposed method.

IV. Experimental Results

A 220 VAC input, 60 V/15 A output prototype is built to verify the effect of the proposed method (Fig. 9). The PSFB converter consists of two PCBs vertically connected via plug-in parts. The PSFB topology board includes basic PSFB converter, isolated drivers of four power MOSFETs, and power supply for chips, fan, and driver circuits. The control board is made up of voltage followers, a 48 MHz microcontroller (STM32F051xx from STMicroelectronics), and driver ICs. The main parameters that correspond to the circuit in Figure 1 are shown in Table I.

TABLE I
Parameters of the PSFB Converter

Description	Designator	Value/model
Input capacitor	C_{IN}	470 µF/470 µF
Power MOSFET	*M1–M4*	IRFPS30N60K
Resonant inductor	L_R	50 µH
Transformer	*T1*	$N_P/N_1 = N_P/N_2 = 2$
Output rectifier	*D1–D2*	DSEI30-06 A
Output inductor	L_{OUT}	130 µH
Output capacitor	C_{OUT}	470 µF/470 µF
Load resistor	R	4 Ω
Divide resistors	R_{VS1}/R_{VS2}	220:1 kΩ
Error amplifier factor	k	1
Switching frequency	f_S	35 kHz
Phase	D	1.8–10 µs
Dead time	t_{DIE}	860 ns

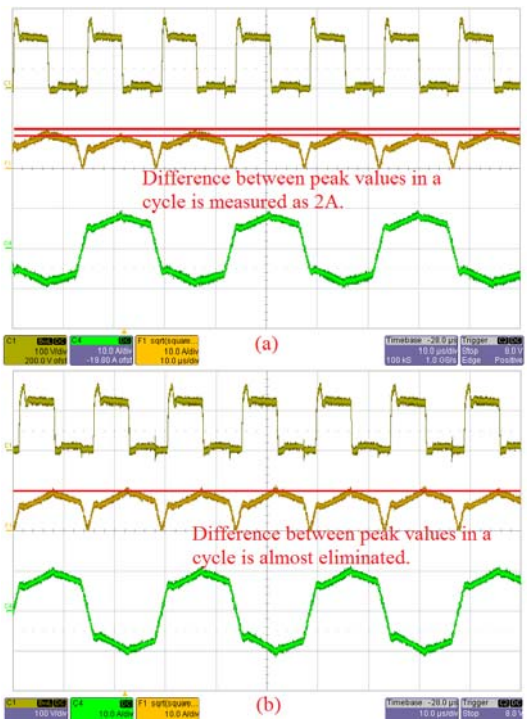

Fig. 10. Test waveforms of VK and IP (test condition: 310 V input, 60 V/15 A output): khaki, VK (100 V/div); brown, abs(IP) (10 A/div); green, IP (10 A/div); time, 10 µs/div: (a) Basic PSFB converter without asymmetric control, (b) SFB converter with the proposed control method.

In a regular PSFB converter without asymmetric control under 310 VDC input and 59 V/15 A output condition, waveforms of the primary side current and cathode voltage of output rectifiers are tested, as shown in Fig. 10(a).

Given that the peak value of the primary side current in waveforms has alternating signs, the green line is difficult to

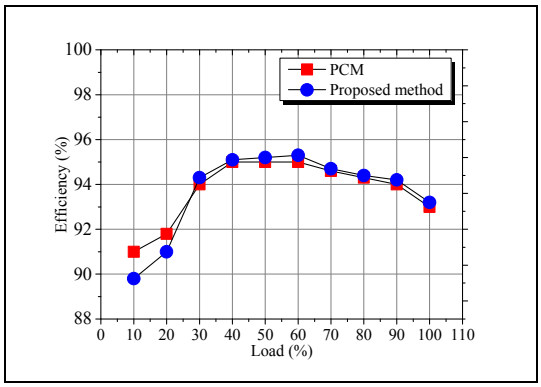

Fig. 11. Efficiency comparison of PCM and the proposed method (test condition: 310 V input, 60 V/1–15 A output).

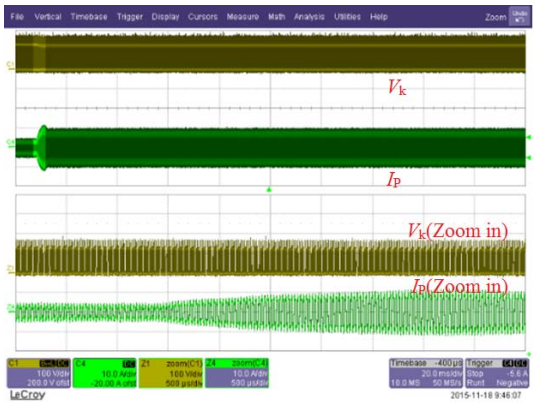

Fig. 12. Load variation from 6 A to 15 A (test condition: 310 V input, 60 V/6–15 A output).

TABLE II
SUPPRESSION EFFECT COMPARISON BETWEEN PCM AND THE PROPOSED METHOD

Time	PCM	Proposed method
1 period	0	200 mA
10 periods	0	16 mA
1 s	0	0

detect. Thus, a square–square root mathematical (absolute value, *abs*) calculation is executed to shift the negative to positive, shown as the brown line in Fig. 10(a). The difference between two adjacent cycles is measured as 2 A according to the red auxiliary lines, which indicates that magnetic offset is sufficiently significant to affect the reliability of power devices.

Fig. 10(b) shows the experimental results when the proposed method is utilized by a conventional PSFB converter. Waveforms are tested under the condition of 310 V input and 59 V/15 A output. The test results are equal to the prototype under symmetrical control technique and higher than the converter with blocking capacitance.

In Fig. 10(b), the primary side current is also processed to a nonnegative range, shown as a brown line. A red auxiliary line is drawn in Fig. 10(b), where the peak value of $abs(I_P)$ is approximately equal to the adjacent cycle, which indicates that the imbalance of the magnetic core is effectively suppressed.

In addition, other indices should be tested to verify the proposed method. Efficiency under different load currents is tested. Fig. 11 shows that efficiency is higher in the proposed method than that in the PCM in the load range of 30–100%. The peak value of efficiency in the proposed method is 93.2%, which is 0.2% higher than that in the PCM solution.

Moreover, the suppression effect of the two methods is compared to prove the effectiveness of our method. Notably, the proposed method does not reduce the imbalance of the transformer core in a single period. The purpose of the proposed method is to regulate the direction of the imbalance, such that the average peak current on the primary side is zero for a long period of time. Table 2 shows the comparison between PCM and the proposed method. The experimental results prove that the effect of our method is not as good as that in PCM, although the proposed method achieves the objective of imbalance suppression for the entire operation procedure.

According to these experimental results, the proposed method is proven to be effective in suppressing the imbalance of the transformer core, and its efficiency is slightly higher than that in the PCM solution.

Light to heavy load variation is also tested; the waveforms of V_K and primary side current are shown in Fig. 12. Transient cost is approximately 30 ms. The time cost is reasonable given the large output capacitance.

According to the low-clock frequency of the selected microcontroller, regulation accuracy is insufficient to reduce the imbalance of the transformer core completely; however, the proposed method can maintain a relatively limited imbalance state. The imbalance direction is controlled to invert every switching cycle in steady state, such that the range of imbalance is limited. The possibility of power device failure is reduced in the PSFB converter because of the limited range. Furthermore, only several external passive devices are introduced compared with the conventional solution, which indicates that the proposed method hardly affects the efficiency of the PSFB converter.

V. CONCLUSION

A high-efficiency and low-cost solution is proposed to suppress transformer core imbalance in PSFB converters. Compared with the common methods, the proposed solution creates an asymmetric control algorithm, which does not accurately balance the transformer core. An approximate control consideration is achieved by a microcontroller, which generates unequal phases in the subsequent cycle according

to the imbalance state in the current cycle. The proposed solution is verified by a 60 V/15 A prototype. Experimental results show that the goal of a balanced transformer core can be achieved. The efficiency of the proposed method is slightly higher than that of the PCM, and the performances of other methods are also tested and compared.

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Juzheng Yu received his B.S. and M.S. degrees in electronics engineering from Southeast University, Nanjing in 2010 and 2013, respectively. He is currently working toward his Ph.D. degree in Southeast University. His research interests include digital control technique, EV/PEV charger, and high-frequency power converter.

Qinsong Qian received his Ph.D. degree in electronics engineering from Southeast University, Nanjing, China in 2012. He joined the School of Electronic Science and Engineering, Southeast University in 2012, where he is currently a lecturer. His research interests include power device design, simulations, and power converter.

Weifeng Sun received his B.S., M.S., and Ph.D. degrees in electronic engineering from Southeast University, Nanjing, China in 2000, 2003, and 2007, respectively. Since 2006, he has been with the School of Electronic Science and Engineering, Southeast University, where he is currently the dean of the School of Electronic Science and Engineering. His research interests include new power device design, power IC, power device model, and power system.

Taizhi Zhang received his B.S. degree in electrical engineering from the Hangzhou Dianzi University, Hangzhou in 2010. He is currently working toward his Ph.D. degree in Southeast University. His research interests include AC–DC, DC–DC, and single-stage PFC converters applied in LED drivers and battery chargers.

Shengli Lu received his Ph.D. degree in information and physics from Nanjing University, Nanjing, China in 1994. Since 1994, he has been with the School of Electronic Science and Engineering, Southeast University, Nanjing, China, where he is currently a professor at the National ASIC System Engineering Research Center. His research interests include VLSI and application-specific integrated circuit.