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Effect of Non-Idealities on the Design and Performance of a DC-DC Buck Converter

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Abstract

In this study, the performance of a direct current (DC)–DC buck converter is analyzed in the presence of non-idealities in passive components and semiconductor devices. The effect of these non-idealities on the various design issues of a DC–DC buck converter is studied. An improved expression for duty cycle is developed to compensate the losses that occur because of the non-idealities. The design equations for inductor and capacitor calculation are modified based on this improved expression. The effect of the variation in capacitor equivalent series resistance (ESR) on output voltage ripple (OVR) is analyzed in detail. It is observed that the value of required capacitance increases with ESR. However, beyond a maximum value of ESR ($r_{c,max}$), the capacitor is unable to maintain OVR within a specified limit. The expression of $r_{c,max}$ is derived in terms of specified OVR and inductor current ripple. Finally, these theoretical studies are validated through MATLAB simulation and experimental results.

Key words: Buck converter, Duty cycle, Equivalent series resistance, Non-idealities, Output voltage ripple

I. INTRODUCTION

Direct current (DC)–DC converters are widely used as power supply in various applications [1]-[4]. Several applications, such as aerospace, military, chemical refineries, and mines, require highly regulated, optimally designed, and compact power supplies. For such applications, an optimum design of inductance and capacitance for buck converter is reported in [5], [6]. In all practical DC–DC converters, power loss occurs because of the internal resistances of inductors, capacitors, and non-ideal switching devices. Most power electronic textbooks and papers have neglected some or all these non-ideal elements while analyzing and designing DC–DC converters [7]-[11]. However, this condition is unacceptable for an accurate and well-designed power supply because these non-idealities affect the desired values of the duty cycle, inductor, and capacitor of a DC–DC converter [12], [13]. For example, the expression for the duty cycle of an ideal buck converter is

$$D = V_o / V_g , \quad (1)$$

where V_o is the output voltage, and V_g is the input voltage.

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However, this relation does not remain valid for a non-ideal buck converter. Owing to the parasitic resistances of inductor, capacitor, diode, and switch, practical DC–DC converters have power losses. Therefore, the actual duty cycle of a non-ideal DC–DC buck converter should be greater than the ideal duty cycle given in Equ. (1) to compensate these losses. An improved expression for this actual duty cycle is derived in this study.

Similarly, the equivalent series resistance (ESR) of an output capacitor plays an important role in the design of capacitors [14]. As the ESR increases, the output voltage ripples (OVR) also increases, thereby reducing the effectiveness of filter capacitors. Moreover, high ESR may lead to instability and increase the power loss in converters [15]. Therefore, arbitrary selection of ESR is inadvisable for a precisely designed DC–DC buck converter. However, the ESR of a capacitor is a parasitic parameter that cannot be avoided by capacitor manufacturers. Nonetheless, power supply designers always prefer a capacitance with low ESR. No analytical solution is available in the literature to evaluate the upper limit of ESR that can be used without exceeding the specified OVR at a particular switching frequency. In this study, a formula for the maximum value of ESR is developed through an in-depth analysis of capacitor voltage ripples to select a capacitor with proper ESR.

The remainder of this paper is organized as follows to

resolve the above-mentioned issues for a buck converter: First, a detailed analysis of a non-ideal buck converter is presented. Second, improved relationships for duty cycle, inductance, and capacitance design are proposed. Third, the analytical expression for maximum allowable ESR for specified OVR is proposed. Finally, MATLAB simulations and experimental results are obtained to confirm these theoretical studies.

II. Analysis of a Non-ideal DC–DC Buck Converter

The power circuit of a non-ideal DC–DC buck converter is shown in Fig. 1. All symbols have a standard meaning, as indicated in Table I. The buck converter is operating in a continuous current conduction mode with duty cycle D and switching frequency f (or switching period T) [7]. The voltage and current equations of the buck converter during the switch-on period ($0 < t \le DT$) and the switch-off period ($DT < t \le T$) are expressed below:

Mode 1: Switch-on ($0 < t \le DT$)

$$v_{L,on}(t) = L\frac{di_L(t)}{dt} = v_g(t) - (r_{sw} + r_L)i_L(t) - v_o(t) \tag{2}$$

$$i_{c,on}(t) = i_L(t) - \frac{v_o(t)}{R} \tag{3}$$

$$v_{o,on}(t) = v_c(t) + r_c i_c(t) \tag{4}$$

Mode 2: Switch-off ($DT < t \le T$)

$$v_{L,off}(t) = L\frac{di_L(t)}{dt} = -(r_d + r_L)i_L(t) - V_F - v_o(t) \tag{5}$$

$$i_{c,off}(t) = i_L(t) - \frac{v_o(t)}{R} \tag{6}$$

$$v_{o,off}(t) = v_c(t) + r_c i_c(t) \tag{7}$$

A. Steady-State Analysis

For steady-state analysis, the time variables are substituted by their respective DC values as [8]

$$i_L(t) = I_L,\ v_g(t) = V_g,\ v_c(t) = V_C\ \ v_o(t) = V_o .$$

According to the principle of inductor volt-second balance, in the steady-state, the average inductor voltage must be equal to zero.

$$V_L = \frac{1}{T}\int_0^T v_L(t)dt = Dv_{L,on}(t) + (1-D)v_{L,off}(t) = 0 \tag{8}$$

Similarly, according to the principle of capacitor charge balance, in the steady-state, the average capacitor current must be equal to zero.

$$I_c = \frac{1}{T}\int_0^T i_c(t)dt = Di_{c,on}(t) + (1-D)i_{c,off}(t) = 0 \tag{9}$$

The average output voltage of the buck converter is

$$V_o = \frac{1}{T}\int_0^T v_o(t)dt = Dv_{o,on}(t) + (1-D)v_{o,off}(t) . \tag{10}$$

By substituting Equs. (2) and (5) into Equ. (8), we obtain

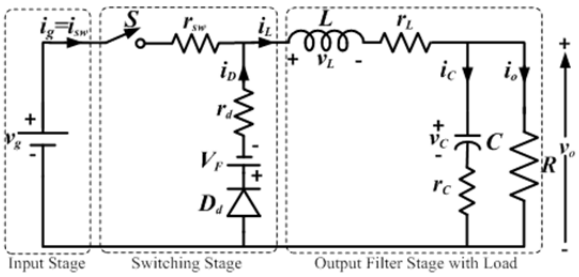


Fig. 1. Non-ideal DC–DC buck converter.

$$DV_g = D'V_F + V_o + (r_L + Dr_{sw} + D'r_d)I_L . \tag{11}$$

Substituting Equs. (3) and (6) into Equ. (9) obtains

$$I_L = \frac{V_o}{R} = I_o . \tag{12}$$

Similarly, substituting Equs. (4), (7), and (9) into Equ. (10) gives

$$V_o = V_C . \tag{13}$$

Replacing Equ. (12) into Equ. (11) provides the relationship for average output voltage as

$$V_o = \frac{DV_g - D'V_F}{1 + \dfrac{(r_L + Dr_{sw} + D'r_d)}{R}}, \tag{14}$$

where $D' = 1 - D$.

Equ. (14) depicts that the output voltage of the buck converter depends on non-idealities and load resistance.

The output voltage variation versus duty cycle plot is shown in Fig. 2 at a constant input voltage and different load resistances. For a particular duty cycle, the non-ideal buck converter produces an output voltage less than that of the ideal buck converter. The output voltage decreases further as the load resistance is decreased. Fig. 3 shows the output voltage variation for different values of input voltages at constant R. For a particular duty cycle, the difference between the output voltage of ideal and non-ideal buck converter becomes larger as input voltage increases. Therefore, the metal oxide semiconductor field-effect transistor (MOSFET) switch should be kept ON for an extended time to achieve the same output voltage in the presence of non-idealities. In other words, the actual duty cycle must be greater than the ideal duty cycle given by Equ. (1).

An improved expression of actual duty cycle is derived by solving Equ. (14) as

$$D = D_{ideal}\frac{1 + \dfrac{r_L}{R} + \dfrac{r_d}{R} + \dfrac{V_F}{V_o}}{1 + \left(\dfrac{r_d - r_{sw}}{R}\right)\dfrac{V_o}{V_g} + \dfrac{V_F}{V_g}}, \tag{15}$$

where $D_{ideal} = V_o/V_g$ is the duty cycle for an ideal buck converter.

The modified duty cycle D in Equ. (15) and the ideal duty cycle D_{ideal} in Equ. (1) are plotted with the desired output voltage (V_o), as shown in Fig. 4. It verifies that the actual duty cycle should be greater than the ideal duty cycle to obtain the

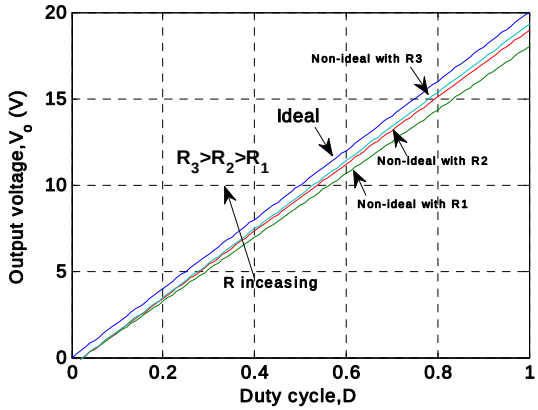


Fig. 2. Output voltage variation with duty cycle at various R and constant V_g.

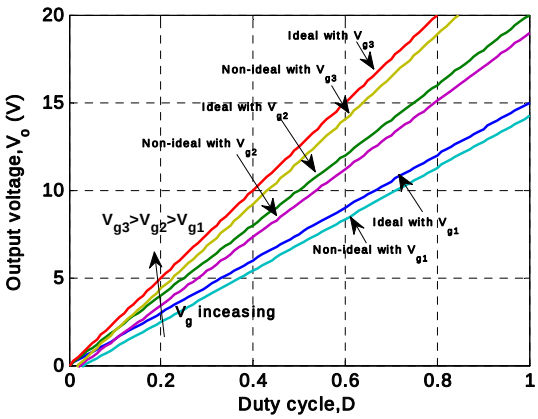


Fig. 3. Output voltage variation with duty cycle at various V_g and constant R.

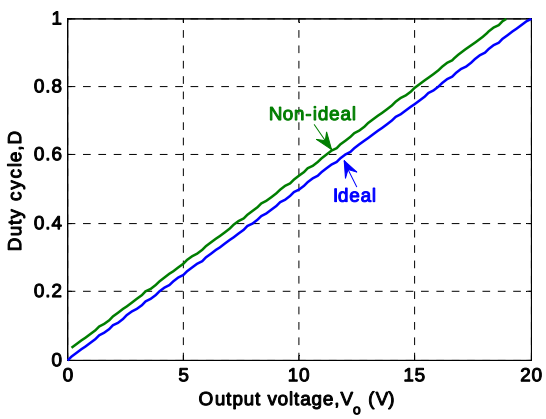


Fig. 4. Duty cycle variation with output voltage.

desired output voltage.

B. Inductor Current Ripple (ICR) and Inductor Design

Let x_L be the ICR factor and Δi_L be the ripple current such that $\Delta i_L = x_L I_L$.

The magnitude of ripple current Δi_L in the steady-state is

$$\Delta i_L = \frac{(r_d + r_L) I_L + V_F + V_o}{L} D'T \,. \tag{16}$$

Substituting I_L from Equ. (12),

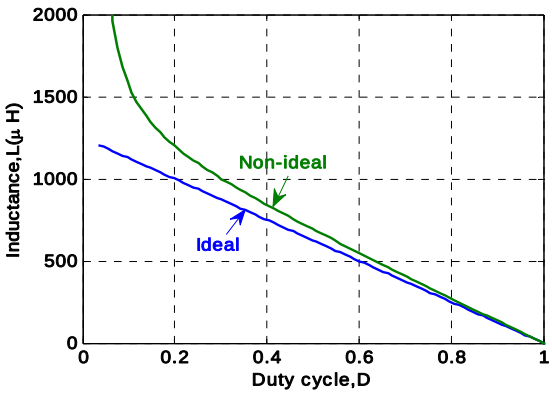


Fig. 5. Inductance variation with duty cycle.

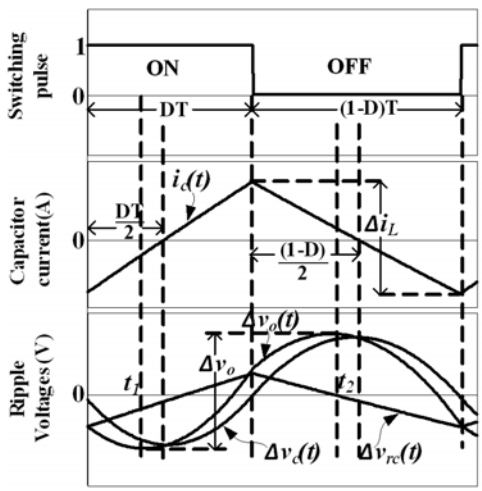


Fig. 6. Capacitor current and voltage ripple waveforms.

$$\Delta i_L = \frac{D'V_o}{Lf}\left(1 + \frac{V_F}{V_o} + \frac{r_L + r_d}{R}\right). \tag{17}$$

Replacing $\Delta i_L = x_L I_L = x_L V_O / R$ and rearranging Equ. (17),

$$L = \frac{(1-D)R}{x_L f}\left(1 + \frac{V_F}{V_o} + \frac{r_d + r_L}{R}\right). \tag{18}$$

Equ. (18) provides the design value of inductance for the desired ICR in terms of converter parameters and non-ideal elements. The required inductance is calculated for ideal and non-ideal buck converters and is plotted with respect to duty cycle in Fig. 5, which depicts clearly that in the non-ideal case, the required inductance value is more than the ideal case. The difference becomes significant at low duty cycles.

C. OVR and Capacitor Design

The capacitor current and voltage ripple waveforms in the steady-state are shown in Fig. 6. If the ESR of output capacitor is considered, then the OVR Δv_o consists of the following two components:

1. Voltage ripple caused by capacitor (Δv_c)
2. Voltage ripple caused by the presence of ESR (Δv_{rc})

Analysis during switch-on ($0 < t \le DT$): The capacitor current dynamics can be given as [16]

$$i_c(t) = \frac{\Delta i_L t}{DT} - \frac{\Delta i_L}{2}. \quad (19)$$

The voltage ripple contribution by the capacitor itself is

$$\Delta v_c(t) = \frac{1}{C}\int_0^t i_c(t)\,dt + \Delta v_c(0) = \frac{\Delta i_L}{2C}\left(\frac{t^2}{DT} - t\right) + \Delta v_c(0), \quad (20)$$

where $\Delta v_c(0)$ is the initial voltage across the capacitor at $t = 0$.

The voltage ripple contribution by the ESR of the capacitor is

$$\Delta v_{rc}(t) = r_c i_c(t) = r_c \Delta i_L\left(\frac{t}{DT} - \frac{1}{2}\right). \quad (21)$$

Therefore, the total voltage ripple during the switch-on period is

$$\Delta v_o(t) = \Delta i_L\left[\frac{t^2}{2CDT} + \left(\frac{r_c}{DT} - \frac{1}{2C}\right)t - \frac{r_c}{2}\right] + \Delta v_c(0). \quad (22)$$

The minimum value of $\Delta v_o(t)$ occurs at time t_1 and is given by

$$t_1 = \frac{DT}{2} - r_c C \text{ and } \Delta v_o(t_1) = -\Delta i_L\left(\frac{DT}{8C} + \frac{r_c^2 C}{2DT}\right) + \Delta v_c(0), \quad (23)$$

$$\Delta v_{rc}(t_1) = -\Delta i_L \frac{r_c^2 C}{DT}, \Delta v_c(t_1) = \Delta i_L\left(-\frac{DT}{8C} + \frac{r_c^2 C}{2DT}\right) + \Delta v_c(0) \quad (24)$$

Analysis during switch-off ($DT < t \le T$): The capacitor current dynamics can be given as

$$i_c(t) = \frac{-\Delta i_L (t - DT)}{D'T} + \frac{\Delta i_L}{2}. \quad (25)$$

The voltage ripple contribution by the capacitor itself is

$$\Delta v_c(t) = \frac{\Delta i_L}{2C}\left(-\frac{(t - DT)^2}{D'T} + (t - DT)\right) + \Delta v_c(DT), \quad (26)$$

where $\Delta v_c(DT)$ is the initial voltage across the capacitor at $t = DT$. In the steady-state, $\Delta v_c(DT) = \Delta v_c(0)$.

The voltage ripple contribution by the ESR of the capacitor is

$$\Delta v_{rc}(t) = r_c i_c(t) = r_c \Delta i_L\left(\frac{-(t - DT)}{D'T} + \frac{1}{2}\right). \quad (27)$$

Therefore, the total voltage ripple during the switch-off period is

$$\Delta v_o(t) = \Delta i_L\left[\frac{-(t - DT)^2}{2CD'T} + \left(\frac{-r_c}{D'T} + \frac{1}{2C}\right)(t - DT) + \frac{r_c}{2}\right] + \Delta v_c(DT) \quad (28)$$

The maximum value of $\Delta v_o(t)$ occurs at time t_2 and is given by

$$t_2 = \frac{(1 + D)T}{2} - r_c C \text{ and } \Delta v_o(t_2) = \Delta i_L\left(\frac{D'T}{8C} + \frac{r_c^2 C}{2D'T}\right) + \Delta v_c(DT), \quad (29)$$

$$\Delta v_{rc}(t_2) = \Delta i_L \frac{r_c^2 C}{(1 - D)T}, \Delta v_c(t_2) = \Delta i_L\left(\frac{D'T}{8C} - \frac{r_c^2 C}{2D'T}\right) + \Delta v_c(DT) \quad (30)$$

1) Voltage Ripples: The total peak-to-peak OVR is

$$\Delta v_o = \Delta v_o(t_2) - \Delta v_o(t_1). \quad (31)$$

Substituting the values from Equs. (23) and (29) into Equ. (31) and simplifying them gives

$$\Delta v_o = \Delta i_L\left(\frac{1}{8fC} + \frac{r_c^2 Cf}{2DD'}\right). \quad (32)$$

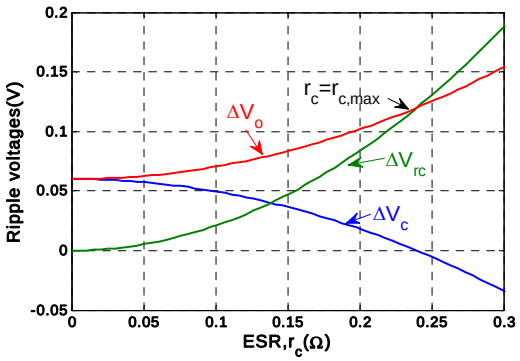


Fig. 7. Variation in voltage ripples with ESR.

Letting $r_c = 0$ gives the OVR for the ideal capacitor as available in the literature.

We can also find the contribution of capacitor voltage ripple and ESR voltage ripple in the peak-to-peak OVR.

The ripple voltage contribution by the capacitor is

$$\Delta v_C = \Delta v_c(t_2) - \Delta v_c(t_1).$$

The ripple voltage contribution by ESR is

$$\Delta v_{rc} = \Delta v_{rc}(t_2) - \Delta v_{rc}(t_1).$$

By substituting the values from Equs. (24) and (30), we have

$$\Delta v_C = \Delta i_L\left(\frac{1}{8fC} - \frac{r_c^2 Cf}{2DD'}\right), \quad (33)$$

$$\Delta v_{rc} = \Delta i_L \frac{r_c^2 Cf}{DD'}. \quad (34)$$

The three voltage ripple variations defined in Equs. (32)-(34) are plotted with respect to ESR, as shown in Fig. 7. From this figure, with an increase in ESR, Δv_{rc} increases at a faster rate than Δv_c decreases, thereby causing a net increase in Δv_o. However, as the value of r_c increases beyond $r_{c,max}$, Δv_{rc} becomes higher than Δv_o, which is practically impossible. This result implies that the capacitor is no longer able to keep OVR within the specified limit for $r_c > r_{c,max}$. The exact relation for this $r_{c,max}$ is derived later.

2) Output Capacitor Design: Let the specified maximum OVR be Δv_{om}. The capacitor is designed such that the following condition must be satisfied:

$$\Delta v_o \le \Delta v_{om}. \quad (35)$$

By substituting Δv_o from Equ. (32) and simplifying it, gives

$$r_c^2 C^2 - \frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_L}\right)C + \frac{DD'}{4f^2} \le 0. \quad (36)$$

Equ. (36) is a quadratic constraint in C. It is solved to generate the minimum value of the capacitor C as

$$C_{\min} = \frac{\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_L}\right) - \sqrt{\left(\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_L}\right)\right)^2 - 4r_c^2\frac{DD'}{4f^2}}}{2r_c^2}. \quad (37)$$

This equation provides the value of minimum capacitance required for $r_c \le r_{c,max}$.

3) Derivation for Maximum Permissible ESR: The additional

term $\frac{r_c^2 Cf\Delta i_L}{2DD'}$ in Equ. (32) appears because of the presence of ESR. As ESR increases, OVR also increases. If the ESR of capacitor is not selected properly, then it may increase the total OVR beyond the maximum permissible value. Therefore, the relationship for the maximum permissible value of ESR for the specified OVR and switching frequency should be determined.

In Equ. (37), $C_{\min}$ must be a real quantity that satisfies the following condition:

$$\left(\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_L}\right)\right)^2 - 4r_c^2\frac{DD'}{4f^2} \geq 0 . \quad (38)$$

On simplifying,

$$r_c \leq 2\sqrt{DD'}\frac{\Delta v_{om}}{\Delta i_L} . \quad (39)$$

Therefore, the maximum permissible value of ESR ($r_{c,\max}$) for specified OVR (Δv_{om})and ICR(Δi_L) is given by

$$r_{c,\max} = 2\sqrt{DD'}\frac{\Delta v_{om}}{\Delta i_L} . \quad (40)$$

If the ESR value is greater than the $r_{c,\max}$ in Equ. (40), then the capacitor will not be able to keep the steady-state OVR in the specified limit. This condition is verified by the experimental results in the subsequent section.

Substituting Equ. (40) into Equ. (37) obtains the minimum value of capacitor at $r_c = r_{c,\max}$ as

$$C_{\min}\big|_{r_C=r_{C,\max}} = \frac{1}{4f}\frac{\Delta i_L}{\Delta v_{om}} . \quad (41)$$

From Equ. (32), for an ideal capacitor ($r_c = 0$), the minimum value of C is

$$C_{\min}\big|_{r_C=0} = \frac{1}{8f}\frac{\Delta i_L}{\Delta v_{om}} . \quad (42)$$

Equ. (41) provides the minimum capacitance required for the worst-case ESR ($r_{c,\max}$). Fig. 8 shows the variation in minimum capacitance value as a function of ESR. The capacitor value increases with an increase in ESR. At $r_c = r_{c,\max}$, the capacitor value becomes double that of with $r_c = 0$. For $r_c > r_{c,\max}$, the capacitance value is a complex value. However, as shown in Fig. 8, MATLAB simulation plots only the real part.

Substituting the values of Δi_L from Equ. (17) into Equ. (40),

$$r_{c,\max} = 2\sqrt{\frac{D}{D'}}\frac{\left(\Delta v_{om}/V_o\right)Lf}{\left(1+\frac{V_F}{V_o}+\frac{r_L+r_d}{R}\right)} . \quad (43)$$

This relation depicts that for specified OVR, the maximum permissible value of ESR ($r_{c,\max}$) is proportional to switching frequency. Therefore, as the switching frequency of the converter increases, the power supply designer is allowed to use a high ESR capacitor without violating the OVR constraint. Fig. 9 shows the variation in $r_{c,\max}$ with frequency. If the switching frequency is 50 kHz, then the designer may use a capacitor with an ESR of 0.6 Ω. As the frequency increases, the required capacitor value decreases.

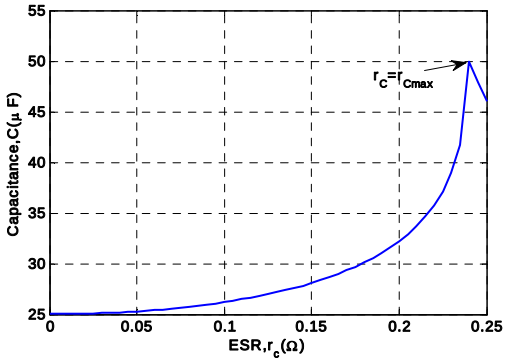


Fig. 8. Value of the minimum capacitance at different ESR.

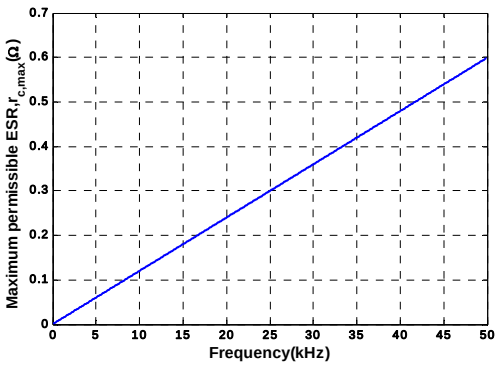


Fig. 9. Maximum permissible ESR ($r_{c,\max}$) vs. frequency.

III. Simulation and Experimental Results

For MATLAB simulation, the buck converter parameters given in Table I are used. For given specifications, according to the relation proposed in Equ. (15), the actual duty cycle is calculated as 0.6415, which is greater than the ideal duty cycle (=0.6). For this actual duty cycle, the inductance value is calculated as 490 μH using Equ. (18). The maximum value of ESR($r_{c,\max}$) and the minimum capacitance ($C_{\min}$) are calculated as 0.2398 Ω and 50 μF, respectively, using Equs. (40) and (41) for the OVR and ICR specified in Table I.

The simulated output voltage for ideal and actual duty cycles is shown in Fig. 10. The results confirm that for ideal duty cycle D = 0.6, the output voltage is 11.2 V; for actual duty cycle D = 0.6415, the output voltage is settled to 12 V (as desired).

We consider four cases for four different values of ESR to investigate the effect of ESR variation on OVR. In each case, the total OVR Δv_o, the ripple caused by capacitor Δv_c and the ripple caused by ESR Δv_{rc} are evaluated and plotted for two switching cycles, as discussed below.

Case 1 ($r_c = 0$): This is the case for an ideal capacitor. However, such a capacitor cannot be obtained in practice. The voltage ripples are shown in Fig. 11(a). The voltage ripple Δv_o is the same as Δv_c. The peak-to-peak OVR is 0.06 V.

Case 2 ($r_c = 0.1\ \Omega < r_{c,\max}$): The voltage ripples are displayed in Fig. 11(b). Owing to the presence of ESR, the total peak-to-peak OVR is increased to 0.07 V. However, this value

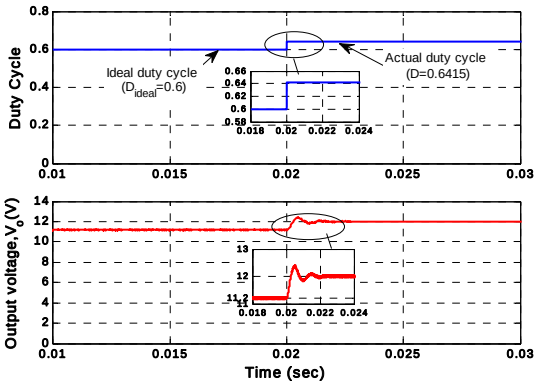


Fig. 10. Simulated output voltage response for ideal and non-ideal duty cycles.

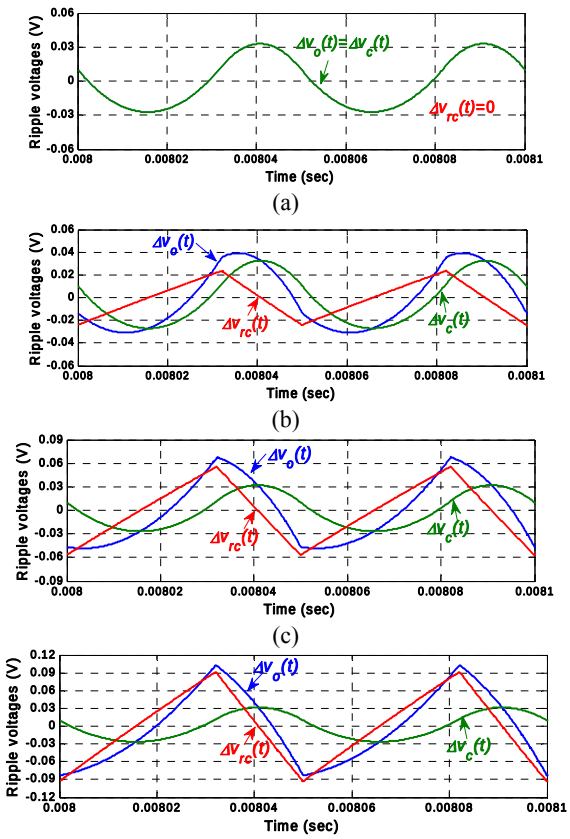


Fig. 11. Simulated voltage ripple waveforms for different ESR values (a) $r_c = 0$, (b) $r_c = 0.1\ \Omega$ ($r_c < r_{c,max}$), (c) $r_c = 0.2398\ \Omega$ ($r_c = r_{c,max}$), and (d) $r_c = 0.4\Omega$ ($r_c > r_{c,max}$).

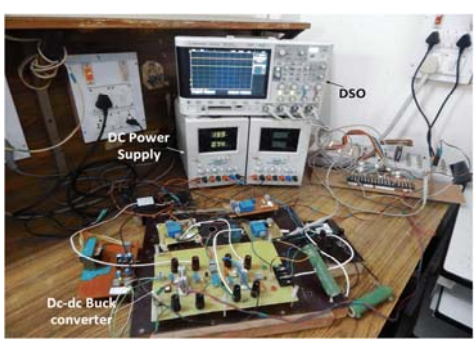


Fig. 12. Experimental setup for the DC–DC buck converter.

TABLE I
BUCK CONVERTER SPECIFICATIONS

Parameter	Value
input voltage, V_g	20 V
output voltage, V_o	12 V
frequency, f	20 kHz
load resistance, R	10 Ω
inductance, L/r_L	490 µH/0.5 Ω
capacitance, C	50 µF
diode forward voltage, V_F	0.5 V
resistance switch/diode (r_{sw}/r_d),	0.05/0.03 Ω
desired ICR, $\Delta i_L/I_L$	0.4
desired OVR, $\Delta v_{om}/V_o$	0.01

TABLE II
KEY COMPONENT LIST

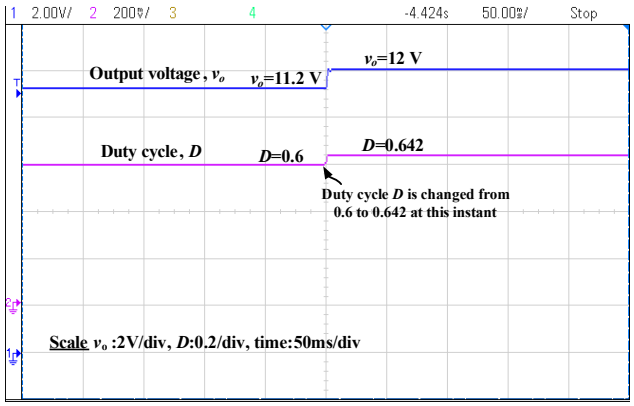
Component Name	Specifications
MOSFET switch	IRF540N
diode	MUR1560
inductor	ferrite core (E-type) with copper winding
capacitor	aluminum electrolytic

is smaller than the maximum allowed OVR (0.12 V).

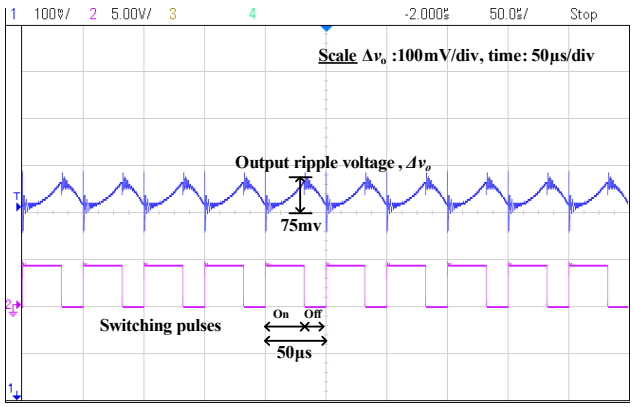
Case 3 ($r_c = r_{c,max} = 0.2398\ \Omega$): The voltage ripples are shown in Fig. 11(c). The ESR voltage ripples increase further, such that the peak-to-peak OVR reaches 0.12 V, which is equal to the maximum allowed OVR.

Case 4 ($r_c = 0.4\ \Omega > r_{c,max}$): As shown in Fig. 11(d), the voltage ripples caused by ESR highly increase. The peak-to-peak OVR is 0.19 V, which is greater than the allowed OVR limit (0.12 V). Thus, the desired performance of the buck converter is degraded.

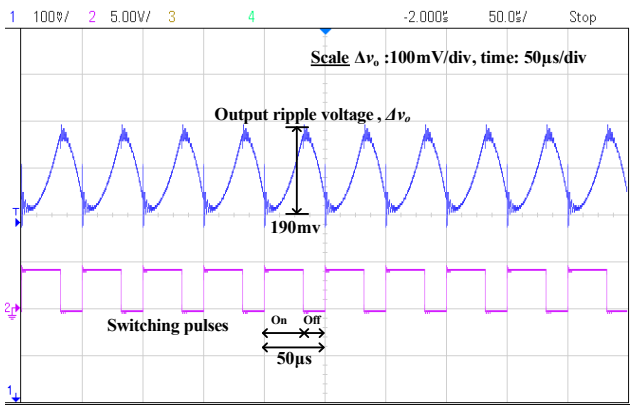
A hardware prototype of buck converter is set up to verify the theoretical studies and simulation results, as shown in Fig. 12. A ferrite core inductor of 490 µH (with 0.5 Ω ESR) and an electrolytic capacitor of 50 µF (with 0.1 Ω ESR) are used. The other key components are listed in Table II. The experimental results are shown in Fig. 13. Fig. 13(a) shows that the output voltage is 11.2 V with a duty cycle of 0.6. If the duty cycle is maintained at 0.642, as obtained from the proposed formula in Equ. (15), then the output voltage is 12 V. Figs. 13(b) and 13(c) show the OVR for $r_c < r_{c,max}$ and $r_c > r_{c,max}$, respectively. For $r_c = 0.1\ \Omega$, the OVR is 75 mV, which is within the maximum specified limit (120 mV). For $r_c = 0.4\ \Omega$, the OVR is 190 mV, as shown in Fig. 13(c). This value is greater than the maximum specified limit (120 mV). Therefore, the experimental results validate the theoretical and simulation results. The dependency of OVR on switching frequency is also experimentally validated for different values of the capacitor ESR. Fig. 14(a) shows that with $r_c = 0.1\ \Omega$, the OVR is less than 0.12 V for a frequency greater than 20 kHz. Fig.



(a)



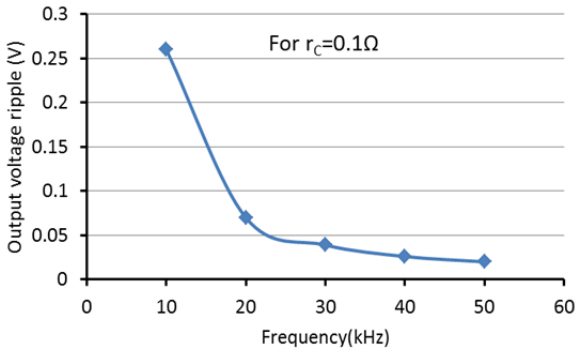
(b)



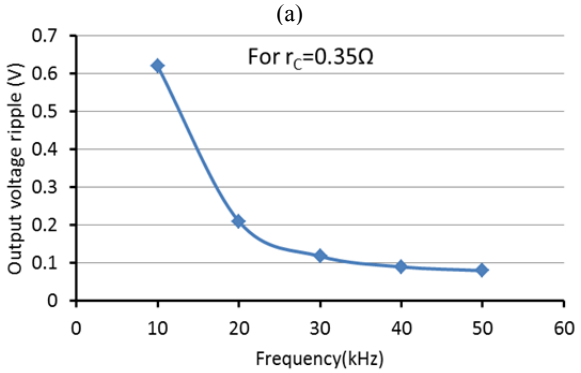
(c)

Fig. 13. Experimental results: (a) output voltage response with ideal and proposed duty cycles, (b) OVR with r_c = 0.1 Ω, and (c) OVR with r_c = 0.4 Ω.

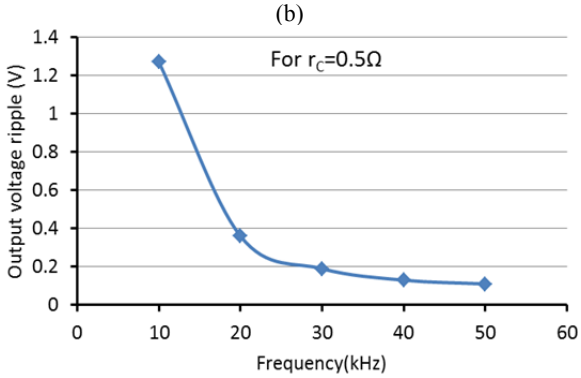
14(b) shows that with r_c = 0.35 Ω, the OVR is within the specified limit for a frequency above 30 kHz. Similarly, Fig. 14(c) depicts that if the converter operates at a switching frequency greater than or equal to 50 kHz, then the OVR is within the desired limit even with a large ESR value of 0.5 Ω. Hence, if the converter operates at a higher frequency, the OVR may remain within the specified limit even with a higher ESR value. The OVR depends on ESR and converter frequency in an opposite manner.



(a)



(b)



(c)

Fig. 14 Experimental results of output voltage variation with frequency with (a) r_c = 0.1 Ω, (b) r_c = 0.35 Ω, and (c) r_c = 0.5 Ω.

IV. Conclusion

In this study, the duty cycle formula for a non-ideal DC–DC buck converter is improved considering parasitic elements. The effect of these parasitics on inductor and capacitor designs is analyzed. Analyses show a significant difference in inductor and capacitance values with the inclusion of non-ideal components. The ESR of output capacitor contributes significant ripples to output voltage. For specified OVR and switching frequency, the maximum allowable value of this ESR is derived. The simulation and experimental results indicate that an ESR beyond this maximum value results in unwanted OVR. Therefore, this analysis may be interesting and useful for a power electronic engineer to design a high-precision power supply. The proposed analysis, with suitable modifications, can be generalized to design other types of DC–DC converters.

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