JPE 16-3-8

http://dx.doi.org/10.6113/JPE.2016.16.3.894 ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Analysis, Design, and Implementation of a Soft-Switched Active-Clamped Forward Converter with a Current-Doubler Rectifier

Paul Jang[†], Hye-Jin Kim^{*}, and Bo-Hyung Cho^{*}

^{†,*}Department of Electrical and Computer Engineering, Seoul National University, Seoul, Korea

Abstract

This study examines the zero-voltage switching (ZVS) operation of an active-clamped forward converter (ACFC) with a current-doubler rectifier (CDR). The ZVS condition can be obtained with a much smaller leakage inductance compared to that of a conventional ACFC. Due to the significantly reduced leakage inductance, the design is optimized and the circulating loss is reduced. The operation of the ACFC with a CDR is analyzed, and a detailed ZVS analysis is conducted on the basis of a steady-state analysis. From the results, a design consideration for ZVS improvement is presented. Loss analyses of the converters shows that enhanced soft-switching contributes to an efficiency improvement under light-load condition. Experimental results from a 100-W (5-V/20-A) prototype verify that the ACFC with a CDR can attain ZVS across an extended load range of loads and achieve a higher efficiency than conventional ACFCs.

Key words: Active-clamp circuit, Current-doubler rectifier, Forward converter, Zero-voltage switching

I. Introduction

The forward converter has been one of the most extensively used topologies in low- and medium-power DC-DC converter applications (e.g., computer and telecommunication systems) because of its simple circuitry, low cost, and high efficiency. However, several issues remain such as high-voltage spikes across the MOSFET and resetting of the transformer. To solve these problems, forward converters have used several reset schemes. An active-clamp circuit is the most widely used scheme because it does not require an additional reset winding or energy dissipative component to minimize the voltage stress across the MOSFET [1]-[7]. In addition, an active-clamp circuit enables zero-voltage switching (ZVS) in a MOSFET.

In a conventional active-clamped forward converter (ACFC), the main switch can achieve ZVS by harnessing either the magnetizing inductance [8]-[10] or the leakage inductance [12]-[14]. The method of magnetizing inductance requires a gap in the transformer that increases the magnetizing current,

Manuscript received Aug. 25, 2015; accepted Jan. 1, 2016 Recommended for publication by Associate Editor Chun-An Cheng. †Corresponding Author: paul716@snu.ac.kr

Tel: +82-880-1785, Fax: +82-878-1452, Seoul National University Department of Electrical and Computer Engineering, Seoul National University, Korea

discharging the output capacitor of the MOSFET and resulting in ZVS. However, a hard-switching operation is employed rather than a soft-switching one when a decreased switching loss cannot compensate for the increased conduction loss [10]. Consequently, this method is only suitable for converters with a small input current and a high-input voltage [11]. The method of the leakage inductance uses the resonance between the leakage inductance and the output capacitor of the MOSFET to discharge the stored energy. The ZVS condition is more easily met as the leakage inductance increases. However, large duty cycle losses result in an overall decrease in efficiency. Several methods have been proposed to improve the ZVS operation while using a relatively large magnetizing inductance and a small leakage inductance [15]-[17]. However, these methods either require additional components [15], [16] or only apply to ACFCs with an externally driven synchronous rectifier on the secondary side [17].

In order to overcome these limitations, this paper proposes an ACFC with a CDR to improve ZVS operation. CDR is widely used in applications with low-output voltage and high-output current because the root-mean-square (RMS) current on the transformer secondary is small and the output voltage ripple is reduced [18]-[20]. Many previous studies have reported on the general advantages of CDR-based topologies

[21]-[25]. It has also been reported that CDR improves ZVS operation when used with a phase-shifted full-bridge converter [26], [27]. However, for a phase shifted full bridge converter, the primary current should decay rapidly during the zero state [27], and the output inductor current should become negative at the switching instant for ZVS improvement, which compromises the general advantages of CDR. While an ACFC with a CDR can inherently use the output inductor energy to improve ZVS operation, it has never been remarked before. Hence, an excessive resonant inductor has been used [12] or ZVS has been reported with only empirical results [21], [28]-[30].

Therefore, the present study rigorously analyzes an ACFC with a CDR to achieve enhanced ZVS operation. This paper demonstrates that an ACFC with a CDR improves the ZVS performance and presents a design consideration for further improvements. A quantitative comparison of the losses in an ACFC with a CDR and those in other ACFCs verifies that the enhanced ZVS performance is responsible for the improvement in light-load efficiency. The experimental results also show that enhanced soft-switching contributes to improvement in efficiency under light-load. Therefore, an ACFC with a CDR exhibits a high efficiency across all load conditions.

Despite its advantages, the proposed converter needs an additional output inductor. If discrete magnetic components are used, three cores are required: one for the transformer and two for the output inductors. These can increase the cost and size of the converter. However, since previous studies [31]-[34] have reported that the three cores can be replaced by integrated magnetic structures, the present study focuses on the aspect of CDR efficiency.

The paper is structured as follows: Section II describes the circuit configuration of the ACFC with a CDR. Section III presents a ZVS analysis based on a steady-state analysis, and provides design considerations for ZVS improvement. Section IV presents a loss analysis to verify the role of the enhanced ZVS performance in improving efficiency. Section V experimentally verifies the assertions of Section IV using a 100-W (5-V/20-A) prototype, and Section VI concludes the paper.

II. CIRCUIT CONFIGURATION

The circuit configurations of the conventional ACFC and an ACFC with a CDR are shown in Figs. 1(a) and 1(b), respectively. Unlike the conventional ACFC, R_{L1} , R_{L2} , and R_t which are the equivalent series resistances (ESR) of L_1 , L_2 , and the transformer, are considered in Fig. 1(b) for the ZVS analysis as explained later. The auxiliary switch S_2 and the clamp capacitor C_c are components of the active-clamp circuit and recycle leakage energy. The transformer is modeled with a magnetizing inductance L_m and an equivalent leakage inductance reflected on the primary side L_{lk} . The

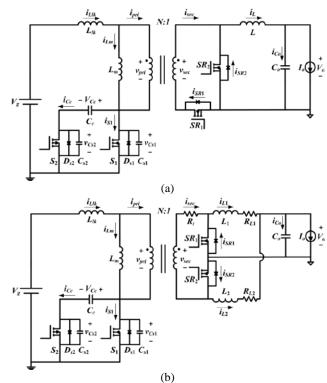


Fig. 1. Circuit configuration. (a) Conventional ACFC. (b) ACFC with CDR.

main switch S_1 is operated with the duty cycle D, and the auxiliary switch S_2 is operated complementarily to the duty cycle of S_1 , with dead times preceding and following the auxiliary switch action. Both of the switches include body diodes D_{s1} and D_{s2} , and output capacitors C_{s1} and C_{s2} . The secondary side comprises two synchronous switches SR_1 and SR_2 , two output inductors L_1 and L_2 , and an output capacitor C_o .

Active-clamp circuitry can be applied to either the high side or the low side. High-side clamps are applied across the primary side of the transformer and use an N-channel auxiliary switch on the clamp network. Hence, they are appropriate for high-input-voltage applications. However, additional high-side gate circuitry is needed to drive the auxiliary switch. A low-side clamp is applied across the drain-to-source of the main switch and a P-channel auxiliary switch is used on the clamp network. The drain-to-source voltage rating of the P-channel switch is lower than that of the N-channel switch and it cannot be used for off-line applications. However, it does not require any additional gate drive circuitry and improves the precision of the control over the delay timing for ZVS.

The level of the input voltage in most forward converter applications is lower than the line voltage. Therefore, the low-side clamp is adopted in this paper. The fundamental principles are exactly the same for both clamps. As a result, the following analyses can also be applied to high-side clamps.

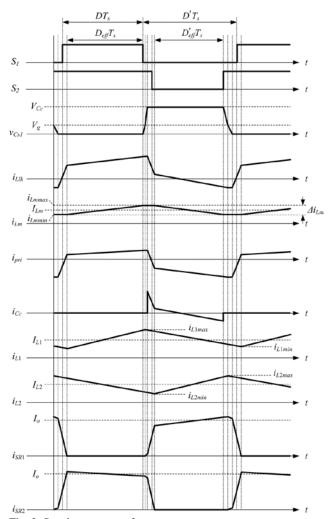


Fig. 2. Steady-state waveforms.

III. ZVS ANALYSIS

ZVS operation of S_2 is guaranteed regardless of load variations [15] and does not need to be considered separately in the design consideration. Consequently, the ZVS analysis of S_1 is conducted in the following.

A. Steady-state analysis

Steady-state waveforms of the ACFC with a CDR are shown in Fig. 2. The operation modes and analyses are complicated by the resonant operation. The circuit operation and ZVS analysis are simplified by the following assumptions:

- 1) The dead times are much shorter than the switch turn-on times and are negligible.
- 2) L_{lk} is much less than L_m .
- 3) C_c is large enough to make the clamp voltage

Since these assumptions make scarcely any changes in the minimum value of $i_{Llk}(t)$, which is the most significant value for the ZVS analysis, they simplify the analysis without

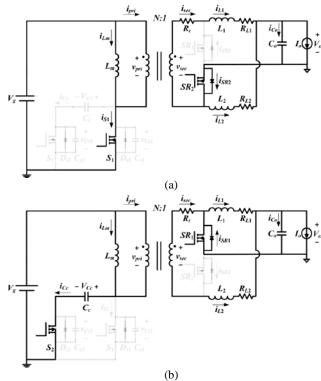


Fig. 3. The two operation states to calculate steady-state DC average values. (a) State 1: S_1 is on. (b) State 2: S_2 is on.

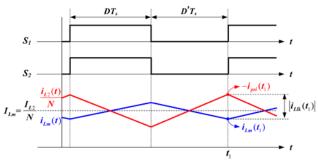


Fig. 4. Approximated steady-state waveforms.

introducing any inaccuracies.

When the above conditions are applied, the total number of intervals in one switching cycle decreases from ten to two and D becomes equal to the effective duty $D_{\it eff}$. Equivalent circuits for these two states are depicted in Fig. 3. The steady-state waveforms of the converter are shown in Fig. 4.

To ensure the ZVS of S_1 , the energy stored in L_{lk} must be larger than the energy stored in C_{s1} at the moment the switch is turned on, t_1 . L_{lk} and $i_{Llk}(t_1)$ are critical determinants of the ZVS of S_1 . ZVS is more easily achieved when both determinants increase. Large values of L_{lk} degrade the converter efficiency and affect the voltage conversion ratio of the forward converter. Therefore, it is more desirable to increase $i_{Ilk}(t_1)$.

In the conventional ACFC, the leakage current $i_{Llk}(t)$ is equal to the magnetizing current $i_{Lm}(t)$, and it discharges C_{s1} at t_1 , as shown in Fig. 5(a). The ZVS operation of S_1 is not

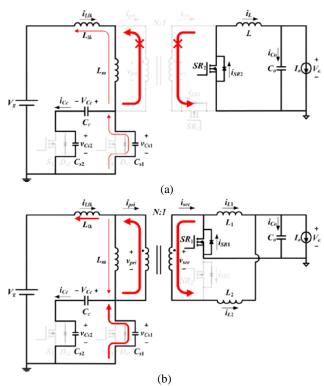


Fig. 5. Current flow of transformer and C_{s1} at t_1 . (a) Conventional ACFC. (b) ACFC with CDR.

easily achieved with a small leakage inductance because the magnitude of $i_{Llk}(t_1)$ is not large enough to totally discharge C_{s1} .

Meanwhile, the transformer-secondary current $i_{sec}(t)$ can flow bidirectionally on the ACFC with a CDR. In this case, $i_{Llk}(t)$ is not equal to $i_{Lm}(t)$. It is determined from the sum of $i_{Lm}(t)$ and the transformer-primary current $i_{pri}(t)$ at t_1 , as shown in Fig. 5(b). The increment of $i_{pri}(t_1)$, reflected from $i_{L2}(t_1)$, can contribute to the ZVS of S_1 . The steady-state and ripple values of $i_{Lm}(t)$ and $i_{pri}(t)$ must be obtained to investigate how enhanced ZVS operation occurs in the proposed converter. The steady-state values of $i_{Lm}(t)$, $i_{L1}(t)$, $i_{L2}(t)$, and $v_{Cc}(t)$ can be obtained by solving the state-space equations (The detailed derivation is provided in the Appendix). The results are as follows [22]:

$$I_{Lm} = \frac{R_{L1} + DR_t}{R_{L1} + R_{L2} + R_t} \frac{I_o}{N} \tag{1}$$

$$I_{L1} = \frac{R_{L2} + D'R_t}{R_{L1} + R_{L2} + R_t} I_o$$
 (2)

$$I_{L2} = \frac{R_{L1} + DR_t}{R_{L1} + R_{L2} + R_t} I_o \tag{3}$$

$$V_{Cc} = \frac{1}{D} V_g \,. \tag{4}$$

From Eqs. (1) and (3), it can be seen that I_{Lm} multiplied by the transformer turn ratio N is equal to I_{L2} This is due to the charge balance on C_c . Therefore, $i_{L/k}(t_1)$ is determined

by the ripple current of $i_{Lm}(t)$ and $i_{L2}(t)$. The absolute value of $i_{Lik}(t_1)$ is given by:

$$\left| i_{Llk}(t_1) \right| = \frac{\left(\frac{V_{Cc} - V_g}{N} - V_o - V_{SR} \right) D'T_s}{2L_2 N} + \frac{\left(V_{Cc} - V_g \right) D'T_s}{2L_m}$$
 (5)

where V_{SR} stands for the sum of the voltage drops across the ESRs and synchronous switches.

In the case of the conventional ACFC, $|i_{Llk}(t_1)^*|$, which corresponds to $|i_{Llk}(t_1)|$, can be written as follow [3]:

$$\left|i_{Llk}(t_1)^*\right| = \frac{E_{lk} - E_{cs}}{\left(V_{Cc} - V_g\right)DT_s} + \frac{\left(V_{Cc} - V_g\right)DT_s}{2L_m},$$
 (6)

where

$$E_{Cs} = \frac{1}{2} \left(C_{s1} + C_{s2} \right) \left(\frac{D}{D} V_g \right)^2 \text{ and } E_{Llk} = \frac{1}{2} L_{lk} \left(\frac{I_o}{N} \right)^2.$$
 (7)

B. ZVS advantageous area

For improved ZVS operation in the ACFC with a CDR relative to the conventional ACFC, $|i_{Llk}(t_1)|$ has to be larger than $|i_{Llk}(t_1)^*|$. If it is assumed that $E_{Cs} = 0$ for the worst case design and neglect V_{SR} in Eq. (5), the ZVS condition for the extended load range can be described as follow:

$$\frac{D^{3}V_{g}^{2}T_{s}^{2}}{L_{2}I_{o}^{2}} \ge L_{lk}.$$
 (8)

When the condition in Eq. (8) is met, the ACFC with a CDR shows enhanced ZVS characteristics when compared with the conventional ACFC. From the small values of L_{lk} , the duty cycle loss is reduced and the design of a forward converter becomes convenient. If the condition in Eq. (8) can be easily satisfied, the ACFC with a CDR represents an appropriate substitute for the conventional ACFC.

The advantageous ZVS conditions for the ACFC with a CDR and the conventional ACFC are investigated according to Eq. (8) using the converter system specifications given in Table I. The results for both converters are given in Fig. 6. The boundary condition line separates the region where the ACFC with a CDR most easily achieves ZVS from the corresponding region for the conventional ACFC. The ACFC with a CDR attains ZVS with a smaller leakage inductance than the conventional ACFC. Moreover, the difference between the minimum inductances for each converter increases as the load decreases.

C. ZVS condition for the ACFC with a CDR

The main switch ZVS condition for the ACFC with a CDR is given by the following:

$$\frac{1}{2}L_{lk}(i_{Llk}(t_1))^2 \ge \frac{1}{2}(C_{s1} + C_{s2})V_{g \max}^2.$$
 (9)

where $V_{\rm g\; max}$ is maximum input voltage.

Using Eqs. (4) and (5) while assuming that V_{SR} is negligible, Eq. (9) can be arranged as:

TABLE I
SYSTEM SPECIFICATION

Input voltage (V_g)	48 V
Output voltage (V_o)	5 V
Rated output current $(I_{o(rate)})$	20A
Switching frequency (f_{sw})	500kHz

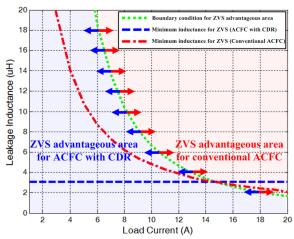


Fig. 6. ZVS advantageous condition.

$$L_{lk} \ge \frac{C_{eq}}{(D_{\min}L_m + L_2N^2)^2} \left(\frac{2L_2L_mN^2}{D_{\min}T_s}\right)^2 . \tag{10}$$

where D_{\min} is the minimum duty ratio.

Unlike the conventional ACFC, the leakage inductor for ZVS is not load dependent for the ACFC with a CDR. A leakage inductor that meets the condition in Eq. (10) guarantees the ZVS condition across the entire range of loads. Furthermore, the ACFC with a CDR can achieve ZVS while keeping L_{lk} much lower than L_m if the output inductor is properly designed. The leakage inductance for ZVS is shown in Fig. 7 under the following conditions: L_m varies from 0 to 400 μ H, L_2 varies from 0.5 to 2 μ H, and V_g is fixed at 48 V. The optimal design conditions can be easily identified from Fig. 7.

IV. Loss Analysis

To verify that the enhanced ZVS performance was responsible for the improved efficiency, a loss analysis was conducted. The ACFC with a CDR was designed according to the system specifications in Table I, and the results are shown in Table II. For the conventional ACFC, the design specifications are the same as those of the ACFC with a CDR, except that a 1- μ H output inductor was used in the conventional ACFC.

The loss factors considered in this analysis are as follows: 1) the conduction loss in the FETs and ESRs (P_{cond}); 2) the switching loss in the FETs (P_{sw}); and 3) the transformer core

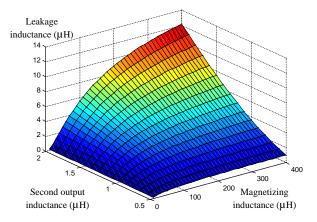


Fig. 7. Leakage inductance for ZVS operating ACFC with CDR.

TABLE II
DESIGN RESULTS OF THE ACFC WITH CDR

Clamp capacitor (C_c)	47nF
Output capacitor (C_o)	47μF
Output Inductor $(L_1 \& L_2)$	1μΗ
ESR of Output Inductor (R_{L1} & R_{L2})	$2 \mathrm{m} \Omega$
ESR of Transformer-Secondary (R_t)	$10 \mathrm{m}\Omega$
Transformer turn ratio (N)	4:1
Magnetizing inductance (L_m)	200μΗ
Leakage inductance (L_{lk})	3μΗ
Main switch (S_1)	STP30NF20
Auxiliary switch (S ₂)	FQP12P20
Synchronous Switches $(SR_1 \& SR_2)$	IPP040N06N

loss (P_{core}). Numerical expressions for each of the loss factors are derived below.

First, the conduction loss is calculated from the resistance and RMS current through each resistor. The conduction loss is expressed as:

$$P_{cond} = R_{dson(S_1)} i_{rms(S_1)}^2 + R_{dson(S_2)} i_{rms(S_2)}^2 + R_{dson(SR_1)} i_{rms(SR_1)}^2 + R_{dson(SR_2)} i_{rms(SR_2)}^2 .$$

$$+ \sum_{i} R_{ESR_i} i_{rms(ESR_i)}^2$$
(11)

Next, the switching loss is estimated from the output capacitor loss and power loss during the switching transition period. The switching loss can be expressed as:

$$P_{sw} = \sum_{i} P_{sw(S_i)} + \sum_{i} P_{sw(SR_i)}$$
 (12)

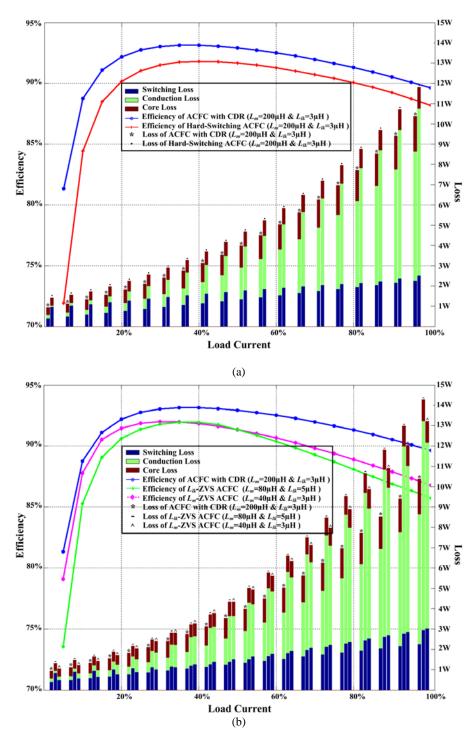


Fig. 8. Comparison of estimated efficiency and loss components. (a) ACFC with CDR and hard-switching ACFC. (b) ACFC with CDR and soft-switching ACFCs.

$$P_{sw(S_i)} = \frac{1}{2} C_{s_i} V_{s_i}^2 + \frac{1}{2} V_i I_i \left(t_{on} + t_{off} \right) f_{sw}$$
 (13)

$$P_{sw(SR_i)} = \frac{1}{2} V_i I_i t_{off} f_{sw}$$
 (14)

where V_i and I_i are the switch voltage and current, and t_{on} and t_{off} are the turn-on and turn-off switching periods of the corresponding power MOSFET, respectively. In the case of synchronous switches, only the turn-off losses are accounted

for because they always attain ZVS by the load current and turn-on losses are negligible.

Finally, the core loss is given by

$$P_{core} = \rho_m V_e K_c f_{sw}^{\alpha} B_m^{\beta} \tag{15}$$

where ρ_m , V_e , and B_m are the core material density, the core volume, and the maximum flux density, respectively. K_c , α , and β are constants that can be determined by fitting the core data provided by the manufacturer [35].

The total efficiency and loss component are calculated for the four converters:

- 1) ACFC with a CDR ($L_m = 200 \, \mu \text{H \& } L_{lk} = 3 \, \mu \text{H}$).
- 2) Hard switching ACFC ($L_m = 200 \, \mu\text{H} \, \& \, L_{lk} = 3 \, \mu\text{H}$).
- 3) L_{lk} -ZVS ACFC ($L_m = 80 \mu H \& L_{lk} = 5 \mu H$).
- 4) L_m -ZVS ACFC ($L_m = 40 \mu H \& L_{lk} = 3 \mu H$).

All of the device parameters needed in the loss calculation are obtained from the datasheet provided by the manufacturer. The results of the loss analysis are shown in Fig. 8.

In Fig. 8(a), the estimated efficiency and loss components of the ACFC with a CDR and the hard-switching ACFC are presented. The ACFC with a CDR has the lowest switching loss due to its outstanding ZVS characteristics. It exhibits a higher efficiency than the hard-switching ACFC at light-load conditions, when switching losses dominate. Due to its small RMS current on the secondary, the ACFC with a CDR also exhibits a higher efficiency in the heavy-load range. Therefore, the ACFC with a CDR achieves a high efficiency when compared to the hard-switching ACFC throughout the whole load.

In Fig. 8(b), a comparison of the ACFC with a CDR and two soft-switching ACFCs is presented. The L_{lk} -ZVS ACFC has the advantage of soft-switching due to its large leakage inductance, thereby attains ZVS from medium-load conditions. However, the duty cycle loss and auxiliary switch turn-off loss increase with the load. Consequently, the L_{lk} -ZVS ACFC exhibits the worst heavy-load efficiency of all of the converters. The L_m -ZVS ACFC achieves soft-switching due to its reduced L_m and it shows a high efficiency at light-load conditions. However, the heavy-load efficiency is worse than the ACFC with a CDR because of the increased conduction loss on the primary side.

The loss analysis shows that the ACFC with a CDR exhibits the most outstanding ZVS performance. The light-load efficiency is expected to improve with soft-switching. At heavy loads, the advantages of a small RMS current on the secondary contribute to a high efficiency. The two soft-switching ACFCs also show high efficiency at light-loads. However, heavy-load efficiency get worse because of the duty cycle loss, switch turn-off loss and primary side conduction loss.

V. EXPERIMENTAL RESULTS

The improved efficiency of the ACFC with a CDR was experimentally verified. Prototypes of the ACFC with a CDR $(L_m=200~\mu\text{H \& }L_{lk}=3~\mu\text{H})$, a hard-switching ACFC $(L_m=200~\mu\text{H \& }L_{lk}=3~\mu\text{H})$, a L_{lk} -ZVS ACFC $(L_m=80~\mu\text{H \& }L_{lk}=5~\mu\text{H})$, and a L_m -ZVS ACFC $(L_m=40~\mu\text{H \& }L_{lk}=3~\mu\text{H})$ were built and tested.

The waveforms for the leakage inductor current (i_{Llk}) , transformer secondary current (i_{sec}) , magnetizing inductor current (i_{Lm}) , and two output inductor currents $(i_{L1}$ and $i_{L2})$ are

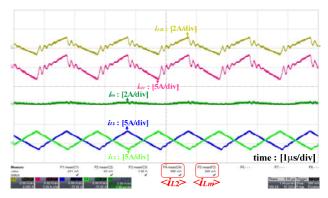


Fig. 9. Current waveforms of the ACFC with CDR at 10% load condition.

shown in Fig. 9 for the ACFC with a CDR at a 10% load. The function for i_{Lm} is calculated from i_{Llk} and i_{sec} divided by the transformer turn ratio. As seen in Fig. 9, the average $\langle i_{Lm} \rangle$ is 226 mA, whereas the average $\langle i_{L2} \rangle$ is 982 mA. This is nearly N times larger than $\langle i_{Lm} \rangle$. Therefore, $i_{Llk}(t_1)$ is determined by the ripple current of i_{Lm} and i_{L2} , as shown in Fig. 4.

Waveforms for the drain-to-source voltage of S_1 (V_{ds1}), the gate-to-source voltage of S_1 (V_{gs1}), the gate-to-source voltage of S_2 (V_{gs2}), and the leakage inductor current (i_{Llk}) are shown in Fig. 10 for the ACFC with a CDR. V_{ds1} is zero before S_1 is turned on, which confirms the ZVS of S_1 with a low electromagnetic interference (EMI) despite a small leakage inductance under all load conditions. The primary conduction loss is greater than that of the conventional ACFC because of the increased $i_{pri}(t_1)$. Nevertheless, a decrease in the primary-switching loss compensates for the increased primary conduction loss. As a result, the efficiency of the ACFC with a CDR is higher than that of the hard-switching converter at light load.

Waveforms for the hard-switching ACFC at a 10% load are shown in Fig. 11(a). When S_1 is turned on, a hard-switching operation is observed with EMI noise before V_{ds1} becomes zero. This diminishes the light-load efficiency of the hard-switching ACFC, as seen in Fig. 14(a). Waveforms of the hard-switching ACFC at 50% and 100% load are shown in Fig. 11(b) and Fig. 11(c), respectively. At the 100% load condition, S_1 almost achieves ZVS due to the increased load current. However, the ACFC with a CDR still shows a high efficiency.

Waveforms for the L_{lk} -ZVS ACFC at a 10% load are shown in Fig. 12 (a). Due to its large leakage inductance, hard-switching operation is observed with less EMI noise below 50% load condition. From a 50% load, S_1 almost achieves ZVS as seen in Fig. 12(b). However, an increased duty cycle loss is observed at the heavy load condition, which deteriorates the efficiency.

Waveforms for the L_m -ZVS ACFC are shown in Fig. 13. Due to its reduced magnetizing inductance, soft-switching operation is observed with less EMI noise under all load

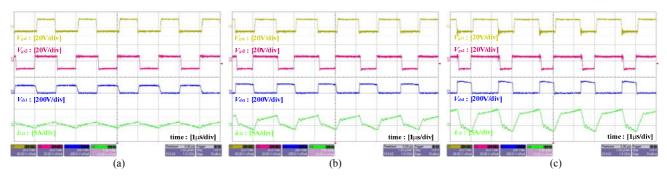


Fig. 10. Waveforms of the ACFC with CDR ($L_m = 200 \,\mu\text{H} \& L_{lk} = 3 \,\mu\text{H}$). (a) 10% load. (b) 50% load. (c) 100% load.

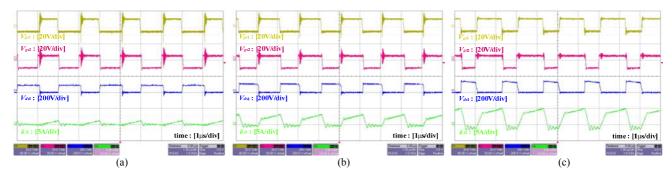


Fig. 11. Waveforms of conventional ACFC ($L_m = 200 \,\mu\text{H} \,\&\, L_{lk} = 3 \,\mu\text{H}$). (a) 10% load. (b) 50% load. (c) 100% load.

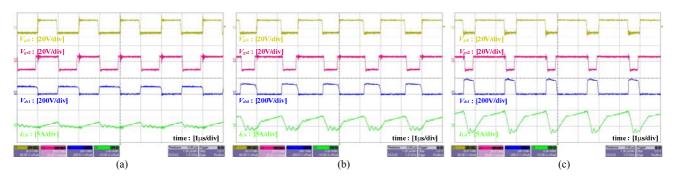


Fig. 12. Waveforms of L_{lk} –ZVS ACFC (L_m = 80 μ H & L_{lk} = 5 μ H). (a) 10% load. (b) 50% load. (c) 100% load.

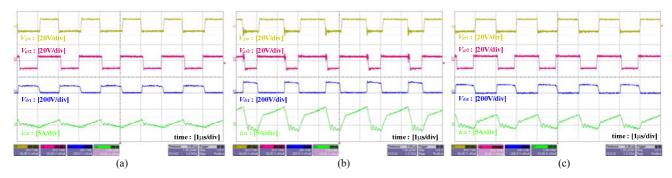


Fig. 13. Waveforms of L_m –ZVS ACFC (L_m = 40 μ H & L_{lk} = 3 μ H). (a) 10% load. (b) 50% load. (c) 100% load.

conditions. However, an enlarged primary current is observed relative to the other ACFCs. This decreases efficiency at heavy-load.

In conclusion, the ACFC with a CDR achieves ZVS of S_1 more easily than the conventional ACFC, even with a small leakage inductance. Improvements in efficiency are most

evident in the light-load conditions, especially, when the switching loss is the dominant factor in the total loss. The conventional ACFC is also able to perform ZVS with an increased resonant inductance or a reduced magnetizing inductance. However, its heavy-load efficiency is worsened by its large duty cycle loss, auxiliary switch turn-off loss and

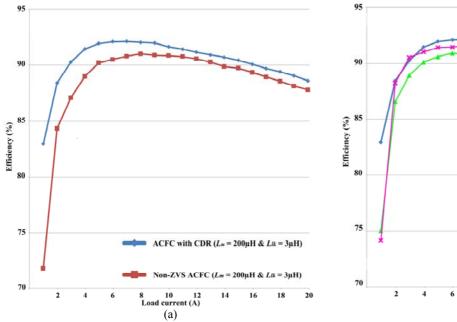


Fig. 14. Efficiency measurement. (a) ACFC with CDR and hard-switching ACFC. (b) ACFC with CDR and soft-switching ACFCs

primary side conduction loss. Consequently, the ACFC with a CDR has a higher efficiency with less EMI noise than the other ACFCs for all load conditions (see Fig. 14).

VI. CONCLUSIONS

In this paper, the ZVS operation of an ACFC with a CDR is studied. Placing the CDR in the transformer secondary, the ZVS condition can be obtained with a much smaller leakage inductance compared to the conventional ACFC. A detailed ZVS analysis is conducted on the basis of a steady-state analysis. The design consideration for ZVS improvement is presented. A loss analysis of the converter shows that the enhanced ZVS performance contributes to improved efficiency under light-load conditions. Experimental results with a 100-W (5-V/20-A) prototype verified that the ACFC with a CDR can attain ZVS of the main switch more efficiently in spite of a small leakage inductance and that it can achieve a high efficiency compared to other ACFCs throughout the whole load range.

APPENDIX

In this appendix, state-space equations of Fig. 3 are described. By solving these equations, (1)-(4) can be obtained.

As shown in Fig. 3, there are two operation modes. In each subinterval, the converter can be denoted by following

equation:

$$\dot{x} = A_i x + B_i u \ (i = 1, 2)$$
 (16)

where x is the state vector of the independent states:

$$x = \begin{bmatrix} i_m & i_{L1} & i_{L2} & v_{Cc} & v_{Co} \end{bmatrix}^T$$
 (17)

8 10 12 Load current (A)

and u is the input vector of the independent sources:

$$u = \begin{bmatrix} V_g & I_o \end{bmatrix}^T. \tag{18}$$

ACFC with CDR (L_m = 200μH & Lik = 3μH)

Lik ZVS ACFC ($L_m = 80\mu$ H & $Lik = 5\mu$ H) L_m ZVS ACFC ($L_m = 40\mu$ H & $Lik = 3\mu$ H)

From Fig. 3 (a), A_1 and B_1 can be described as follow:

$$A_{1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{(R_{L1} + R_{t})}{L_{1}} & 0 & 0 & -\frac{1}{L_{1}} \\ 0 & 0 & -\frac{R_{L2}}{L_{2}} & 0 & -\frac{1}{L_{2}} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_{0}} & \frac{1}{C_{0}} & 0 & 0 \end{bmatrix} B_{1} = \begin{bmatrix} \frac{1}{L_{m}} & 0 \\ \frac{1}{NL_{1}} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{1}{C_{0}} \end{bmatrix} . (19)$$

From Fig. 3 (b), A_2 and B_2 can be described as follow:

$$A_{2} = \begin{vmatrix} 0 & 0 & 0 & -\frac{1}{L_{m}} & 0 \\ 0 & -\frac{R_{t1}}{L_{1}} & 0 & 0 & -\frac{1}{L_{1}} \\ 0 & 0 & -\frac{(R_{t2} + R_{t})}{L_{2}} & -\frac{1}{NL_{2}} & -\frac{1}{L_{2}} \\ \frac{1}{C_{c}} & 0 & -\frac{1}{NC_{c}} & 0 & 0 \\ 0 & \frac{1}{C_{o}} & \frac{1}{C_{o}} & 0 & 0 \end{vmatrix}$$
 $B_{2} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{1}{C_{o}} \end{bmatrix}$. (20)

For the duty cycle of the main switch, S_1 , and the auxiliary switch, S_2 , which are assumed to be D and (1-D), respectively, the state-space averaged model which is indicated by a single equivalent set is

$$\dot{x} = Ax + Bu \ (i = 1, 2)$$
 (21)

where the equivalent matrices are defined as

$$A = DA_1 + (1 - D) A_2$$

$$B = DB_1 + (1 - D) B_2$$
(22)

The steady-state solution can be obtained when (21) is equal to 0. Therefore, the DC values indicated by capital letters can be obtained by solving the following:

$$X = -A^{-1}BU. (23)$$

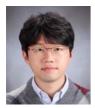
Unless R_{LI} , R_{L2} , and R_t are considered on (19) and (20), A becomes a singular matrix. Then (23) does not provide unique solution for the DC values. Consequently, R_{LI} , R_{L2} , and R_t should be considered in case of the ACFC with a CDR, unlike the conventional ACFC.

REFERENCES

- [1] J. A. Cobos, O. Garcia, J. Uceda, J. Sebastian, and E. de la Cruz, "Comparison of high efficiency low output voltage forward tolopogies," in 25th Annual IEEE Power Electronics Specialists Conference (PESC), Vol. 2, pp. 887-894, Jun. 1994.
- [2] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," *IEEE Trans. Power Electron.*, Vol. 11, No. 1, pp. 162-169, Jan. 1996.
- [3] Q. Li, F. C. Lee, and M. M. Jovanovic, "Design considerations of transformer DC bias of forward converter with active-clamp reset," in 14th Annual Applied Power Electronics Conference and Exposition (APEC), Vol. 1, pp. 553-559, Mar. 1999.
- [4] Y. Xi and P. K. Jain, "A forward converter topology employing a resonant auxiliary circuit to achieve soft switching and power transformer resetting," *IEEE Trans. Ind. Electron.*, Vol. 50, No. 1, pp. 132-140, Feb. 2003.
- [5] V. Tuomainen and J. Kyyra, "Effect of resonant transition on efficiency of forward converter with active clamp and self-driven SRs," *IEEE Trans. Power Electron.*, Vol. 20, No. 2, pp. 315-323, Mar. 2005.
- [6] Y. K. Lo, T. S. Kao, and J. Y. Lin, "Analysis and design of an interleaved active-clamping forward converter," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 4, pp. 2323-2332, Aug. 2007
- [7] T. Qian and B. Lehman, "Dual interleaved active-clamp forward with automatic charge balance regulation for high input voltage application," *IEEE Trans. Power Electron.*, Vol. 23, No. 1, pp. 38-44, Jan. 2008.
- [8] H. Huang, "Design guidelines on the effect of resonant transitions of forward converter on efficiency with active clamp," in 23rd Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 600-606, Feb. 2008.
- [9] D. H. Park, H. J. Kim, and Y. S. Sun, "A development of the off-line active clamp ZVS forward converter for telecommunication applications," in 19th International Telecommunications Energy Conference (INTELEC), pp. 271-276, Oct. 1997.
- [10] J. A. Cobos, O. Garcia, J. Sebastian, and J. Uceda, "Resonant reset forward topologies for low output voltage on board converters," in 9th Annual Applied Power Electronics Conference and Exposition (APEC), Vol. 2, pp. 703-708, Feb. 1994.
- [11] J. Feng, Y. Hu, W. Chen, and C. Wen, "ZVS analysis of asymmetrical half-bridge converter," in *IEEE Power Electronics Specialists Conference (PESC)*, Vol. 1, pp. 243-247, 2001.
- [12] B. R. Lin, H. K. Chiang, C. E. Huang, and D. Wang,

- "Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier," in *IEEE Region 10 TENCON*, pp. 1-6, 2005.
- [13] K. B. Park, G. W. Moon, and M. J. Yoon, "Two-switch active-clamp forward converter with one clamp diode and delayed turnoff gate signal," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 10, pp. 4768-4772, Oct. 2011.
- [14] K. B. Park, C. E. Kim, G. W. Moon, and M. J. Youn, "Three-switch active-clamp forward converter with low switch voltage stress and wide ZVS range for high-input voltage applications," *IEEE Trans. Power Electron.*, Vol. 25, No. 4, pp. 889-898, Apr. 2010.
- [15] A. Acik and I. Cadirci, "Active clamped ZVS forward converter with soft-switched synchronous rectifier for high efficiency, low output voltage applications," in *IEE Proc. Electric Power Application*, Vol. 150, No. 2, pp. 165-174, Mar. 2003.
- [16] S. Yang, Z. Qian, Q. Ouyang, and F. Z. Peng, "An improved active-clamp ZVS forward converter circuit," in 23rd Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 318-322, 2008.
- [17] S. S. Lee, S. W. Choi, and G. W. Moon, "High efficiency active clamp forward converter with synchronous switch control ZVS operation," *Journal of Power Electronics*, Vol. 6, No. 2, pp. 131-138, Mar. 2006.
- [18] H. J. Chiu and L. W. Lin, "A high efficiency soft-switched AC-DC converter with current doubler synchronous rectification," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 3, pp. 709-718, Jun. 2005.
- [19] U. Badstuebner, J. Biela, D. Christen, and J. W. Kolar, "Optimization of a 5-kw telecom phase-shift DC-DC converter with magnetically integrated current doubler," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 10, pp. 4736-4745, Oct. 2011.
- [20] B. R. Lin, K. Huang, and D. Wang, "Analysis and implementation of full-bridge converter with current doubler rectifier," in *IEE Proceedings Electric Power* Applications, Vol. 152, No. 5, pp. 1193-1202, Sep. 2005.
- [21] L. Huber and M. M. Jovanovic, "Forward-flyback converter with current-doubler rectifier: Analysis, design, and evaluation results," *IEEE Trans. Power Electron.*, Vol. 14, No. 1, pp. 184-192, Jan. 1999.
- [22] Y. Wen, H. Mao, and I. Batarseh, "DC bias analysis and small-signal characteristic of active-clamp forward-flyback DC-DC converter with a current doubler rectifier," in 20th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Vol. 3, pp. 1531-1536, 2005.
- [23] I. D. Jitaru and S. Birca-Galateanu, "Small-signal characterization of the forward-flyback converters with active clamp," in *IEEE Applied Power Electronics* Conference and Exposition (APEC), pp. 626-632, 1998.
- [24] J. Sun and V. Mehrotra, "Unified analysis of half-bridge converter with current-doubler rectifier," in 16th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Vol. 1, pp. 514-520, Mar. 2001.
- [25] H. J. Chiu and L. W. Lin, "A high-efficiency soft-switched AC/DC converter with current-doubler synchronous rectification," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 3, pp. 709-718, Jun. 2005.
- [26] N. H. Kutkut, D. M. Divan, and R. W. Gascoigne, "An improved full-bridge zero-voltage-switching PWM converter using a two-inductor rectifier," *IEEE Trans. Ind. Appl.*, Vol. 31, No. 1, pp. 119-126, Jan./Feb. 1995.
- [27] X. Ruan and J. Wang, "Calculation of the resonant capacitor

- of the improved current-doubler-rectifier ZVS PWM full-bridge converter," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 2, pp. 518-520, Apr. 2004.
- [28] N. Frohleke, J. Richter, P. Wallmeier, and H. Grotstollen, "Soft switching forward-flyback converter with one magnetic component and current doubler rectification circuit," in *IEEE Industry Applications Conference*, pp. 1161-1168, Vol. 2, Oct. 1996.
- [29] B. R. Lin and H. K. Chiang, "Analysis and implementation of a soft switching interleaved forward converter with current doubler rectifier," *IET Electric Power Applications*, pp. 697-704, Sep. 2007.
- [30] Y. C. Kuo, C. T. Tsai, Y. P. Kuo, N. S. Pai, and Y. C. Luo, "An active-clamp forward converter with a current-doubler circuit for photovoltaic energy conversion," in *International Conference on Information Science, Electronics and Electrical Engineering (ISEEE)*, Vol. 1, pp.513-517, Apr. 2014
- [31] P. Xu, Q. Wu, P. L. Wong, and F. C. Lee, "A novel integrated current-doubler rectifier," in 15th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Vol. 2, pp. 735-740, Feb. 2000.
- [32] P. Xu, M. Ye, and F. C. Lee, "Single magnetic push-pull forward converter featuring built-in input filter and coupled-inductor current doubler for 48 V VRM," in 17th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Vol. 2, pp.843-849, Mar. 2002.
- [33] J. Sun, K. F. Webb, and V. Mehrotra, "Integrated magnetics for current-doubler rectifiers," *IEEE Trans. Power Electron.*, Vol. 19, No. 3, pp. 582-590, May 2004.
- [34] H. Zhou, T. X. Wu, I. Batarseh, and K. D. T. Ngo, "Comparative investigation on different topologies of integrated magnetic structures for current-doubler rectifier," in *IEEE Power Electronics Specialists Conference (PESC)*, pp. 337-342, Jun. 2007.
- [35] C. W. T. McLyman, Transformer and Inductor Design Handbook, 4th Edition, CRC Press, 2004



Paul Jang received his B.S. degree in Electrical Engineering from Seoul National University, Seoul, Korea, in 2010; where he is presently working towards his Ph.D. degree. His current research interests include converter parallel operation, modular converter systems, distributed power systems, and soft switching converters.



Hye-Jin Kim received his B.S. and M.S. degrees in Electrical Engineering from Seoul National University, Seoul, Korea, in 2010, and 2012, respectively; where he is presently working towards his Ph.D. degree. His current research interests include the design, analysis, and control of power factor correction converters and distributed power systems.



Bo-Hyung Cho received his B.S. and M.S. degrees from the California Institute of Technology, Pasadena, CA, USA; and his Ph.D. degree from the Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA, all in Electrical Engineering. Prior to his research at Virginia

Tech, he was a member of the Technical Staff with the Department of Power Conversion Electronics, TRW Defense and Space System Group, USA. From 1982 to 1995, he was a Professor in the Department of Electrical Engineering, Virginia Tech. In 1995, he joined the School of Electrical Engineering, Seoul National University, Seoul, Korea, where he is presently working as a Professor. His current research interests include power electronics, distributed power systems, and the modeling, analysis and control of spacecraft power processing equipment. Dr. Cho is a member of Tau Beta Pi. He was a recipient of the 1989 Presidential Young Investigator Award from the National Science Foundation. He chaired the 2006 IEEE Power Electronics Specialists Conference.