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Analysis, Design, and Implementation of a High-Performance Rectifier

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Abstract

A high-performance rectifier is introduced in this study. The proposed rectifier combines the conventional pulse width modulation, soft commutation, and instantaneously average line current control techniques to promote circuit performance. The voltage stresses of the main switches in the rectifier are lower than those in conventional rectifier topologies. Moreover, conduction losses of switches in the rectifier are certainly lower than those in conventional rectifier topologies because the power current flow path when the main switches are turned on includes two main power semiconductors and the power current flow path when the main switches are turned off includes one main power semiconductor. The rectifier also adopts a ZCS-PWM auxiliary circuit to derive the ZCS function for power semiconductors. Thus, the problem of switching losses and EMI can be improved. In the control strategy, the controller uses the average current control mode to achieve fixed-frequency current control with stability and low distortion. A prototype has been implemented in the laboratory to verify circuit theory.

Key words: Pulse width modulation, Rectifier, Soft switching

I. INTRODUCTION

DC power supply is an essential electric power source of various electronic products. Using a full-bridge diode rectifier with a large filter capacitor as the front-end rectification to obtain DC output voltage is the conventional method. However, this method will encounter excessively large peak input current and high harmonic distortion. Its input power factor is lower by approximately 0.5–0.6, which does not meet the IEC61000-3-2 limits. Thus, electronic product designers must conduct research on how to reduce input current harmonics and enhance input power factor for their DC power supplies. Inserting a power factor correction (PFC) circuit into the DC power supply is the most common method.

In various active power factor correctors, the boost power factor corrector is the most general circuit, as shown in Fig. 1(a) [1]-[7]. However, its conduction losses are large because its power current flow paths always include three main power semiconductors. Moreover, the commutation losses of its main power semiconductors are also large because its main power semiconductors are operated under hard-switching conditions.

Several power factor correctors with low conduction losses are proposed to address this problem [11]-[14]. These power factor correctors are the basic two-switch bridgeless PFC boost rectifier, as shown in Fig. 1(b) [11]-[13], and the totem pole bridgeless PFC boost rectifier, as shown Fig. 1(c) [14]. Their conduction losses are certainly lower than previous topologies because their power current flow paths only include two main power semiconductors. Several soft-switching topologies have been proposed to improve their commutation losses [15]-[19]. In previous topologies, the voltage stresses of their main active power switches are equal to the output voltage V_o. However, reducing voltage stress of semiconductors is a more important matter because the cost of semiconductors is dependent on the rated operation voltage.

A high-performance rectifier is proposed in this study, as shown in Fig. 1(d), to reduce conduction losses and commutation losses. The conduction losses in the proposed rectifier are certainly lower than those in previous topologies because the power current flow path when the main switches are turned on only includes two main power semiconductors and the power current flow path when the main switches are turned off only includes one main power semiconductor. Moreover, the proposed rectifier uses a ZCS auxiliary circuit to derive the ZCS function for its power semiconductors to improve commutation losses. The efficiency of the proposed

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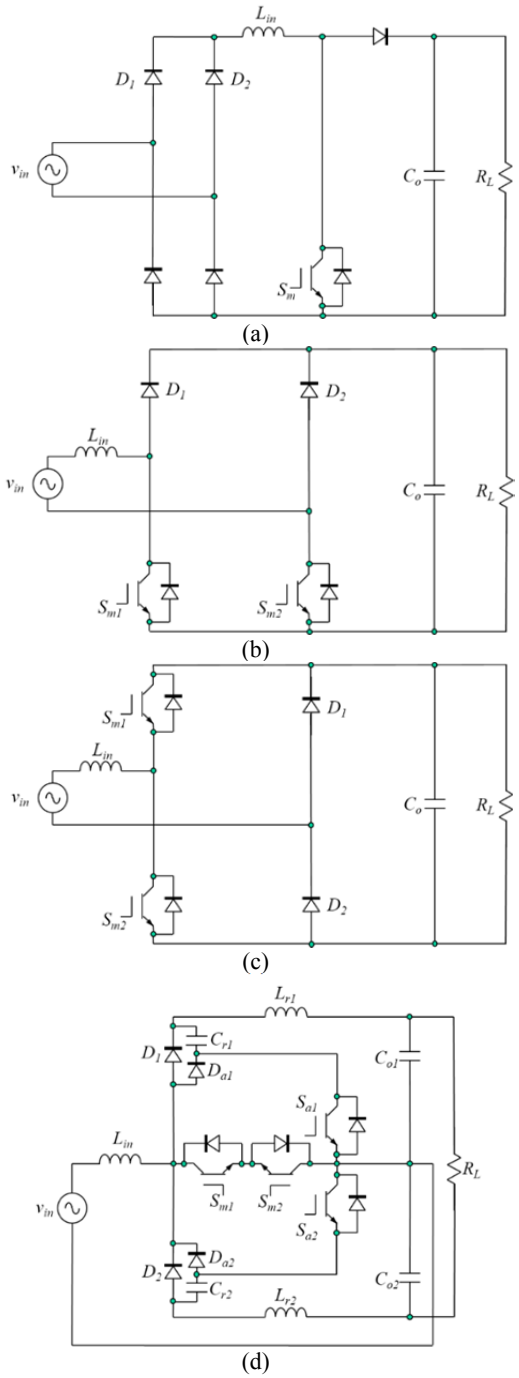


Fig. 1. (a) Conventional PFC boost rectifier [1], (b) basic two-switch bridgeless PFC boost rectifier [11], (c) totem pole bridgeless PFC boost rectifier [14], and (d) proposed high-performance rectifier.

rectifier will be higher than that in previously mentioned topologies. Moreover, the voltage stress of its main active power switches is equal to $V_o/2$ and is lower than one of the previously mentioned topologies. Thus, the main circuit cost of the proposed rectifier can be decreased. The comparisons of the number of semiconductors in the power current flow path and the voltage stress on the main semiconductors are shown in Tables I and II, respectively.

TABLE I
COMPARISON OF VOLTAGE STRESS ON THE MAIN SWITCHES AND DIODES IN DIFFERENT RECTIFIERS

	Main switches	Main diodes
Conventional PFC boost rectifier	V_o	V_o
Basic two-switch bridgeless PFC boost rectifier	V_o	V_o
Totem pole bridgeless PFC boost rectifier	V_o	V_o
Proposed high-performance rectifier	$V_o/2$	V_o

TABLE II
COMPARISON OF THE NUMBER OF SEMICONDUCTORS IN THE CURRENT FLOW PATH

	Switch ON	Switch OFF
Conventional PFC boost rectifier	3	3
Basic two-switch bridgeless PFC boost rectifier	2	2
Totem pole bridgeless PFC boost rectifier	2	2
Proposed high-performance rectifier	2	1

Accordingly, low voltage stresses, low switching losses, low conduction losses, and low EMI noise can be achieved in the proposed rectifier. In the control strategy, its controller uses the average current mode control to achieve fixed-frequency current control with stability and low distortion. Thus, the proposed rectifier has good dynamic characteristics. Its behavior is described by seven transition states during one switching period in the positive half-line period. A design strategy is built and a physical system of the 1 kW proposed rectifier is generated to assess system performance.

II. PRINCIPLE OF THE PROPOSED HIGH-PERFORMANCE RECTIFIER

A. Circuit Description

A power stage diagram of the proposed rectifier is shown in Fig. 1(d). The proposed rectifier is composed of a bridgeless PFC boost rectifier with low conduction losses and low voltage stress and a ZCS auxiliary circuit. The bridgeless PFC boost rectifier with low conduction losses and low voltage stress is operated in continuous conduction mode (CCM). Moreover, it is composed of an input inductor L_{in}, two main switches S_{m1} and S_{m2}, two main diodes D_1 and D_2, and two output capacitors C_{o1} and C_{o2}. The bridgeless PFC boost rectifier performs certain functions, such as PFC.

The ZCS auxiliary circuit is composed of two diodes D_{a1} and D_{a2}, two resonant inductors L_{r1} and L_{r2}, two resonant capacitors C_{r1} and C_{r2}, and two switches S_{a1} and S_{a1}, which

are rated as small power compared with the output power. The ZCS auxiliary circuit is used to perform ZCS functions for all power semiconductors in the proposed rectifier.

B. Principle of Operation

The drive signals of the main power switches (S_{m1} and S_{m2}) in the proposed rectifier are shown in Fig. 2(b). These main power switches are the same. Thus, both main switches are simultaneously turned on and off and the control circuit can be simplified. Moreover, the commercial PFC IC can be employed and the control circuit cost can be reduced. In the positive half cycle of the input line voltage, the current flows through the switch S_{m1} and the antiparallel diode of switch S_{m2} when the switches S_{m1} and S_{m2} are turned on. The power current flow path is changed to flow through diode D_1 when the switches S_{m1} and S_{m2} are turned off. Similarly, in the negative half cycle of the input line voltage, the current flows through the switch S_{m2} and the antiparallel diode of switch S_{m1} when the switches S_{m1} and S_{m2} are turned on. The power current flow path is changed to flow through diode D_2 when the switches S_{m1} and S_{m2} are turned off. Thus, lower conduction losses are achieved because the power current flow path only includes two power semiconductors when the switches S_{m1} and S_{m2} are turned on and the power current flow path only includes one power semiconductor when the switches S_{m1} and S_{m2} are turned off. Moreover, the proposed rectifier uses a dual boost rectifier topology. In one boost rectifier, which is composed of L_{in}, S_{m1}, the antiparallel diode of switch S_{m2}, D_1, and C_{o1} is operated in the positive half cycle of the input line voltage. In another boost rectifier, which is composed of L_{in}, S_{m2}, the antiparallel diode of switch S_{m1}, D_2, and C_{o2} is operated in the negative half cycle of the input line voltage. Both rectifiers show symmetrical topology. The voltages across C_{o1} and C_{o2} of the proposed rectifier without the additional balance circuit are approximately the same. Thus, the voltages across C_{o1} and C_{o2} are approximately equal to $V_o/2$. Moreover, the voltage stress across the main power switches is approximately equal to $V_o/2$.

C. State of Operation of the Proposed High-performance Rectifier

In the proposed rectifier circuit, circuit operation in the positive half cycle of the input line voltage is the same as that in the negative half cycle of the input line voltage. Thus, only the circuit operation in the positive half cycle of the input line voltage is described in this study to simplify the analysis. Given that the proposed rectifier is focused on higher power demand, it is operated in CCM. The operation of the ZCS auxiliary circuit has a short time interval compared with one switching period. Thus, input current i_{in} and output voltage v_o can be assumed to be constant values I_{ink} and V_o in the kth switching period, respectively. In addition, the following assumptions are made during one switching cycle:

1. The input voltage in the kth switching period is constant and equals V_{ink}.
2. $v_{Cr}(t)$ equals zero and $i_{Lr}(t)$ equals I_{ink}.

Based on these assumptions, circuit operations in one switching cycle can be divided into seven states. The seven dynamic equivalent circuits and the ideal relevant waveforms of the proposed rectifier during one switching period are shown in Figs. 3 and 4, respectively.

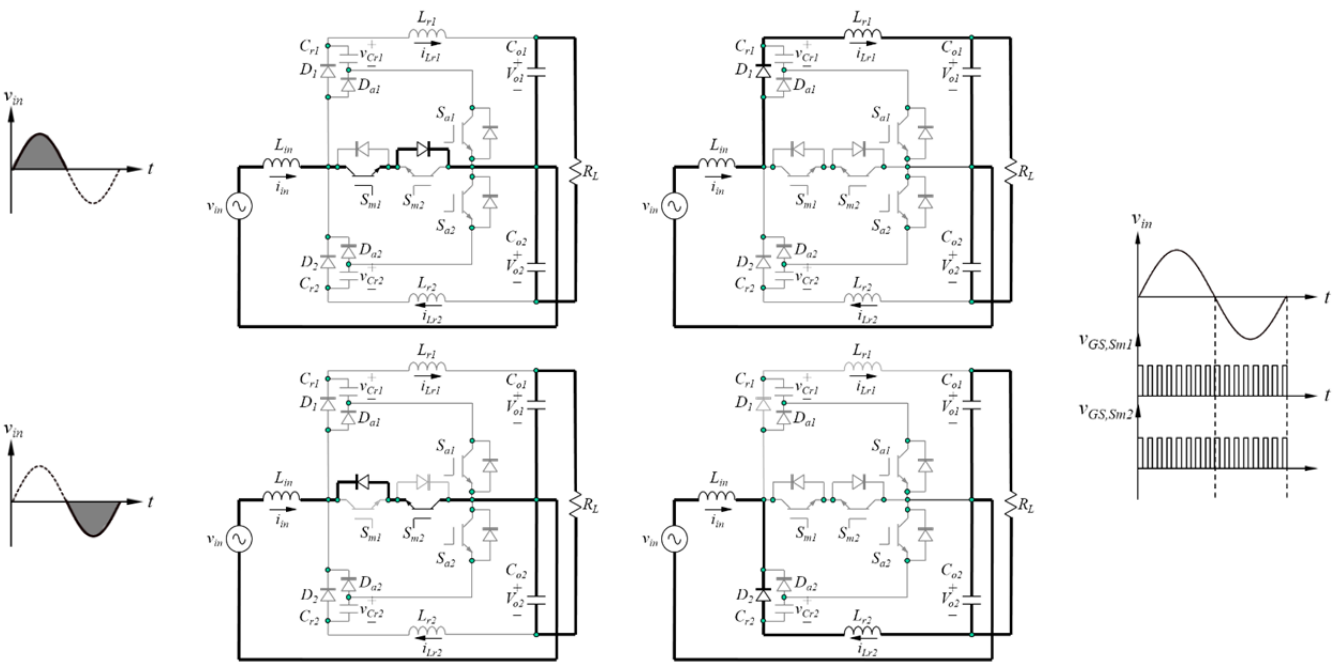


Fig. 2. (a) Topological states for operation mode. (b) Gate signals of main switches.

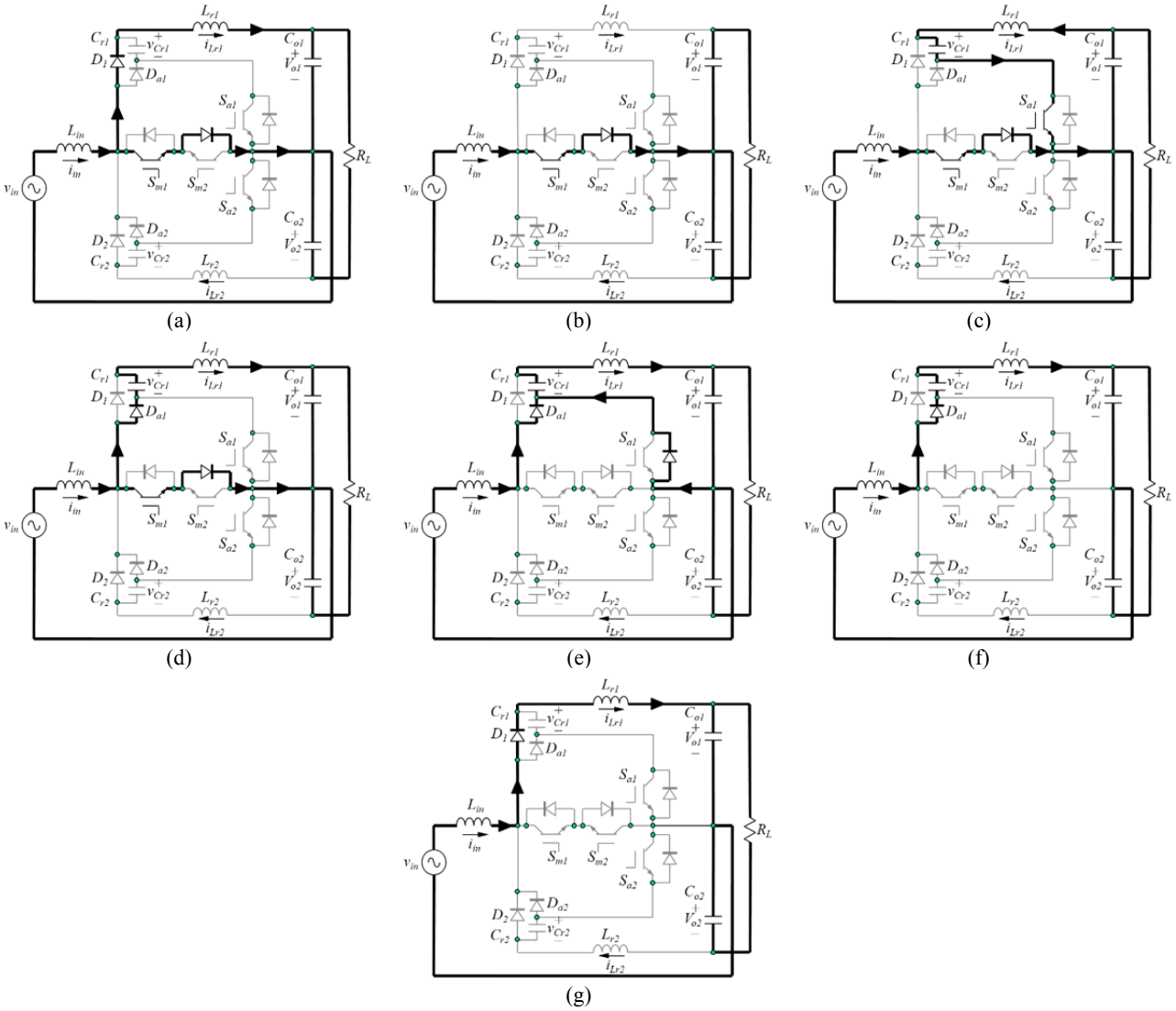


Fig. 3. The topology states of the proposed high-performance rectifier.

STATE 1: $[t_{k0}, t_{k1}]$, Fig. 3(a).

Before state 1, S_{m1} and S_{m2} maintain a turn-off state. The energy stored in inductors L_{in} and L_{r1} are delivered to capacitor C_{o1} through D_1. This state starts when the gates of S_{m1} and S_{m2} are triggered. S_{m1} is turned on under ZCS. Although S_{m2} is triggered, it is not turned on. Resonant inductor L_{r1} discharges linearly by output voltage V_o. Resonant current $i_{Lr}(t)$ decreases from I_{ink} to zero. The state is completed when $i_{Lr}(t)$ reaches zero and diode D_1 is naturally turned off.

STATE 2: $[t_{k1}, t_{k2}]$, Fig. 3(b).

Inductor L_{in} is charged by V_{ink} at this time. The other semiconductors maintain a turn-off state.

STATE 3: $[t_{k2}, t_{k3}]$, Fig. 3(c).

When S_{a1} is turned on under ZCS, the resonance behavior of C_{r1} and L_{r1} starts and this state also starts. The resonant path is through V_{o1}, L_{r1}, C_{r1}, and S_{a1}. $i_{Lr1}(t)$ initially increases and then decreases when it reaches its peak value. $v_{Cr1}(t)$ also increases. When $i_{Lr1}(t)$ drops to zero, the state ends.

STATE 4: $[t_{k3}, t_{k4}]$, Fig. 3(d).

During this state, the resonance behavior of C_{r1} and L_{r1} is on hold. However, the resonant path is changed through V_{o1}, L_{r1}, C_{r1}, D_{a1}, S_{m1}, and the antiparallel diode of S_{m2}. Although the resonant current can flow through the antiparallel diode of S_{a1}, the resonant current still only flows through S_{m1} and the antiparallel diode of S_{m2}. This phenomenon occurs because the voltage drop of S_{m1} and antiparallel diode of S_{m2} counterbalances the voltage drop of the antiparallel diode of S_{a1}, which makes the low impedance current path flow through S_{m1} and the antiparallel diode of S_{m2}. Moreover, based on Kirchhoff's current law, $i_{sm1} = i_{in} - i_{Lr1}$. Given that i_{Lr} is less than i_{in} and i_{sm1} is positive, no current flows through S_{m2} and the current flows through the antiparallel diode of S_{m2}. $v_{Cr1}(t)$ decreases and $i_{Lr1}(t)$ increases. This state ends when $i_{Lr1}(t)$ increases to I_{ink}.

STATE 5: $[t_{k4}, t_{k5}]$, Fig. 3(e).

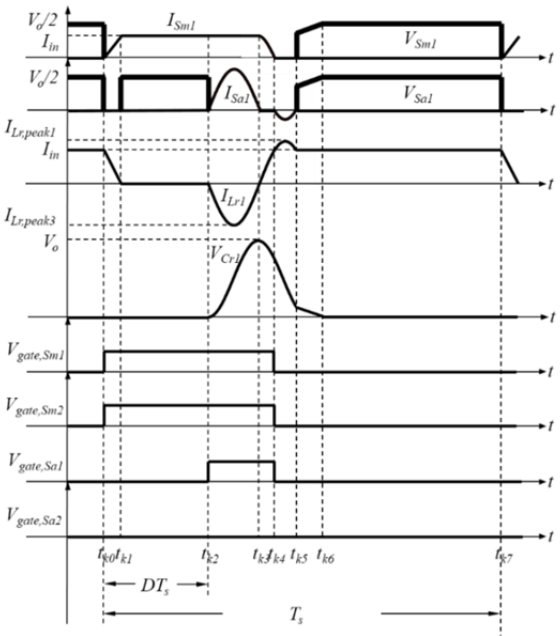


Fig. 4. Waveform diagram of the proposed high-performance rectifier under the *k*th switching period in the positive half cycle of the input line voltage.

The previous resonance operation is still maintained in this state. However, the resonant path is changed again and the resonant current flows through V_{o1}, L_{r1}, C_{r1}, and the antiparallel diode of S_{a1}. Given that the resonant current i_{Lr1} is larger than the input current i_{in}, the antiparallel diode of S_{m2} is reverse biased and is naturally turned off. Thus, no current flows through S_{m1}, S_{m2}, and S_{a1}. Turning S_{m1}, S_{m2}, and S_{a1} off is recommended under zero-current conditions. Thus, S_{m1}, S_{m2}, and S_{a1} are turned off at $t = t_{k4}$. $v_{Cr1}(t)$ continuously decreases. $i_{Lr1}(t)$ initially increases and then decreases when it reaches its peak value. This state ends when $i_{Lr1}(t)$ drops to I_{ink} again.

STATE 6: $[t_{k5}, t_{k6}]$, Fig. 3(f).

The resonant capacitor C_{r1} is discharged through D_{a1}, C_{r1}, L_{r1}, and V_{o1} in this state. Therefore, $v_{Cr1}(t)$ decreases linearly toward zero. This state ends when $v_{Cr1}(t)$ drops to zero again.

STATE 7: $[t_{k6}, t_{k7}]$, Fig. 3(g).

In this state, input inductor L_{in} is charged by V_{ink}. This state is maintained until S_{m1} is again turned on under zero-current conditions.

After state 7, the state of the circuit operation is restored to the first state. $v_{Cr1}(t)$ equals zero and $i_{Lr1}(t)$ also equals I_{ink}. Thus, the previous assumption is still valid.

D. Output Characteristics

The inductor voltage must satisfy Kirchhoff's voltage law under one switching period because the proposed rectifier is operated in the steady state. Thus,

$$V_{ink} \cong \left[(1-D) - \frac{\Delta t_3}{T_s} - \frac{\Delta t_4}{T_s} - \frac{\Delta t_5}{T_s}\right]\frac{V_o}{2}, \tag{1}$$

where:

$$\Delta t_3 \equiv t_{k3} - t_{k2} = \frac{\pi}{\omega_r}, \tag{2}$$

$$\Delta t_4 \equiv t_{k4} - t_{k3} = \frac{1}{\omega_r}\arcsin\left(\frac{I_{ink}Z_o}{V_o}\right), \tag{3}$$

$$\Delta t_5 \equiv t_{k5} - t_{k4} = \frac{\pi}{\omega_r} - 2\Delta t_4, \tag{4}$$

$$Z_o = \sqrt{\frac{L_r}{C_r}}, \tag{5}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}. \tag{6}$$

The voltage conversion ratio (M) can be expressed in Equation (7):

$$M(D) = \frac{V_O}{V_{in,rms}} \cong \frac{2\sqrt{2}}{(1-D) - \left[1 - \frac{1}{2\pi}\sin^{-1}\left(\frac{\sqrt{2}I_{in,rms}Z_O}{V_O}\right)\right]\left(\frac{f_S}{f_r}\right)} \tag{7}$$

Moreover, the voltage conversion ratios of the other topologies shown in Fig. 1 are identical and equal to $\sqrt{2}/(1-D)$. The voltage conversion ratio of the proposed rectifier without ZCS auxiliary circuit is $2\sqrt{2}/(1-D)$. Thus, the proposed rectifier has a voltage doubler characteristic compared with the other topologies. In addition, the voltage conversion ratio of the proposed rectifier with ZCS auxiliary circuit shown in Equation (7) reveals that f_s/f_r will influence the voltage conversion ratio. Given that the ZCS auxiliary circuit has an auxiliary role, a small f_s/f_r is recommended to reduce its effect.

E. Commutation Analysis

From the operation analysis of stage 5, the constraint of the following inequalities should be satisfied to achieve soft commutation in the proposed high-performance rectifier:

$$\frac{V_o/2}{Z_o} > I_{in,peak}. \tag{8}$$

Moreover, the turn-on time interval $\Delta t_{on,Sa1,2}$ of switch $S_{a1,2}$ must be less than the minimum conduction time.

$$\Delta t_{on,S_a} \le (1 - D_{\min})T_s, \tag{9}$$

where $D_{\min}$ is the minimum duty cycle.

The time interval $\Delta t_{on,Sa1,2}$ is governed by the following expression:

$$\Delta t_{on,S_a} = \Delta t_3 + \Delta t_4 = \frac{\pi}{\omega_r} + \frac{1}{\omega_r}\sin^{-1}\left(\frac{I_{ink}Z_o}{V_o}\right). \tag{10}$$

III. CONTROL STRATEGY

The functional block diagram of the controller of the proposed high-performance rectifier is shown in Fig. 5(a).

Moreover, the details of the control circuit of the proposed high-performance rectifier are shown in Fig. 5(b). The controller can be divided into two sections, namely, main PFC part and soft-switching control logic part. The main PFC part adopts the average current mode control method to correct the power factor. This study uses the commercial PFC control IC UC3854, which is produced by Texas Instruments Company, to perform basic PFC functions. The function block diagram of the IC UC3854 is shown in Fig. 5(a). For obtaining close unity power factor, UC3854 senses the synchronous line input voltage from transformer T. Moreover, it uses a multiplier/divider to combine several necessary signals, which include the feedforward synchronous line input voltage, the root–mean–square line input voltage, and the output feedback error voltage, to generate the current reference of the current error amplifier. The current error amplifier in the UC3854 uses the current reference and the output current signal of the Hall effect sensor to generate the error current to achieve the average current mode control function. Then, the error current signal enters the pulse width modulator. The pulse width modulator uses a comparator to compare the error current with the sawtooth waveform, which is a constant frequency signal used to generate the main PFC PWM control signal; this signal is in pin 16 of the UC3854.

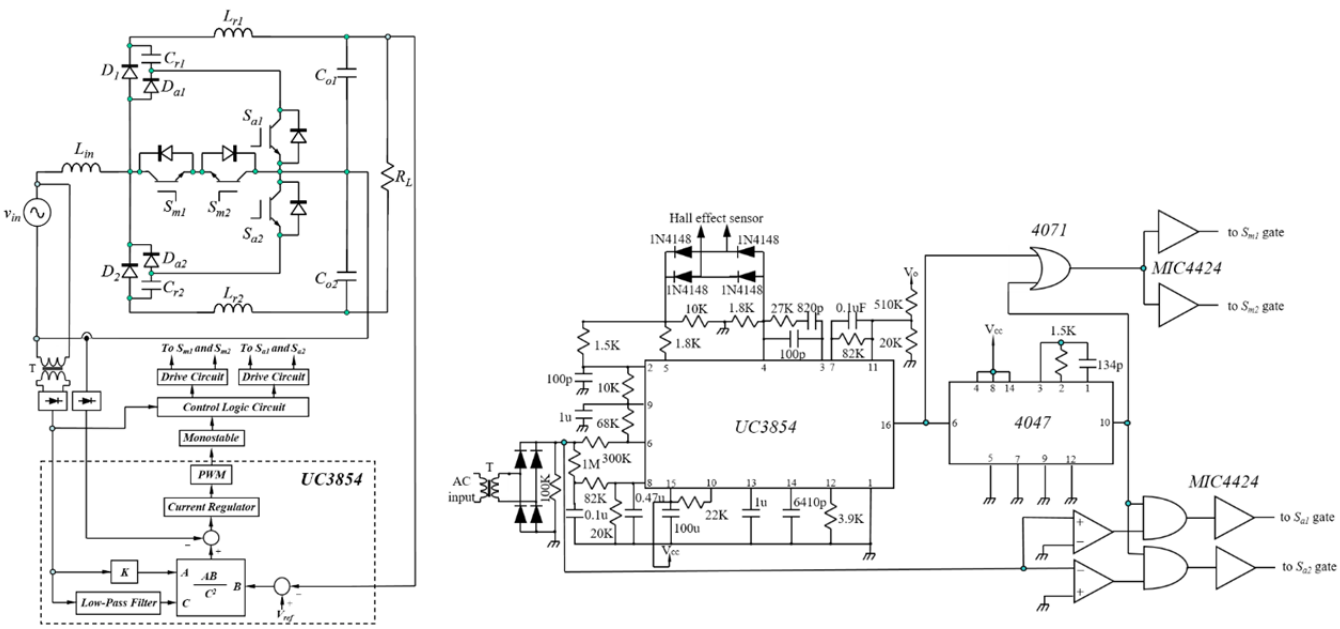
Then, the main PFC PWM control signal enters the soft-switching control logic part, which is composed of a monostable multivibrator, tow comparators, several logic gates, and four drive circuits, to obtain soft-switching control signals. Fig. 5(b) shows that the two comparators are used to determine the operational cycle of the input line voltage. First, the main PFC PWM control signal triggers the monostable multivibrator (IC CD4047) through the negative edge trigger mode. Then, the monostable multivibrator outputs a constant pulse width, which is the control signal of the auxiliary switches. The constant pulse width is distributed to auxiliary switches S_{a1} and S_{a2} according to the output signals of the two comparators. If the proposed rectifier operates in the positive half cycle of the input line voltage, then the constant pulse width signal is transmitted to drive S_{a1}; otherwise, it is transmitted to drive S_{a2}. Moreover, with regard to the generation method of the control signals of the main power switches (S_{m1} and S_{m2}), the main switches must maintain the turn-on state when the auxiliary switches are turned on according to previous main power circuit analysis. The main PFC PWM control signal must be synthesized with the constant pulse width signal by the OR gate to generate the new PFC PWM control signal. Given that the main switches (S_{m1} and S_{m2}) are simultaneously turned on and off according to the previous main power circuit analysis, the new PFC PWM control signal directly triggers the two power switches.

IV. Design Considerations and Experimental Results

A high-performance rectifier is designed and employed as an example. Its specifications are listed as follows:

- Input voltage: $v_{in}(t) = 155\sin(2\pi*60t)$;
- Output voltage: $V_o = 400$ V;
- Maximum output power: $P_{o,\max} = 1{,}000$ W;
- Switching frequency: $f_s = 40$ kHz.

The implemented power stage circuit of the proposed rectifier is shown in Fig. 5(a) and is focused on higher power demand. Therefore, the implemented power stage circuit of the



(a) (b)

Fig. 5. (a) Functional block diagram of the controller of the proposed high-performance rectifier. (b) Details of the circuit of the proposed high-performance rectifier controller.

proposed rectifier is operated under CCM. Its design procedure is described along with the previously described circuit characteristics, as follows:

1) Consideration of the Input Current Ripple and Selection of the Input Inductor L_{in}: When the input line voltage is at its maximum, the duty ratio D is at its minimum and can be calculated according to the conversion ratio of the conventional boost converter, as follows:

$$D_{\min} = (1 - \frac{V_{in,peak}}{V_o / 2}) = 0.225 . \quad (10)$$

The input ripple current is also at its maximum value at this time, which can be denoted as follows:

$$\Delta I_{in} = \frac{V_{in,peak}}{L_{in}} D_{\min} T_s . \quad (11)$$

The input ripple current is selected as 10% input maximum current. Thus,

$$\Delta I_{in,\max} = 0.1 \times \sqrt{2} \times \frac{P_{o,\max}}{V_{in,rms}} = 1.286 \text{ A} , \quad (12)$$

$$L_{in} = \frac{V_{in,peak}}{\Delta I_{in,\max}} D_{\min} T_s = 678 \text{ μH} . \quad (13)$$

Therefore, L_{in} = 680 μH is selected.

2) Selection of the Output Capacitor: The selection of the output capacitor is dependent on the switching frequency ripple current, the second harmonic ripple current, the output ripple voltage, and the hold-up time. The hold-up time is defined as the time required for the output voltage to remain within regulation after the AC input voltage is removed. However, the hold-up time often dominates the other factors in output capacitor selection. The output capacitor C_o will be selected according to the hold-up time requirements. Thus,

$$C_o \geq \frac{2 P_{o,\max} \Delta t}{V_o^2 - V_{o,\min}^2} , \quad (14)$$

where Δt is the hold-up time, $P_{o,\max}$ is the maximum output power, V_o is the output voltage, and $V_{o(\min)}$ is the minimum output voltage that the load can normally operate.

In this case, Δt = 34 ms, P_o = 1,000 W, V_o = 400 V, and $V_{o(\min)}$ = 300 V. Thus, C_o is 971 μF. C_o = 940 μF is selected.

3) Selection of the Resonant Parameters: Based on the specifications, the maximum input current can be obtained when the output power is rated as the maximum power, as follows:

$$I_{in,\max} = \frac{\sqrt{2} P_o}{V_{in,rms}} = 12.86 \text{ A} . \quad (15)$$

Thus, the peak input current is defined as follows:

$$I_{in,peak} = I_{in,\max} + \frac{\Delta I_{in,\max}}{2} = 13.5 \text{ A} . \quad (16)$$

Equation (7) shows that the voltage conversion ratio is relative to parameters D and f_s/f_r. The lower the value of f_s/f_r, the lower the effect of the ZCS switching cell. Thus, the value of f_s/f_r is recommended to be lower than 0.3. In this case, f_s/f_r = 0.1 is selected. Thus,

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} = 2\pi f_r = 20\pi f_s = 2.513 \times 10^6 \text{ rad/s} . \quad (17)$$

The inequality in (8) should be satisfied to ensure that the main power switch turns on and off under ZCS. Thus,

$$Z_o = \sqrt{\frac{L_r}{C_r}} \leq \frac{V_o}{2 I_{in,peak}} = 14.81 \, \Omega . \quad (18)$$

Thus, expression (18) divided by (17) results in the following equation:

$$L_r \leq \frac{V_o}{4\pi f_r I_{in,peak}} = 5.893 \times 10^{-6} \text{ H} . \quad (19)$$

$L_{r1} = L_{r2} = L_r$ = 4 μH is selected to clear the occurrence of zero-current switching. By substituting L_r = 4 μH into (17), C_r = 39.59 nF can be obtained, and $C_{r1} = C_{r2} = C_r$ = 47 nF is selected.

4) Selection of the Main Power Switches and Diodes: From the circuit operation analysis, the maximum current through the main switches (S_{m1}, S_{m2}) and the main diodes (D_1, D_2) and the maximum voltages across them can be calculated as follows:

$$i_{DS1,\max} = i_{DS2,\max} \cong I_{in,\max} = \frac{\sqrt{2} P_{o,\max}}{V_{in,rms}} = 12.86 \text{ A} , \quad (20)$$

$$v_{DS1,\max} = v_{DS2,\max} \cong V_o / 2 = 200 \text{ V} , \quad (21)$$

$$i_{D1,\max} = i_{D2,\max} \cong I_o = \frac{P_{o,\max}}{V_o} = 2.5 \text{ A} , \quad (22)$$

$$v_{D1,\max} = v_{D2,\max} \cong V_o = 400 \text{ V} . \quad (23)$$

5) Selection of the auxiliary power switches and diodes.

From the circuit operation analysis, the maximum current through auxiliary switch S_a and the maximum voltage across it can also be obtained as follows:

$$i_{DSa1,\max} = i_{DSa2,\max} \cong I_{Lr,peak3} = \frac{V_o / 2}{Z_o} = 13.5 \text{ A} , \quad (24)$$

$$v_{DSa1,\max} = v_{DSa2,\max} \cong V_o / 2 = 200 \text{ V} . \quad (25)$$

In addition, the maximum current through auxiliary diodes D_{a1} and D_{a2} and the maximum voltage across them can also be obtained as follows:

$$i_{Da1,\max} = i_{Da2,\max} \cong I_{Lr,peak1} = \frac{V_o / 2}{Z_o} = 13.5 \text{ A} , \quad (26)$$

$$v_{Da1,\max} = v_{Da2,\max} \cong V_o = 400 \text{ V} . \quad (27)$$

Thus, IRFP 264 and DSEP30-06A MOSFETs are selected as the power switches and diodes to fulfill the hardware requirements. UC3854 is selected as the controller. The circuit parameters of the UC3854 controller can be defined according to [20]. Fig. 6(a) illustrates the experimental

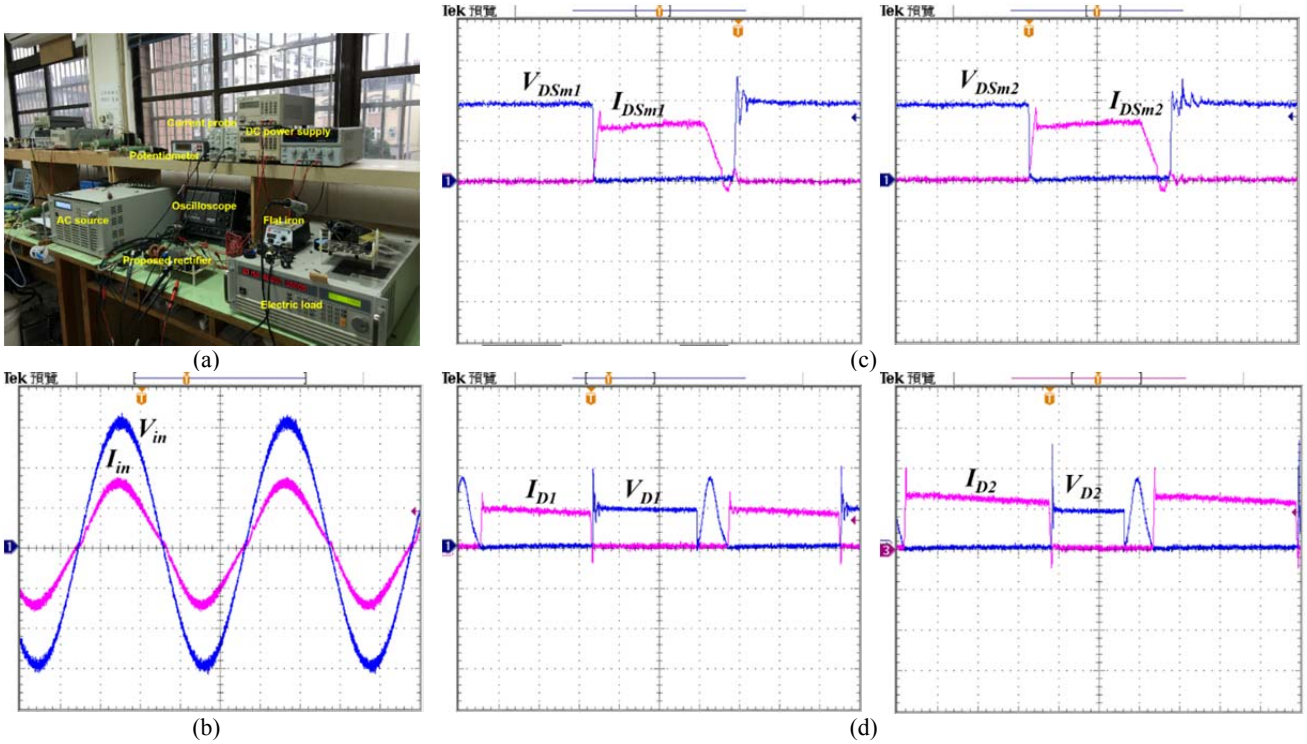


Fig. 6. (a) Experimental platform. (b) Waveforms of input voltage $v_{in}(t)$ and input current $i_{in}(t)$ under 1,000 W output power rating. v_{in} = 50 V/div; i_{in} = 10 A/div; time = 4 m/div. (c) Commutation in main switches S_{m1} and S_{m2} under 1,000 W output power rating. V_{DSm1}, V_{DSm2} = 100 V/div; I_{DSm1}, I_{DSm2} = 10 A/div; time = 2 μs/div. (d) Commutation in main diodes D_1 and D_2 under 1,000 W output power rating. V_{D1}, V_{D2} = 250 V/div; I_{D1}, I_{D2} = 10 A/div; time = 4 μs/div.

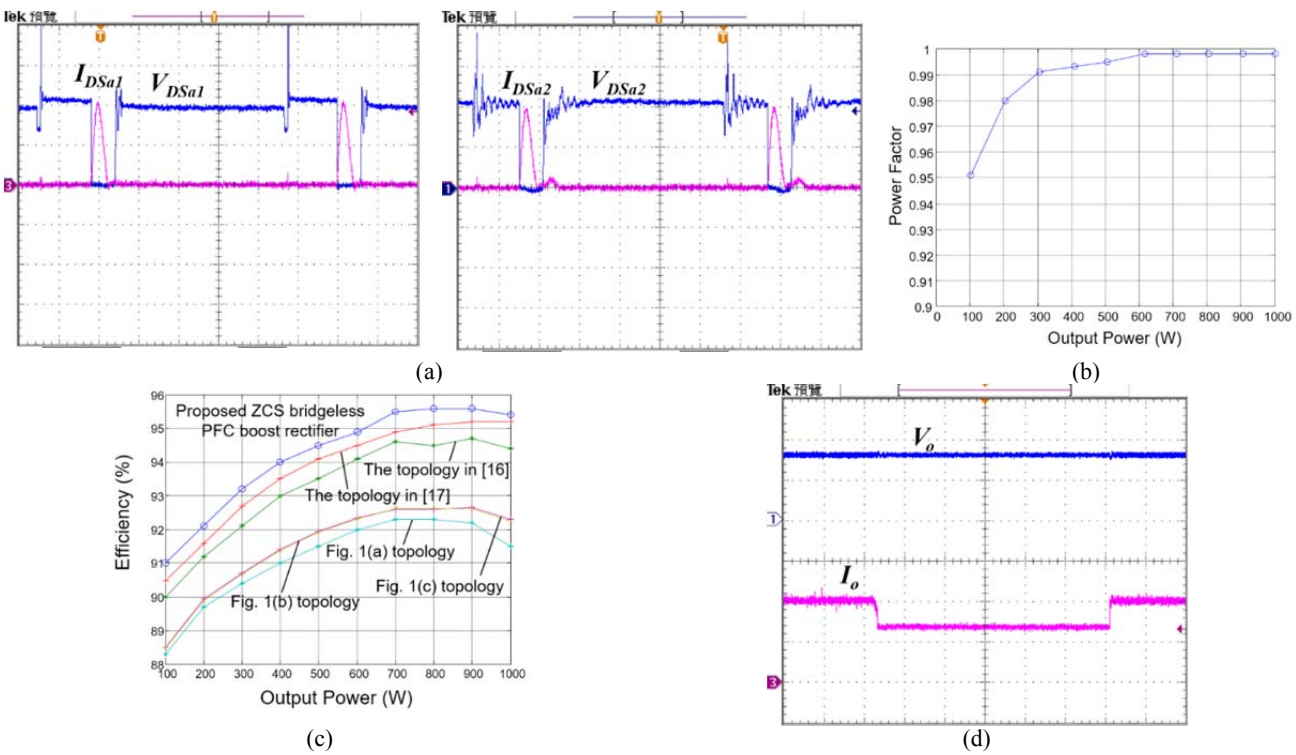


Fig. 7. (a) Commutation in auxiliary switches S_{a1} and S_{a2} under 1,000 W output power rating. V_{DSa1}, V_{DSa2} = 100 V/div; I_{DSa1}, I_{DSa2} = 10 A/div; time = 4 μs/div.(b) Power factor according to the output power. (c) Experimental efficiency of the proposed ZCS bridgeless PFC boost rectifier compared with the other topologies. (d) Transient waveforms of the output voltage and current during load change (V_o = 250 V/div; I_o = 1 A/div; time = 20 ms/div).

platform for this work. The waveforms of the input voltage and current are almost in phase and the measured power factor is more than 0.99, as shown in Fig. 6(b). A high power factor has been achieved. The commutation phenomenon in main switches S_{m1} and S_{m2}, auxiliary switches S_{a1} and S_{a2}, and main diodes D_1 and D_2 is measured and shown in Figs. 6(c), 6(d), and 7(a), respectively. The experimental results shown in Figs. 6(c), 6(d), and 7(a) reveal that ZCS is achieved for these active switches (S_{m1}, S_{m2}, and S_a). Main diodes D_1 and D_2 were also softly commutated under ZCS. Therefore, the switching losses for the main switches and main diodes are practically zero. Moreover, the voltage stresses of the active power switches are equal to $V_o/2$ = 200 V according to the experimental results shown in Figs. 6 and 7. The voltage stresses of the active power switches in other topologies with soft-switching technique [15]-[19] are equal to half of that in the topologies [15]-[19]. Lower voltage stress on the active power switches in the proposed rectifier has been achieved and verified.

The measured power factor curves versus output power with different input voltages and versus input voltage with different output powers are shown in Fig. 7(b). The power factors are greater than 0.9 under all conditions. This result reveals that a high power factor is achieved. The measured efficiency curves versus output power with different topologies are shown Fig. 7(c). Given that the traditional topologies shown in Figs. 1(a), 1(b), and 1(c) are operated under hard-switching conditions, the efficiencies of topologies with soft-switching technique, which include the proposed rectifier and the topologies in [16] and [17], are higher than the efficiencies of traditional topologies shown in Figs. 1(a), 1(b), and 1(c). Fig. 7(c) shows the experimental results for verification. Moreover, conduction losses in the proposed rectifier are less than those in the topologies with soft-switching technique [16], [17]. The efficiency of the proposed rectifier is higher than the efficiency of the topologies in [16] and [17], which can also be verified from the experimental results shown in Fig. 7(c). The transient waveforms of the output voltage and current during load change are shown in Fig. 7(d), which reveals that the effect of load changing on the output voltage is small. Thus, the dynamic characteristic of the proposed rectifier is good.

V. Conclusion

A high-performance rectifier is proposed in this study. A prototype circuit of the proposed rectifier has been implemented. The proposed rectifier has the following characteristics:

1) Main switches S_{m1}, S_{m2}, D_1, and D_2 can achieve ZCS.
2) Main switches S_{m1} and S_{m2} have lower voltage stresses compared with the other boost rectifiers.
3) The proposed rectifier uses the ZCS auxiliary circuit to obtain soft-switching functions.
4) The proposed rectifier is regulated by the conventional PWM technique at constant frequency. Thus, it combines the advantages of PWM and soft-switching techniques.
5) High power efficiency of approximately 95.5% is acquired under the rated power of 1,000 W.

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