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A Novel Control Scheme for T-Type Three-Level SSG Converters Using Adaptive PR Controller with a Variable Frequency Resonant PLL

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Abstract

In this paper, a novel quasi-direct power control (Q-DPC) scheme based on a resonant frequency adaptive proportional-resonant (PR) current controller with a variable frequency resonant phase locked loop (RPLL) is proposed, which can achieve a fast power response with a unity power factor. It can also adapt to variations of the generator frequency in T-type Three-level shaft synchronous generator (SSG) converters. The PR controller under the static *α-β* frame is designed to track ac signals and to avert the strong cross coupling under the rotating *d-q* frame. The fundamental frequency can be precisely acquired by a RPLL from the generator terminal voltage which is distorted by harmonics. Thus, the resonant frequency of the PR controller can be confirmed exactly with optimized performance. Based on an instantaneous power balance, the load power feed-forward is added to the power command to improve the anti-disturbance performance of the dc-link. Simulations based on MATLAB/Simulink and experimental results obtained from a 75kW prototype validate the correctness and effectiveness of the proposed control scheme.

Key words: Proportional-resonant control, Quasi direct power control, Resonant phase locked loop, Shaft synchronous generator, T-type there-level converter

I. INTRODUCTION

A combination of a brushless excite synchronous generator (BESG) and an ac/dc/ac converter scheme is widely applied in variable-speed constant-frequency (VSCF) generation systems, such as ship shaft generation and wind turbine generation, to harvest matched load power or maximum power from synchronous generator. The concept of a shaft generator converter has been around for decades due to its many distinct advantages, such as using cheaper natural gas instead of diesel fuel, better efficiency for combustion engines, and reduced noise level in ship rooms [1]. The main purpose of this application is to make full use of the surplus power of combustion engines to provide power for the ship grid. An ac/dc/ac converter consists of a pulse width modulation (PWM) rectifier, an intermediate dc-link capacitor and a PWM inverter [2]. The rectifier is used to transfer specific power from the BESG to the dc-link capacitor. The inverter connected to the dc-link is used to generate constant-voltage constant-frequency (CVCF) power for ship grid. In particular, multilevel topologies, such as the T-type three-level converter as a modification of the neutral point control (NPC) converter, are more efficient than other multilevel converters in low-voltage applications [3], [4]. Fig. 1 shows a T-type three-level SSG back-to-back converter.

The rectifier control scheme has been widely studied by scholars in grid-connected operating conditions [5]-[11]. However, few studies have been carried out in the synchronous generator-connected mode. From the existing related literature, several practical control strategies have been proposed for grid-rectifiers, such as voltage-oriented vector control based on a decoupled proportional-integral (PI) regulator [5], direct power control with a fixed switching frequency [6], [7], model predictive control [7], [8], repetitive control [9], fuzzy control [10] and sliding-mode control [11].

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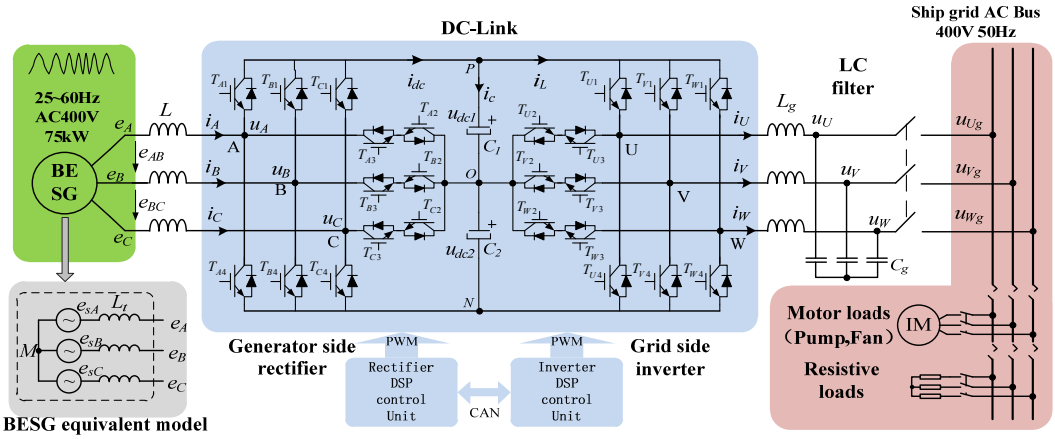


Fig. 1. The structure of T-type three-level SSG converter.

These control strategies have been successfully applied to grid-connected rectifier control with improved performance.

In order to improve the response performance of current-loops, several methods have been proposed [12]-[17]. In [12], the control of a distributed generation converter under the rotating *d-q* frame using a Park transformation has been analyzed, in which 3-phase sinusoidal quantities are transformed into constant values under rotating *d-q* coordinates and a PI controller with inductance decoupling to eliminate errors. However, a strong coupling item $\omega_e L$ under *d-q* coordinates makes it difficult to design the controller, especially when the system frequency ω_e or inductance L varies [13], [14].

The authors of [15] proposes a complex vector PI (CVPI) control under the *d-q* fame to solve the coupling problem from the perspective of the controller itself. However, the designation of the CVPI controller needs frequency information, which deteriorates the system performance. Reference [16] proposes a predictive current control scheme with load power feed-forward to enhance the system response. However, the dynamic/static response of the predictive current control depends on an accurate predictive mathematical model and an appropriate cost function [17]. To solve these problems, a proportional-resonant (PR) controller under the static *α-β* frame has been proposed [18], [19] and the static error of the sinusoidal signal control at the resonant frequency point can be completely eliminated because the PR controller can provide an infinite gain at this frequency. As a result, the inductance-frequency coupling item is removed and the current control performance can be greatly enhanced. However, unlike PI controllers, the PR controller is always difficult to design to make the control system stable because the PR controller is a multi-order system, especially when taking the digital control delay into consideration [20]. Reference [21] proposes a PR controller design method based on the root locus trajectory and a cascaded compensator, where the PR parameters can be confirmed to ensure the system stability and dynamic response. In order to achieve a fast transient response, reference [22] proposes a methodology to optimize the transient response of the PR current controller. This is based on the study of the error signal transfer function roots by the means of the pole-zero plots in the z-domain. All of these schemes are applied in a small scale variation of the frequency (grid-connected mode). In a VSCF generation system, the frequency of the synchronous generator voltage varies more significantly than that in the grid-connected mode and the synchronous reactance is larger than the line impedance of the grid [23]. To obtain the best performance from the PR control, its resonant frequency must be identical to the generator frequency [23]. Thus, it should be noticed that an adaptive adjustment of the PR control is necessary when generator frequency variations are registered in the system [24], [25]. The ideal way to accomplish this is to observe the precise generator frequency in real time to modify the PR parameters [26].

The frequency observer is generally realized by a phase-locked loop (PLL). The grid-connected rectifier can lock the frequency and phase by a PLL while most of the generator-connected rectifiers can realize this by a position encoder. However, the moist and vibrating conditions on a ship make the encoder hard to maintain. Moreover, the generator voltage is distorted. As a result, the frequency and phase are difficult to obtain by a traditional PLL or position encoder. When the detected voltage is distorted by low-order harmonics or switching frequency harmonics, the precise frequency and phase are hard to obtain by a general digital PLL (DPLL) which is called a traditional PLL [27]. In some references, an enhanced PLL is proposed to lock the frequency in a polluted utility grid [27]-[30]. The authors of [28] propose a grid synchronization PLL based on an adaptive low-pass notch filter, which is a modified version of a PLL based on the fast Fourier transform, which is robust to harmonics and imbalances of the grid voltage. The authors of [30] present a state-feedback quasi-static PLL model, which can identify and quantify the inherent frequency

self-synchronization mechanism in converter control systems. All of these methods realize the grid-phase lock under harmonic distortions but do not take wide frequency variations into consideration and are hard to design in digital signal processors. As a result, a variable frequency resonant PLL is proposed based on a multi-resonant-compensator to solve this problem in this paper.

The structure of this paper is presented as follows. In section II, the T-type three-level SSG converter system and the operational principle are introduced. A mathematical model under the static α-β frame of a PWM rectifier and its instantaneous power model are set up in Section III. In Section IV, an adaptive adjustment PR current controller is proposed based on a mathematical model of a current-loop, to reduce the inductance-frequency coupling impact on the current control performance. Based on the method of the frequency response and the method of the root locus trajectory, the PR parameters are designed for the purpose of the dominant pole configuration. In order to obtain an accurate generator frequency to adjust the resonant frequency of the PR controller, the analysis and design of the variable frequency resonant phase locked loop based on a multi-resonant compensator are discussed. According to the instantaneous power balance, an inverter power feed-forward scheme is proposed in the dc-link control loop to ease the burden of the voltage controller. A small-signal model is established to analyze the anti-turbulence of the dc-link voltage power charge. The results of simulations and prototype experiments are presented in Section V. The feasibility and validity of the proposed control scheme have been verified. Finally, some conclusions are presented in Section VI.

II. Analysis of the System Structure

The topology structure of a T-type three-level shaft synchronous generator converter is shown in Fig. 1.

- The brushless excited synchronous generator (BESG) is a four-pole synchronous generator which is equipped with an automatic voltage regulator (AVR). The synchronous speed is 1500*rpm*. The rotor of the synchronous generator is connected to the principal axis of a ship engine through the clutch, which can operate from 25Hz to 60Hz. By designing the AVR, the output voltage of the generator is stabilized at 400V while its frequency varies from 25Hz to 60Hz. The main purpose of this design is to realize operation at the full power scale when the ship speed varies.
- The full-power back-to-back T-type three-level converter is the core part in this system. It includes a PWM rectifier and a grid inverter. In order to avoid over modulation, the target voltage of the dc-link ought to be set at 600V. The grid inverter should be able to operate in the stand-alone operational mode and the grid-connected operational mode. In addition, smooth-switching between the two modes is also essential. Both sides communicate with each other through the DSP's controller area network (CAN) bus.

III. Mathematical Model of a Three-Level T-Type Converter

In Fig. 1, the left half part is a T-type three-level PWM rectifier circuit. L is the ac inductance, and R is the ac inductor inner resistance. $C=C_1/2=C_2/2$ is the polar film capacitor between the dc stack buses. e_x, i_x and u_x ($x=A,B,C$) denote the generator voltages, input currents and phase voltages of rectifier respectively. S_x=-1,0,1 stands for the switching function. i_{dc} and i_L denote the current from rectifier to the dc-link and the load current from the dc-link to the inverter, while u_{dc1}, u_{dc2} and u_{dc} represent the upper/lower capacitors voltages and dc-link voltage respectively. u_y and i_y ($y=U,V,W$) denote the grid side voltages and currents.

Taking phase A as an example, when T_{A1} and T_{A2} are closed and T_{A3} and T_{A4} are open, S_A=1, and the voltage u_{AO} = $u_{dc}/2$. When T_{A2} and T_{A3} are closed and T_{A1} and T_{A4} are open, S_A=0, and the voltage u_{AO} = 0. When T_{A3} and T_{A4} are closed and T_{A1} and T_{A2} are open, S_A=-1, and the voltage u_{AO} = $-u_{dc}/2$. According to this principle, the tri-state switching function S_x can be decomposed into three two-state switching functions S_{xP}, S_{xO} and S_{xN} as follows:

$$S_x = \begin{cases} 1 \Leftrightarrow & S_{xP}=1, S_{xO}=0, S_{xN}=0 \\ 0 \Leftrightarrow & S_{xP}=0, S_{xO}=1, S_{xN}=0 \\ -1 \Leftrightarrow & S_{xP}=0, S_{xO}=0, S_{xN}=1 \end{cases} \quad (x=A,B,C) \tag{1}$$

The mathematical model of the three-level T-type PWM rectifier in the static a-b-c frame can be derived as:

$$\begin{cases} L\dfrac{di_A}{dt}+Ri_A=e_A-\left(u_{AO}-u_{MO}\right) \\ L\dfrac{di_B}{dt}+Ri_B=e_B-\left(u_{BO}-u_{MO}\right) \\ L\dfrac{di_C}{dt}+Ri_C=e_C-\left(u_{CO}-u_{MO}\right) \end{cases} \tag{2}$$

$$\begin{cases} C_1\dfrac{du_{dc1}}{dt}+i_L=i_AS_{AP}+i_BS_{BP}+i_CS_{CP} \\ C_2\dfrac{du_{dc2}}{dt}+i_L=-i_AS_{AN}-i_BS_{BN}-i_CS_{CN} \end{cases} \tag{3}$$

u_{xO} and u_{MO} can be expressed as follows:

$$\begin{cases} u_{AO}=u_{dc1}S_{AP}-u_{dc2}S_{AN} \\ u_{BO}=u_{dc1}S_{BP}-u_{dc2}S_{BN} \\ u_{CO}=u_{dc1}S_{CP}-u_{dc2}S_{CN} \end{cases} \tag{4}$$

$$u_{MO}=\frac{1}{3}u_{dc1}\sum_{x=A,B,C}S_{xP}-\frac{1}{3}u_{dc2}\sum_{x=A,B,C}S_{xN} \tag{5}$$

By applying the Clark transformation T_{clark} = $\frac{2}{3}\begin{bmatrix}1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2\end{bmatrix}$, Eq. (2) and Eq. (3) can be derived in

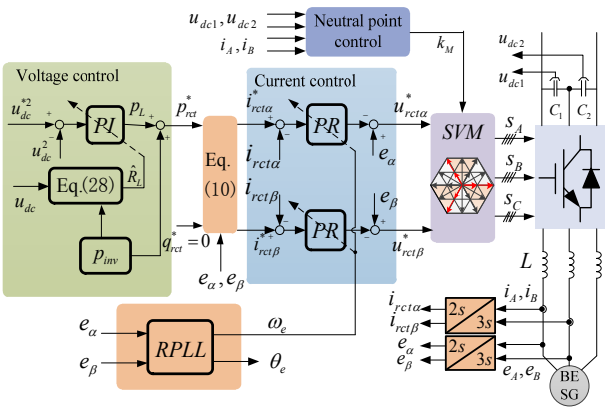


Fig. 2. The block of proposed quasi-DPC control scheme.

the stationary α-β frame as:

$$\begin{cases} L\dfrac{di_{rct\alpha}}{dt} + Ri_{rct\alpha} = e_\alpha - u_{rct\alpha} \\ L\dfrac{di_{rct\beta}}{dt} + Ri_{rct\beta} = e_\beta - u_{rct\beta} \end{cases} \tag{6}$$

$$\begin{cases} u_{rct\alpha} = u_{dc1}S_{\alpha P} - u_{dc2}S_{\alpha N} \\ u_{rct\beta} = u_{dc1}S_{\beta P} - u_{dc2}S_{\beta N} \end{cases} \tag{7}$$

$$\begin{cases} C_1\dfrac{du_{dc1}}{dt} + i_L = \dfrac{3}{2}\left(i_{rct\alpha}S_{\alpha P} + i_{rct\beta}S_{\beta P}\right) \\ C_2\dfrac{du_{dc2}}{dt} + i_L = -\dfrac{3}{2}\left(i_{rct\alpha}S_{\alpha N} + i_{rct\beta}S_{\beta N}\right) \end{cases} \tag{8}$$

where the subscript *rct* denotes the generator side variables. $i_{rct\alpha}$, $i_{rct\beta}$, $u_{rct\alpha}$, $u_{rct\beta}$, e_α and e_β are the ac current, rectifier input voltage and generator voltage in the stationary α-β frame, respectively. $S_{\alpha P}$, $S_{\beta P}$ and $S_{\alpha N}$, $S_{\beta N}$ are the coordinate components of S_{xP} and S_{xN} in the stationary α-β frame.

The primary function of the T-type PWM rectifier in a SSG converter system as a power converter is to absorb specific active and reactive powers from the BESG to keep a constant dc-link voltage. The instantaneous active and reactive powers are given by:

$$\begin{bmatrix} p_{rct} \\ q_{rct} \end{bmatrix} = \frac{3}{2}\begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix}\begin{bmatrix} i_{rct\alpha} \\ i_{rct\beta} \end{bmatrix} \tag{9}$$

where p_{rct} and q_{rct} mean the active power and reactive power. Assuming that p^*_{rct} and q^*_{rct} are the given values of the active and reactive powers from the BESG and that the rectifier operates in the unity power factor (i.e., q^*_{rct}=0), then the input current commands $i^*_{rct\alpha}$ and $i^*_{rct\beta}$ are derived as:

$$\begin{bmatrix} i^*_{rct\alpha} \\ i^*_{rct\beta} \end{bmatrix} = \frac{2}{3}\frac{p^*_{rct}}{(e_\alpha^2 + e_\beta^2)}\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \tag{10}$$

Due to the three-phase balanced generator voltages and the constant voltage amplitude from 25Hz to 60Hz, the current commands $i^*_{rct\alpha}$ and $i^*_{rct\beta}$ are in the phase of the generator voltages e_α and e_β. According to the mathematical model established above, an adaptive proportional-resonant (PR) current controller in the stationary α-β frame and a proportional-integral (PI) voltage controller based on the

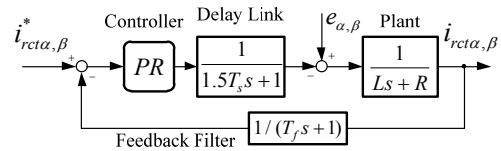


Fig. 3. Control model scheme of current inner-loop.

principle of simultaneous power balance can be designed. In general, there are two types of PR controllers. They are as follows:

$$G'_{PR}(s) = K_p + \frac{K_r s}{s^2 + \omega_e^2} \tag{11}$$

$$G''_{PR}(s) = K_p + \frac{K_r}{s^2 + \omega_e^2} \tag{12}$$

where K_p and K_r denote the proportional coefficient and resonant coefficient, respectively. By contrasting Eq. (11) and Eq. (12), it can be observed that both of the controllers can have an infinite gain at the resonant frequency point. In the control system, the 180° delay phase-shifting is fed into the system by the Eq. (12) controller, while a 90° delay phase-shifting is fed by the Eq. (11) controller. Thus, Eq. (11) is selected for its better phase margin. This method improves the tracking performance of the ac signal and eliminates the steady-state error.

IV. Control Schemes of Converter

A. General Block of the Quasi-DPC Scheme

Based on an analysis of the mathematical model of a PWM rectifier and instantaneous power, a quasi-DPC control block with an adaptive resonant frequency PR controller is proposed and shown in Fig. 2. This scheme takes a dc voltage controller as an outer-loop to generate a given value of active power. Then it calculates the given value of the inner-loop current. A PI controller is chosen in the dc voltage control loop, while a PR controller is needed in the ac current inner-loop. The quasi-DPC scheme realizes the active and reactive power control by using a fast current controller.

However, considering the varying frequency of a BESG, a general PR controller with a constant resonant frequency cannot reach the expected performance. When the actual current frequency is very different from the resonant frequency of the PR controller, it can deteriorate the dynamic/static performance of the current loop. Therefore, a variable frequency resonant phase locked loop (RPLL) is proposed, which is used for tracking the frequency and phase of the BESG voltage. The output frequency of the RPLL can modify the resonant frequency of the PR controller, so that it can ensure that the PR controller regulates the ac current at the right frequency.

B. Resonant Frequency Adaptive PR Control Scheme

In order to improve the current dynamic response, the selection of the controller parameters seems especially important. Unlike the pole-zero cancellation method in the PI

TABLE I
THE SYSTEM PARAMETERS

Parameter	Value
Synchronous speed of BESG /*rpm*	1500
Operational frequency range of BESG /*Hz*	25↔60
AC inductance L/*mH*	0.3
AC inductor inner resistance R/*Ω*	0. 15
Polar film capacitor between DC link C/*μF*	1100
Filter inductance L_g/*mH*	0.5
Filter capacitor C_g/*μF*	10
Resistive load R_{Load} on the inverter side/*Ω*	4.2
Switching frequencies of IGBT /*kHz*	5

controller design, the second order PR controller needs the synthesis design method to optimize the controller parameters. Taking the control delay of a digital control system and the filter of the feedback current into consideration, from Eq. (6) and Eq. (11), a control block of the current inner-loop is set up in Fig. 3 and the currents formulas can be expressed as:

$$\begin{aligned} i_{rct\alpha,\beta} &= \frac{[K_p(s^2+\omega_e^2)+K_r s](T_f s+1)}{D(s)} i^*_{rct\alpha,\beta} \\ &+ \frac{(s^2+\omega_e^2)(1.5T_s s+1)(T_f s+1)}{D(s)} e_{\alpha,\beta} \\ &= i_{M\alpha,\beta} + i_{dis\alpha,\beta} \end{aligned} \tag{13}$$

In this formula, the characteristic polynomial D(s) is denoted as:

$$\begin{aligned} D(s) &= (s^2+\omega_e^2)(1.5T_s s+1)(Ls+R)(T_f s+1) \\ &+ K_p(s^2+\omega_e^2)+K_r s \end{aligned} \tag{14}$$

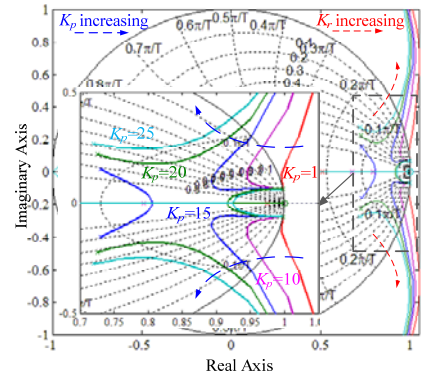
where T_s is the PWM control cycle, and T_f is the time constant of the feedback current filter (in this paper T_f=1/(2π5k)). $i_{M\alpha,\beta}$ is generated by the current reference, while $i_{dis\alpha,\beta}$ is generated by disturbances of the BESG voltage. At the resonant frequency point, no matter what the values of K_p (K_p>0) and K_r (K_r>0) are, the provided the system is stable, and the frequency response characteristic of Eq. 13 can be obtained as:

$$\begin{cases} \dfrac{i_{M\alpha,\beta}(j\omega_e)}{i^*_{rct\alpha,\beta}(j\omega_e)} = \left\{ \dfrac{[K_p(s^2+\omega_e^2)+K_r s](T_f s+1)}{D(s)} \right\}\Bigg|_{s=j\omega_e} = 1 \\ \dfrac{i_{dis\alpha,\beta}(j\omega_e)}{e_{\alpha,\beta}(j\omega_e)} = \left\{ \dfrac{(s^2+\omega_e^2)(1.5T_s s+1)(T_f s+1)}{D(s)} \right\}\Bigg|_{s=j\omega_e} = 0 \end{cases} \tag{15}$$

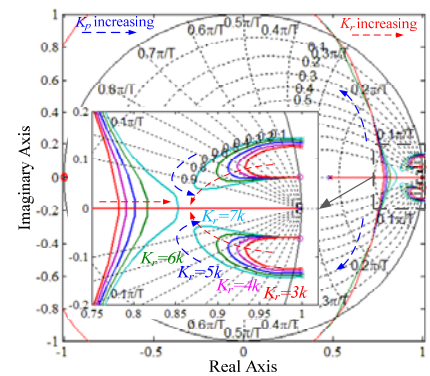
From Eq. 15, it can be observed that if the radian frequency of the current reference is equal to ω_e, the current controller can achieve zero static error. In addition, thedisturbance of the BESG voltage variation can also be eliminated.

Thus, the close-loop transfer function of the current inner-loop can be expressed as:

$$G_{cl}(s) = \frac{[K_p(s^2+\omega_e^2)+K_r s](T_f s+1)}{D(s)} \tag{16}$$



(a)



(b)

Fig. 4. The roots locus of current PR control loop with different parameters of (a) K_p=1,10,15,20,25 and (b) K_r=3k,4k,5k,6k,7k.

The corresponding open-loop transfer function is obtained as:

$$G_{ol}(s) = \frac{K_p(s^2+\omega_e^2)+K_r s}{(s^2+\omega_e^2)(1.5T_s s+1)(Ls+R)(T_f s+1)} \tag{17}$$

To achieve the realization of the digital control system, the discretization process is taken into the system. In this paper, a bi-linear discrete method (*Tustin*) is used [31]. It is given by:

$$s = \frac{2(1-z^{-1})}{T_s(1+z^{-1})} \tag{18}$$

By substituting the system parameters shown in Table I into Eq. (16), the root locus of the current closed-loop transfer function in the z-domain can be illustrated in Fig. 4. From Eq. (16) and Eq. (17), it is known that the current-loop is a fifth-order system by using a PR controller. In order to make the control loop obtain a better dynamic performance, the system predominant poles should be configured as a typical second-order system. Taking both the static and dynamic responses into consideration, the system damping coefficient ζ should be set to 0.707. Meanwhile, the three other poles should be kept away from the unit circle boundary. Firstly, with K_p confirmed in a specific range of values, the root locus in the z-domain with K_r varying from zero to infinity is drawn in Fig. 4(a). Then with K_r confirmed in a specific range of values, the root locus in the z-domain with K_p varying from zero to infinity is drawn in Fig. 4(b).

From Fig. 4(a), the following can be determined. When

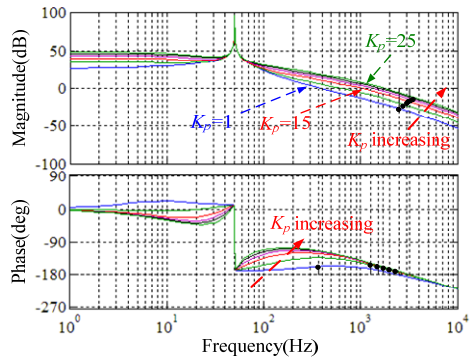


Fig. 5. Bode diagram of current open-loop with different K_p.

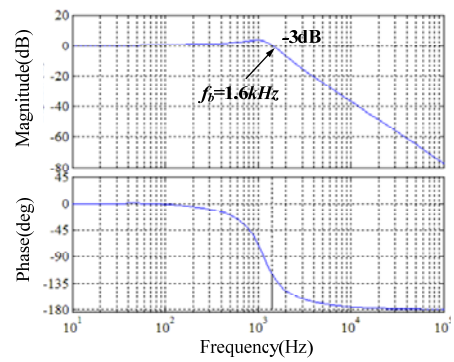
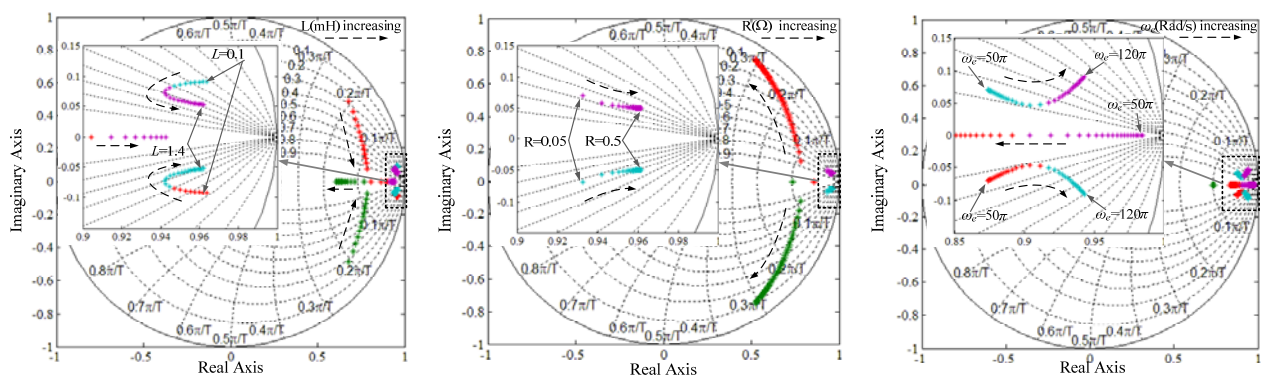


Fig. 6. Bode diagram of current of current closed-loop.



(a) (b) (c)

Fig. 7. Roots locus of current PR control loop corresponding to the change of system parameters of (a) L, (b) R, (c) ω_e.

$0<K_p<1$, the system root locus starts from the boundary of the unit circle and moves outside the circle. The system is unstable. As a result, there is no proper K_p. When $1<K_p<12$, the system root locus moves from the inner unit circle to outside the unit circle. However, the locus have not reached the equal damping ratio (ζ=0.707) line. There is no proper K_p. When $12<K_p<18$, the system root locus crosses the equal damping ratio (ζ=0.707) line and the poles on this line are nearer to the boundary of the unit circle unlike the other poles. Thus, there is a proper K_p in this value range. When $K_p>18$, the system root locus gradually goes away from the equal damping ratio. From Fig. 4(b), the following can be determined in the same way. When $0<K_r<4500$, the system root locus does not reach the equal damping ratio (ζ=0.707) line. There is no proper K_r. When $4500<K_r<5500$, the system root locus crosses the equal damping ratio (ζ=0.707) line. The predominant poles exist. There is a proper K_r in this value range. When $K_r>5500$, the poles at the cross points of the system root locus and the equal damping ratio line gradually get close to other poles, and lose the predominant function.

In addition, a certain gain margin and phase margin should also be considered to determine K_p. According to Eq. (16), an open-loop system bode diagram is illustrated in Fig. 5. When K_p varies from 1 to 25, the magnitude margin decreases slowly while the phase margin first increases and then decreases gradually. When K_p=25, the magnitude margin is 19.3dB and the phase margin is 31.3°. If K_p increases continuously, the phase margin becomes negative and the system becomes unstable.

Based on the principle discussed above, K_p=15.6 is confirmed. Meanwhile K_r=5400. Based on the designed parameters, the frequency response characteristic of the current closed-loop transfer function Eq. (16) is illustrated in Fig. 6. From this it can be seen that the system has a wider bandwidth f_b=1.61kHz which approaches to a twenty-six-fold current frequency. Therefore, the response of the current control loop to the current reference is very fast. According to the aforementioned analysis, quick instantaneous power control in a PWM rectifier can be realized as long as the response speed of the current control loop is fast enough. This makes the quasi-DPC scheme possible.

Generally, the parameters of a current control loop may change along with variations of ambient temperature and load. In order to confirm the controller robustness corresponding to changes in the inductance, resistance and frequency, the distribution of the characteristic roots along with the changes of these three parameters are drawn in the z-domain and shown in Fig. 7 (a)-(c). Fig. 7 (a) shows the migration of the characteristic roots of the current closed-loop transfer function when L changes from 0.1mH to 1.4mH, all of the closed-loop characteristic roots are located inside the unit circle and system is stable. Fig. 7 (b) shows the migration of the characteristic roots when R changes from 0.05Ω to 0.5Ω and all of the roots are located inside the unit circle.

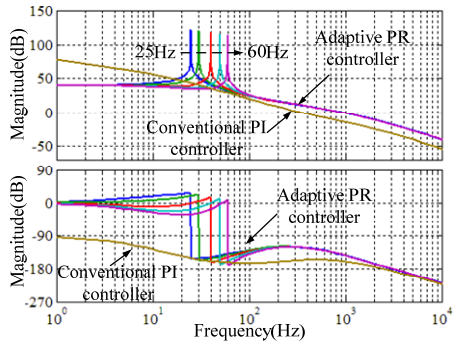


Fig. 8. Comparison of conventional PI controller and adaptive PR controller.

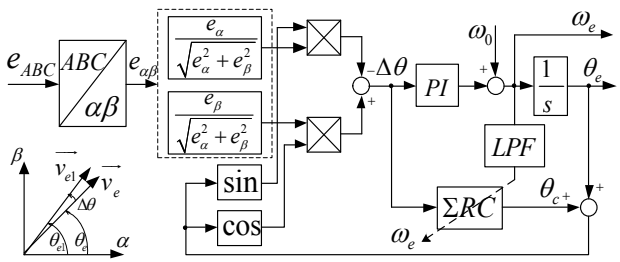


Fig. 9. Block of variable frequency RPLL.

However, they tend to move to the boundary of the unit circle. This may cause an unstable system as R increases. However, the line resistance in a high-power converter does not generally transcend to 0.5Ω. Thus, the system can be kept stable.

According to Fig. 7 (c), it can be observed that all of the characteristic roots are located inside the unit circle, when ω_e varies from 50π *rad/s* (25Hz) to 120π *rad/s* (60Hz). However, all of these roots are much closer to the boundary of the unit circle and tend to move outside of it when the frequency decreases or increases. In particular ω_e decreases approaching to 50π *rad/s* (25Hz), and the roots move much closer to the boundary of the unit circle along the path of the real axis direction. Thus, the frequency of the BESG should be tracked in real time to reduce the impact on the system stability against frequency variations. A comparison of a conventional PI controller and an adaptive PR controller is shown in Fig. 8. This indicates that an open loop transfer function with the proposed controller has a higher gain at a specific frequency than that with the conventional PI controller.

C. Variable Frequency Resonant PLL Design

Unlike the traditional rectifier circuit [12], the input of the rectifier circuit in this paper is the BESG, which has a higher impedance than the grid. Moreover, the designed inductance in the line is much smaller (0.3mH). When the driving signal comes out, the terminal voltage of the BESG is distorted by harmonics and its frequency varies from 25Hz to 60Hz. The conventional digital phase-locked loop (DPLL) faces a serious challenge in tracking the precise frequency and phase of a terminal voltage. Based on the theory of resonant control and a modified PLL which is based on the unity voltage

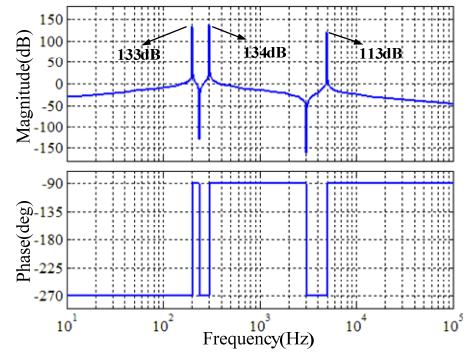


Fig. 10. Bode diagram of multi-resonant compensator.

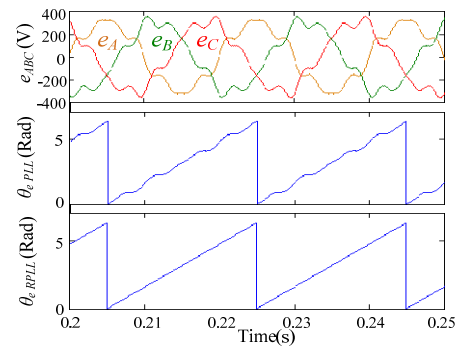


Fig. 11. Contrastive simulation of PLL and RPLL.

vector orientation, the fluctuation of the PLL output frequency and phase is compensated by multi resonant controllers (ΣRC). Then, the block of the variable frequency RPLL can be constructed in Fig. 9.

Assuming that θ_{e1} is the phase angle of the BESG voltage, v_{e1} is the unit voltage vector and θ_e is the output observed phase angle of the PLL, and v_e is the unit vector at its direction. The relationship among these variables is expressed as:

$$\begin{cases} v_{e1} = (\cos\theta_{e1}, \sin\theta_{e1}) \\ v_e = (\cos\theta_e, \sin\theta_e) \end{cases} \tag{19}$$

If $\Delta\theta=\theta_{e1}-\theta_e$, when $\Delta\theta\approx 0$, the following formula is obtained:

$$\begin{aligned} \Delta\theta \approx \sin\Delta\theta &= \sin(\theta_{e1}-\theta_e) \\ &= \sin\theta_{e1}\cos\theta_e - \cos\theta_{e1}\sin\theta_e \\ &= v_e \times v_{e1} \end{aligned} \tag{20}$$

This means that the two vectors product is approximately equal to the subtraction their phase angles.

By using a PI regulator to reduce the deviation between the two vectors, the angle frequency ω_e of the vector v_e can be obtained by the output of the PI. The integration of ω_e is equal to the observed phase angle θ_e. By analyzing the THD, the BESG voltage includes the 5th, 7th and a high frequency switching harmonic, which makes the angle deviation include the 4th, 6th and 99th harmonics [27]. A traditional PI regulator cannot eliminate this deviation which varies periodically and sinusoidally. Thus, a multi-resonant compensator scheme is introduced to eliminate the sinusoidal deviation. The transfer function of the multi-resonant compensator is expressed as:

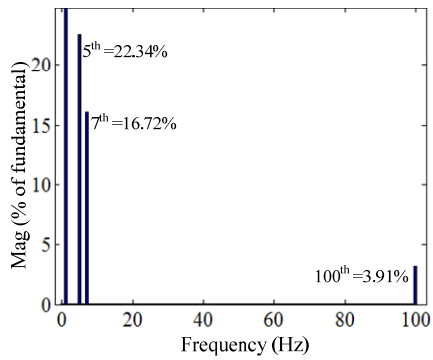


Fig. 12. Voltage harmonics analysis with THD.

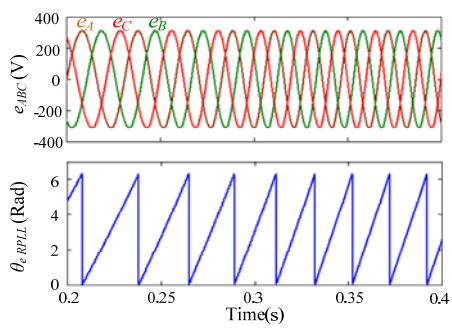


Fig. 13. frequency tracking process of RPLL from 30Hz to 50Hz.

$$G_{\Sigma R}(s)=\frac{K_{r4}s}{s^2+(4\omega_e)^2}+\frac{K_{r6}s}{s^2+(6\omega_e)^2}+\frac{K_{r99}s}{s^2+(99\omega_e)^2} \quad (21)$$

The compensation value θ_c is calculated by ΣRC to eliminate the deviation of the phase and frequency. However, when the fundamental frequency varies, the constant resonant compensator cannot realize the aforementioned effect. Therefore, the output frequency ω_e is used to modify the resonant frequency of the compensator. Then, self-adaptive tracking of the resonant frequency can be realized [28]-[30].

A Bode diagram of the multi-resonant compensator is shown in Fig. 10. It can be observed that a higher amplitude at the resonant frequency point can be achieved, which can realize the zero steady-state error control at this frequency.

When K_{r4}=400, K_{r6}=800 and K_{r99}=1000, the amplitudes are 133dB, 134dB and 113dB, respectively.

Fig. 11 shows a contrastive simulation of the PLL and the RPLL, when the voltage contains 5th, 7th and 100th harmonics. Fig. 12 shows the voltage THD. The simulation results indicate that obvious fluctuations of the phase appear in the traditional PLL, while the contrary is the case in the RPLL. In addition, the fast frequency tracking ability is essential for the variable frequency RPLL. Fig. 13 shows the frequency tracking process from 30Hz to 50Hz within a 0.2s interval.

D. Voltage Controller with Instantaneous Power Feed-Forward

The substance of the dc-link voltage fluctuation is that the generator rectifier input power is not equal to that in the grid inverter when a sudden load is imposed or unloaded. Assuming that R_L is the equivalent load resistance between the P-N points and noticing that $u_{dc}=2u_{dc1}=2u_{dc2}$, from Eq. (7)

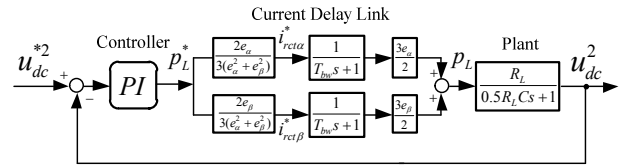


Fig. 14. Block of dc-link voltage outer-loop.

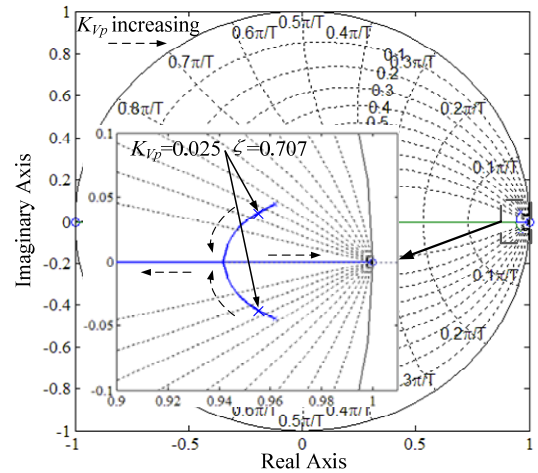


Fig. 15. Root locus plots in z-domain when K_{Vi}=49.5, $0<K_{Vp}<\infty$.

and Eq. (8) the instantaneous power balance equation is derived as:

$$p_L=\frac{3}{2}(i_{rct\alpha}u_{rct\alpha}+i_{rct\beta}u_{rct\beta})=\frac{C}{2}\frac{du_{dc}^2}{dt}+\frac{u_{dc}^2}{R_L} \quad (22)$$

where p_L stands for the absorbing power of the rectifier. The transfer function G_V(s) from the square of the dc voltage u_{dc}^2 to the instantaneous power p_L can be obtained:

$$G_V(s)=\frac{u_{dc}^2(s)}{p_L(s)}=\frac{R_L}{0.5R_LCs+1} \quad (23)$$

From Eq. (23), the relation between u_{dc}^2 and p_L represents linearity.

Therefore, the output of the dc voltage controller can be designed as:

$$p_L^*=(K_{Vp}+\frac{K_{Vi}}{s})(u_{dc}^{*2}-u_{dc}^2) \quad (24)$$

where K_{Vp} and K_{Vi} are the parameters of the PI regulator.

Considering the delay of the current inner-loop ($T_{bw}=1/2\pi f_b$), the dc voltage open-loop transfer function with a PI controller is obtained as:

$$G_{oV}(s)=\frac{R_L(K_{Vp}s+K_{Vi})}{s(0.5R_LCs+1)(T_{bw}s+1)} \quad (25)$$

The closed-loop transfer function is derived as:

$$G_{cV}(s)=\frac{K_{Vp}R_Ls+K_{Vi}R_L}{0.5R_LCT_{bw}s^3+(0.5R_LC+T_{bw})s^2+(K_{Vp}R_L+1)s+K_{Vi}R_L} \quad (26)$$

The control block of the dc-link voltage outer-loop is illustrated in Fig. 14.

Since $0.5R_LC>>T_{bw}$, Eq. (26) presents a nearly typical second order model. The damping ratio and natural frequency are given by:

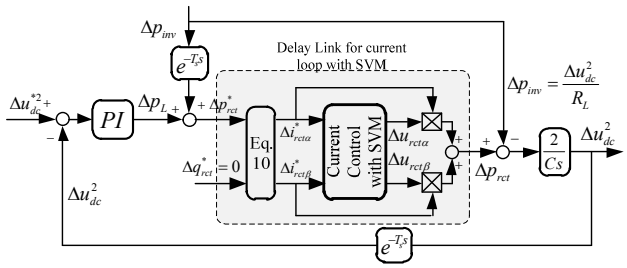


Fig. 16. The small-signal model of the proposed control scheme.

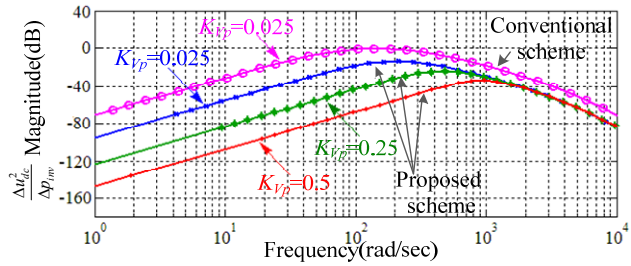
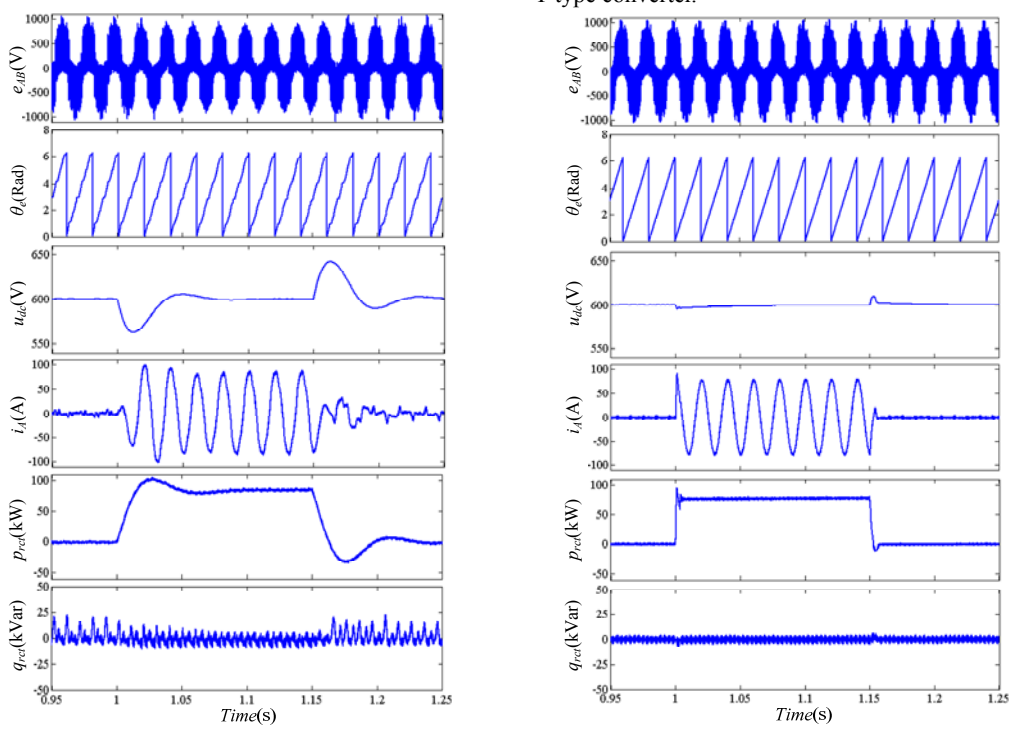


Fig.17. The bode diagram of small-signal model of three-level T-type converter.



(a) (b)

Fig. 18. Simulation results of the load sudden change transient response. (a) Conventional scheme. (b) Proposed scheme.

$$\begin{cases} \xi = (K_{Vp}R_L + 1)/(R_L C\sqrt{2K_{Vi}/C}) \\ \omega_n = \sqrt{2K_{Vi}/C} \end{cases} \tag{27}$$

To achieve better dynamic performance and stability, the damping ratio should be set to 0.707. The natural frequency should be designed as 300*rad/s* to avoid mutual interference between the voltage loop and the current loop. Therefore, at the rated load (i.e., R_L=4.8Ω), the parameters of the PI controller can be obtained as K_{Vp}=0.025 and K_{Vi}=49.5. When K_{Vi}=49.5, the root locus in the z-domain with an increase of K_{Vp} is shown in Fig. 15. It can be seen that the variation of K_{Vp} has very little impact on the system stability.

From Eq. (27), the gain value K_{Vp} of the PI controller is determined by the load. In order to maintain the designed optimal second order system performance, R_L should be estimated in real-time and the estimation method is given by:

$$\frac{u_{dc}^2}{\hat{R}_L} = p_{inv} \tag{28}$$

The parameters of the PI controller can be modified online.

Instantaneous power feed-forward is adopted to reduce the burden of the dc voltage regulator when the load changessuddenly:

$$p_{inv} = \frac{3}{2}(u_{inv\alpha}i_{inv\alpha} + u_{inv\beta}i_{inv\beta}) \tag{29}$$

$$p_{rct}^* = p_L^* + p_{inv} \tag{30}$$

where p_{inv} is the instantaneous power of the grid side inverter. $u_{inv\alpha}$, $u_{inv\beta}$ and $i_{inv\alpha}$, $i_{inv\beta}$ denote the grid side voltages and currents in the stationary α-β frame. p^*_{rct} is the active power command. Considering the inverter power feed-forward, p^*_L becomes the command of the capacitor charging power. Through this method, the system can keep an ideal dynamic performance in the entire power range with a smaller film capacitor (C=1100μF).

E. Small-Signal Analyses

In order to analyze the anti-disturbance capability of the dc-link voltage against sudden changes of load power, a small-signal model is established. The system state variables can be described as the sum of two parts i.e. the quantity on the operating point which is called a large signal and the

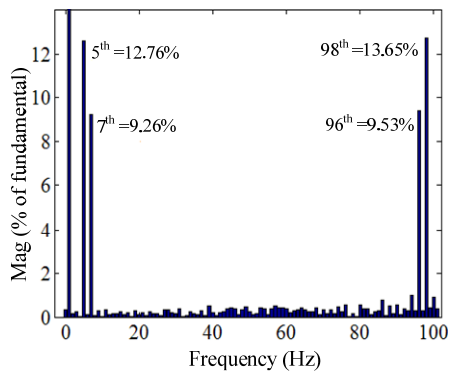


Fig. 19. generator voltage harmonics analysis with THD.

small deviation from the operating point which is called a small signal. This is shown by:

$$u_{dc}^2 = U_{dc}^2 + \Delta u_{dc}^2 \tag{31}$$

$$p_{inv} = P_{inv} + \Delta p_{inv} \tag{32}$$

$$p_{rct} = P_{rct} + \Delta p_{rct} \tag{33}$$

where U_{dc}^2, P_{inv} and P_{rct} stand for the large signal; and Δu_{dc}^2, Δp_{inv} and Δp_{rct} stand for the small signal. Substituting (31)-(33) into the state equations (6)-(8) and considering the PR current control with a SVM module as a $T_{bw}=1/2\pi f_b$ time delay, the small-signal model of the T-type converter is derived as:

$$\Delta u_{dc}^2 = \frac{2}{Cs}(\Delta p_{rct} - \Delta p_{inv}) \tag{34}$$

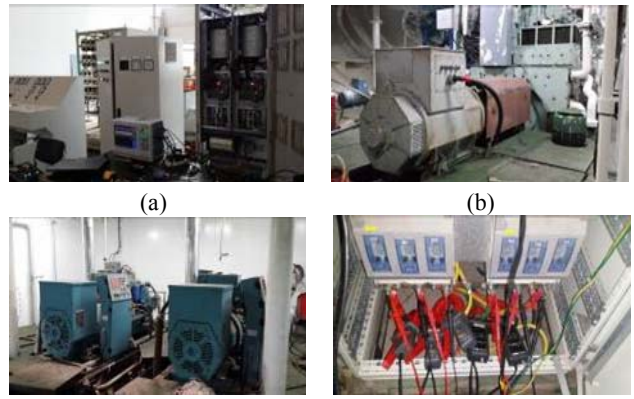
A small-signal model block with the proposed control scheme is illustrated in Fig. 16, from which the transfer function from Δp_{inv} to Δu_{dc}^2 is obtained as:

$$\frac{\Delta u_{dc}^2}{\Delta p_{inv}} = \frac{G_V(s)\dfrac{1}{T_{bw}s+1}e^{-T_s s}}{1+G_V(s)\dfrac{1}{T_{bw}s+1}(PI)e^{-T_s s}} \tag{35}$$

In Eq. (35), $PI=K_{Vp}+K_{Vi}/s$ is the voltage controller, and e^{-Ts} is the effect of the sampling delay on the digital control system, which can be replaced by a first-order delay by the Taylor series. Fig. 17 shows a Bode diagram of the proposed control scheme and the conventional control scheme. It is shown that the proposed scheme has a lower magnitude peak than the conventional scheme at the same low voltage controller gain (K_{Vp}=0.025), which does not lead to a large overshoot of the voltage response. Hence, fluctuations of dc-link voltage are suppressed with the power charges. When the dc-link voltage PI gain increases, the magnitude peak decreases. The system stability is investigated from the root locus plots i.e. Fig. 15. It is observed that the system is kept stable when K_{Vp} varies from 0.025 to 0.5 since the system poles stay within the unit circle.

V. Simulation and Experimental Results

To validate the proposed control scheme, the simulation of a 75kW T-type three-level SSG converter is established based on MATLAB/Simulink R2011b. The system parameters are listed in Table I.



(a) (b) (c) (d)

Fig. 20. Hardware prototype. (a) 75kW T-type three-level SSG converter. (b) BESG and ship engine. (c) Diesel auxiliary generator. (d) Measuring instruments.

A. Simulation

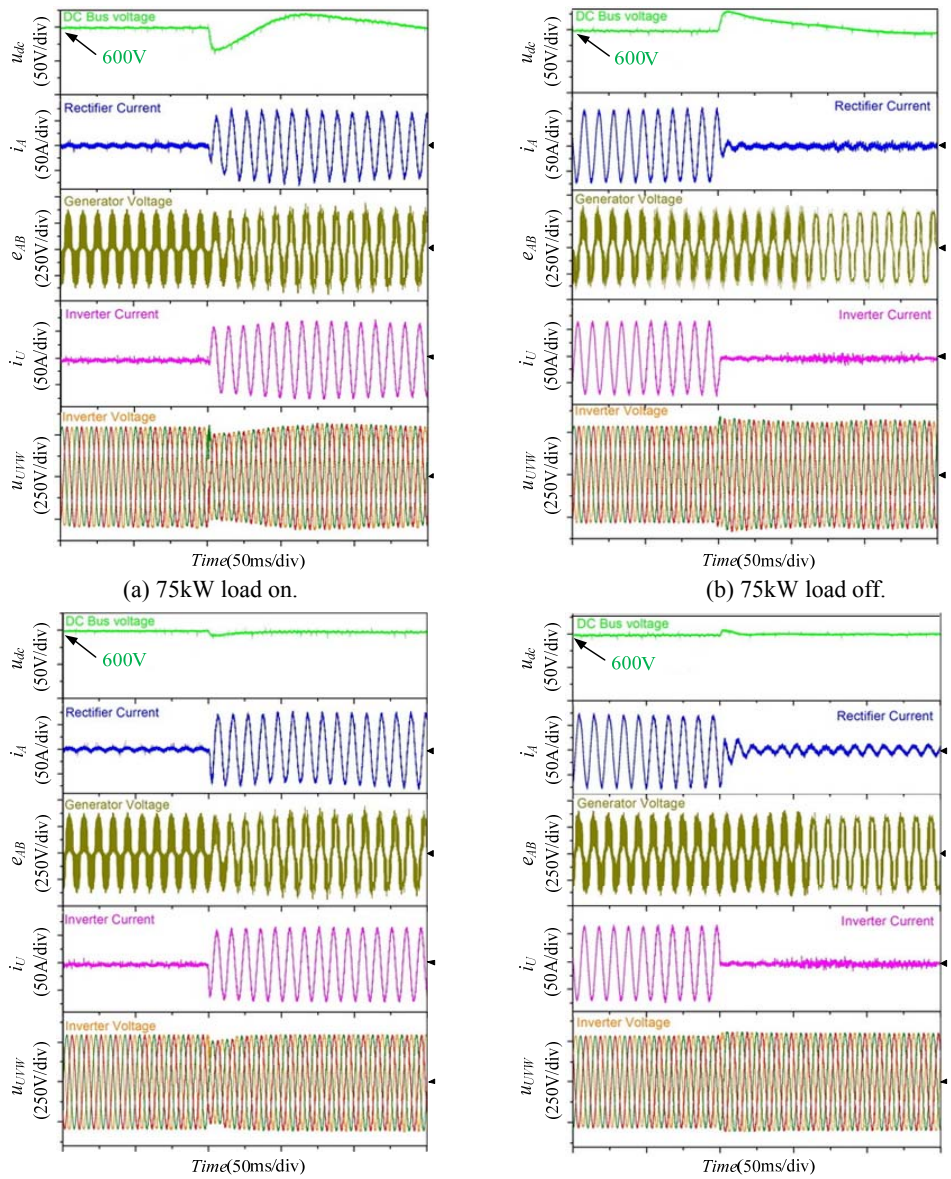
The simulation results of the conventional scheme, which is based on the voltage-oriented control with a PI controller and a DPLL [12], and the proposed scheme are compared in Fig. 18. The generator terminal voltage harmonics analysis with the THD is shown in Fig. 19. The simulation is a sudden load change process in which a resistive load is imposed at 1s and unloaded at 1.15s.

Fig. 18(a) adopts the conventional scheme and shows the transient response of the dc-link voltage, the generator current, the voltage phase, the active power and the reactive power in the entire process. The output phase angle of the DPLL is unstable for the distorted generator voltage. Due to the impact of the strong coupling on the current control-loop and the inaccurate output frequency of the DPLL, the response speed to the reference current is unsatisfactory and an overshoot is inevitable. The fluctuation extent of the dc-link voltage approaches 50V. As a result, the active power fluctuates greatly while the reactive power is not kept at zero.

On the other hand, Fig. 18(b) shows the adoption of the proposed quasi-DPC scheme. When compared to Fig. 18(a), it can be observed that the system dynamic-static performance has been significantly improved. After a very short transient, the generator current tracks its reference value with a high rapidity and stability. The fluctuation extent of the dc-link voltage is reduced to 6V which is much smaller than that in the conventional scheme. In addition, the active power is kept at a specific constant value while the reactive power is kept at zero. According to the comparative simulation results, fast power control is successfully achieved by the proposed quasi-DPC scheme.

B. The Prototype Experiment

The prototype of a 75kW T-type three-level SSG converter is developed based on a Texas Instruments' digital signal processer (DSP) chip TMS320F28335 and an Altera's complex programmable logic device (CPLD) chip EPM3032-AT144. Fig. 20 shows the hardware prototype,



(a) 75kW load on. (b) 75kW load off.

(c) 75kW load on. (d) 75kW load off.

Fig. 21. Experimental results of the load sudden change transient response with (a), (b) Conventional scheme, (c), (d) Proposed scheme.

including a T-type three-level SSG converter, a YOKOGAWA DL850 recorder, a brushless excite synchronous generator tied to the principal axis of a ship engine, a diesel auxiliary generator and a Tektronix's voltage/current probe. An Infineon FF600R12ME4 power module is selected, and the dead time is set to 2μs. For an objective analysis of the experiment results, the YOKOGAWA DL850 recorder is adopted to measure the voltages and currents on both side of the converter. The parameters of the experimental prototype are the same as those used in the simulation.

In order to test the dynamic performance of the proposed control scheme, load sudden change experiments are conducted in the inverter stand-alone operational mode. Due to the considerable load capacity, the rotor speed should be around 1500*rpm*, and the frequency of the ship shaft synchronous generator is approximately at 50Hz. The inverter output voltage (RMS) and its frequency are kept at constant values of 400V and 50Hz, respectively. The power of the resistive load is 75kW. Experimental results obtained with the conventional scheme and the proposed scheme are shown in Fig. 21. They are identical to the simulation. The transient response of the rectifier current with the proposed scheme is faster than that with the conventional scheme. The generator current with the proposed scheme tracks its reference value within five switching cycles (1ms). When the 75kW resistive load suddenly changes, the fluctuation extent of the dc-link voltage is kept within 60~65V by using the conventional control scheme [see Fig. 21(a) and (b)]. However, with the proposed scheme, the dc voltage fluctuation extent can be kept at 8~10V [see Fig. 21(c) and (d)]. The dc-link voltage reaches the reference value (600V) without an overshoot in

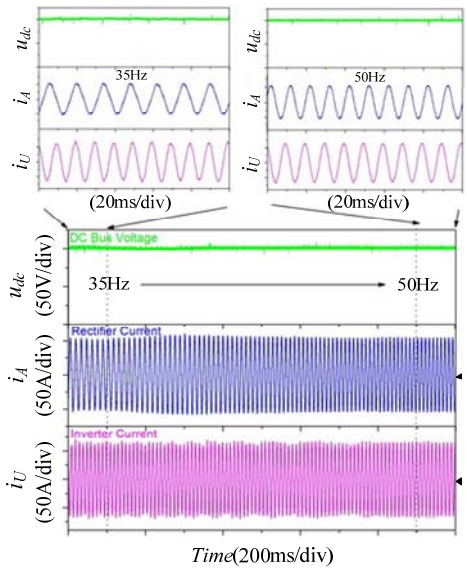


Fig. 22. Experimental results of proposed scheme with speed variation from 35Hz to 50Hz in 2s.

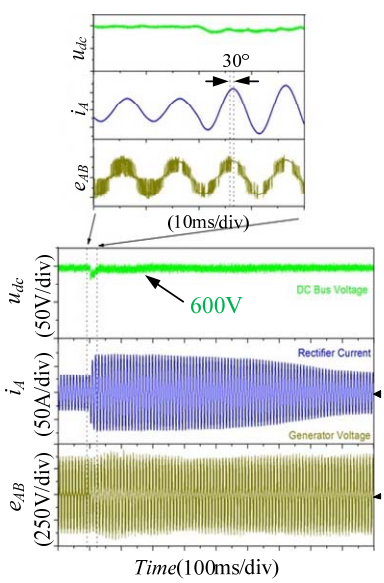
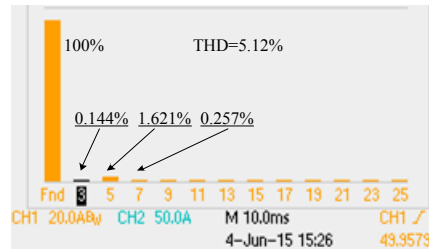


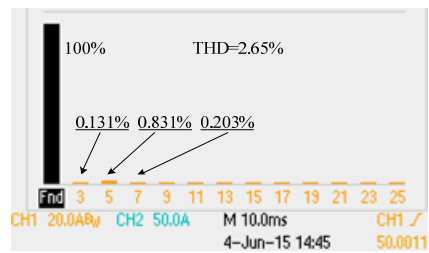
Fig. 23. Experiment on the 7.5kw ac motor load.

approximately 22ms. According to the waveforms of u_{UVW} and i_U in Fig. 21(a)-(d), by using the proposed scheme, the output voltage and the power response at the inverter side are much more stable than those with the conventional scheme. This indicates that the proposed control scheme can provide a fast power response and a fast current control. It also indicates that the dc-link voltage has an excellent robustness to power changes with a small voltage deviation. According to experimental results of a sudden change in load, the proposed scheme achieves the effect of quasi-direct power control.

An experiment on rotor speed variations is also conducted for testing the ship speed variation working conditions. Making the BESG operate at speed of 900 rpm (35Hz) with a 55kW load on the system, the speed increases linearly up to 1500 rpm (50Hz) in a 2s interval. The entire experiment



(a)



(b)

Fig. 24. Current THD at (a) generator side and (b) grid side.

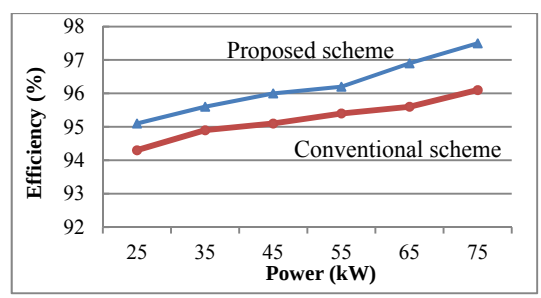


Fig. 25. System efficiency curve.

process and its partial waveforms are shown in Fig. 22. The experimental result show that the proposed scheme can adapt the changes in the frequency. The envelope curve of the generator current is kept at 115A when the frequency varies from 35Hz to 50Hz. This indicates that the proposed variable frequency phase locked loop can track the frequency and phase of the BESG precisely.

Fig. 23 shows an experiment on a 7.5kw ac motor load. Before the motor load direct starting, a 40kW resistive load is loaded on the system. From the figure, it can be seen that the same rapid dynamic response is presented upon the application of an ac motor load. The generator current is nearly sinusoidal and in the phase with the generator phase voltage (i.e. the generator power factor approaches 1).

Fast Fourier transform (FFT) analyses of the generator side current and grid side current with the proposed scheme are shown in Fig. 24. The THD of the generator side current is 5.12% while the THD of the grid side current is 2.65%. As a result, the harmonic characteristic and EMC of the entire generation system have been significantly improved, which perfectly meets the standards of vessel electronic power supplies. The efficiency of a T-type SSG converter with the conventional scheme and with the proposed scheme at each power scale is measured with a FLUKE 1725 power logger.

The system maximum efficiency is promoted to 97.5% with the proposed scheme with the full power scale application as shown in Fig. 25.

VI. CONCLUSION

This paper presents a novel fast instantaneous power control scheme for T-type Three-level SSG converters. A novel quasi direct power control is proposed, which adopts a resonant frequency adaptive PR controller with a variable frequency resonant PLL. The current control loop parameters have been designed by analyzing the frequency response characteristic and root locus trajectory in detail. The rotating transformation and strong coupling are both eliminated. To suppress the impact of a distorted generator voltage on the DPLL, a multi-resonant compensator is introduced into the modified RPLL. As a result, an accurate generator frequency is obtained to modify the PR controller's resonant frequency. This method provides a fast current dynamic response and promotes system robustness. According to the theory of instantaneous power balance, the load instantaneous power is fed forward to the dc-link voltage control loop to alleviate the burden on the voltage controller. As a result, a fast power response with a unity power factor is easily achieved by the proposed scheme. Moreover, all of the controllers are designed based on the predominant pole method with the required phase margin and steady-state error. The simulation and experimental results show that the proposed control scheme is feasible and valid for T-type three-level SSG converter systems.

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