

Natural Balancing of the Neutral Point Potential of a Three-Level Inverter with Improved Firefly Algorithm

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Abstract

Modern power systems driven by high-power converters have become inevitable in view of the ever increasing demand for electric power. The total power loss can be reduced by limiting the switching losses in such power converters; increased power efficiency can thus be achieved. A reduced switching frequency that is less than a few hundreds of hertz is applied to power converters that produce output waveforms with high distortion. Selective harmonic elimination pulse width modulation (SHEPWM) is an optimized low switching frequency pulse width modulation method that is based on offline estimation. This method can pre-program the harmonic profile of the output waveform over a range of modulation indices to eliminate low-order harmonics. In this paper, a SHEPWM scheme for three-phase three-leg neutral point clamped inverter is proposed. Aside from eliminating the selected harmonics, the DC capacitor voltages at the DC bus are also balanced because of the symmetrical pulse pattern over a quarter cycle of the period. The technique utilized in the estimation of switching angles involves the firefly algorithm (FA). Compared with other techniques, FA is more robust and entails less computation time. Simulation in the MATLAB/SIMULINK environment and experimental verification in the very large scale integration platform with Spartan 6A DSP are performed to prove the validity of the proposed technique.

Keywords: Firefly Algorithm, FPGA, Natural Voltage Balancing, NPC Inverter, Selective Harmonic Elimination

I. INTRODUCTION

The advantages of multilevel inverters (MLIs), such as improved power quality and design flexibility, with components of low voltage ratings to handle or produce high voltage levels and hence high power levels have resulted in the extensive use of these inverters in high-power applications [1]. The three well-known configurations of MLI are diode clamped, flying capacitor, and cascaded H bridge type multilevel inverters. Among them, the NPC inverter is used more often in the high-voltage industrial sector at the voltage range of 2.3 KV to 4.16 KV. Several applications of the NPC inverter can even handle voltages up to 6 KV [2]. Its compactness, efficiency, and good

performance make the NPC inverter useful in the drives industry.

The increasing demand for electrical power could be satisfied only with appropriately designed high-power converters. If these converters are operated at a high switching frequency, then the harmonic content could be reduced at the cost of high switching losses. However, strict power quality and high switching frequency should be maintained. If the system is power efficiency conscious, then a low switching frequency should be opted for. Selective harmonic elimination pulse width modulation (SHEPWM) is an efficient scheme with a switching frequency in the order of a small integer multiple of the fundamental frequency.

With SHEPWM, the strength of the dominant low-order harmonics is reduced drastically or nearly eliminated. Then, the high-order harmonics can be easily eliminated with small passive filters. To eliminate the low-order harmonics and improve the spectral with the required amplitude of the fundamental wave, a set of trigonometric Fourier series transcendental equations need to be solved. In addition, a set of switching angles need to be obtained. Such a set of

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nonlinear equations are traditionally solved with the Newton–Raphson (NR) method [3]-[5]. However, the NR method can be applied to continuously differentiable functions and requires an approximate but appropriate initial guess. Another drawback of the NR method is that it consumes much computation time and thus cannot be applied in real-time applications. Under such circumstances, several authors recommended and demonstrated that this problem can be regarded as an optimization problem rather than a deterministic algebraic problem so that optimally estimated switching angles can be obtained.

In addition to the estimation of the switching angles, an additional issue exists in the case of the NPC inverter. This issue is associated with the balancing of the DC voltages prevailing across the terminals of the split capacitors at the DC link. SHEPWM allows for natural balancing of the neutral point voltage because of symmetrical pulse patterns over a quarter cycle of the period.

The authors in [6] and [7] proposed a technique to achieve balancing of the DC voltage. In this technique, the switching angles are first estimated. Then, fine adjustment is incorporated into this solution set to address the balancing of the voltage across the DC link capacitors. The authors in [8] presented a six-level diode-clamped inverter for a standalone application that is powered by a photovoltaic unit. In [9], the performance of SHEPWM for NPC inverters was compared with that of three other PWMs. SHEPWM has also been used in voltage-source-converter-based drive applications with the aim of reducing the common-mode voltage [10]. Optimal switching angles for NPC inverters have been discovered by using the clonal selection algorithm [11].

Evaluation of switching angles by solving the SHE equations has been demonstrated by using other heuristic search algorithms, such as the genetic algorithm [12], differential evolution [13], particle swarm optimization [14], and the bee algorithm [15], for other types of MLIs.

In this study, a nature-inspired meta heuristic algorithm known as the self-adaptive improved firefly algorithm (FA) [17] is utilized to obtain optimum switching angles for the three-level neutral point clamped inverter. The original FA depends on its parameters, such as absorption coefficients (γ), attraction coefficient (β), and random movement factor (μ), which result in the attainment of local optima unless their values are properly selected. In the proposed FA, the value of μ is adaptively tuned in each iteration. A powerful mutation strategy is incorporated to improve performance and prevent convergence into any unexpected local minima. Hence, this method yields better results than the original FA.

The proposed methodology is validated in a simulation environment using MATLAB/SIMULINK. An experimental setup is also developed with a field-programmable gate array (FPGA) in the SPARTAN 6A DSP platform. Concurrent processing capability, calculation ability, flexibility, high-

integration density, processing speed, and dynamic reconfiguration in the hardware architecture during runtime make FPGA a proper solution for the implementation of the proposed PWM. In [18], variable common-mode injection PWM for a three-level inverter was implemented with FPGA. In the current work, FPGA is utilized to implement SHE. The experimental results validate the simulation results obtained.

II. NPC INVERTER TOPOLOGY

The NPC inverter has been applied in various industrial applications since its introduction in 1981. The topological arrangement of the three-phase three-level NPC inverter is shown in Fig. 1. In its basic form, the three-level three-phase NPC inverter has two DC link capacitors (C1 and C2) connected in series, and this section is connected across the main DC power source. Thus, the sourcing DC voltage is divided into three voltage levels, namely, $+V_{dc}/2$, 0, and $-V_{dc}/2$. These voltage levels appear at the output of each phase of the inverter through appropriate switching of the power semiconductor devices. Thus, the three phases of the inverter share a common DC bus. The middle point of the two capacitors is denoted as “0,” which is the neutral point. Two complementary switch pairs, namely, (Sa1, Sa1') and (Sa2, Sa2'), exist. Two clamping diodes (Da1, Da1') per phase are also present in this inverter. The two outer switches are the main switching devices (Sa1, Sa2') that operate for pulse width modulation, and the two inner switches are the auxiliary switching devices (Sa2, Sa1') that clamp the output terminal potential to the neutral point potential with the help of the two clamping diodes.

Table I shows the three states in terms of the voltage levels of a three-phase three-level inverter. The neutral point of the load is connected to the center point of the split DC link capacitors when the state is 0. During this period, current flows through the neutral line. This condition causes a capacitor to become discharged while the other is being charged. The average neutral current is zero, and the average neutral point voltage is also zero under normal operating conditions for a wide range of modulation indices. However, under transient conditions or under conditions of three-phase load imbalances, the average neutral current is no longer zero, and the neutral point voltage is subjected to variations. In a multilevel inverter with multiple DC link capacitors, the duration of contribution of electric power is not equally shared by all the capacitors over a cycle of a period because of the different periods of conduction of each switch.

III. SELECTIVE HARMONIC ELIMINATION

VSC topologies associated with SHEPWM provide high-quality output voltage. With SHEPWM, the power quality may be increased for utility-grade power electronic

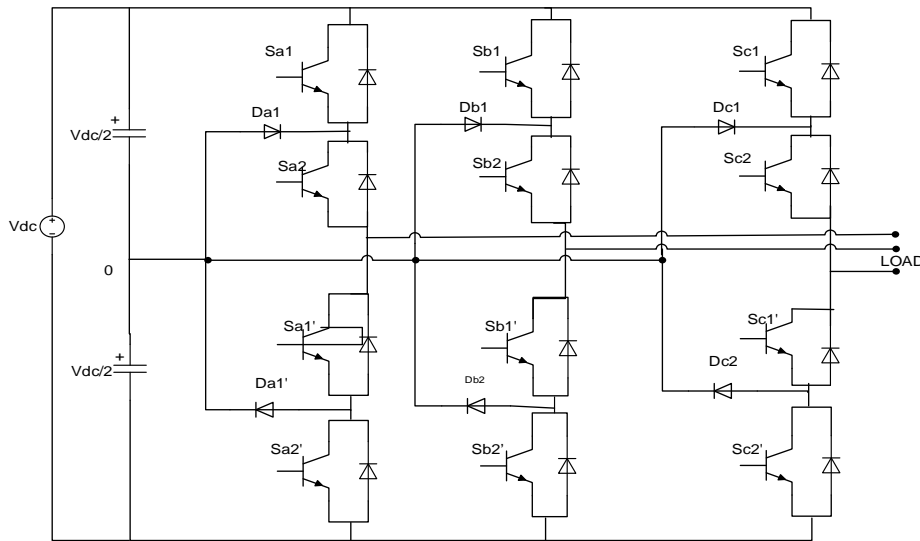


Fig. 1. Structure of three-level NPC inverter.

TABLE I

VOLTAGE LEVELS AND THE CORRESPONDING SWITCHING STATES OF THE INVERTER

Sa1	Sa2	Sa1'	Sa2'	Switching States	Output Phase Voltage
1	1	0	0	+	+V _{dc} /2
0	1	1	0	0	0
0	0	1	1	-	-V _{dc} /2

converters, such as those utilized in HVDC power transmission systems. Other modern and advanced static compensators (STATCOMs) belonging to the family of flexible alternating current transmission system (FACTS) technologies can also benefit from the SHEPWM strategy. VSC experiences higher switching losses because of PWM control compared with current-sourced solutions that use low-frequency line-commutated thyristors. Meanwhile, SHEPWM is considered as an optimum modulation scheme owing to its superior harmonic profile with minimum switching frequency. Selectively eliminating low-order harmonics does not immediately lead to overall improvement of the quality of the output voltage wave of the inverter. It basically pushes out the energy content in these harmonics toward high-order harmonics. Therefore, the total harmonic distortion (THD) of the SHEPWM-based inverter output voltage remains high until the high-order harmonics are also eliminated by filtering them with passive filters.

A. Mathematical Model of Switching

A three-level inverter line to neutral SHEPWM waveform is shown in Fig. 2. It has five switching angles, namely, α_1 , α_2 , α_3 , α_4 , and α_5 .

$$0 \leq \alpha_1 \leq \alpha_2 \leq \alpha_3 \leq \alpha_4 \leq \alpha_5 \leq \frac{\pi}{2} \quad (1)$$

Owing to the waveform characteristics of odd and half-wave

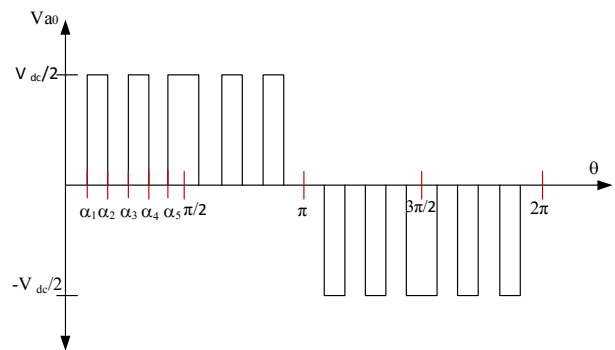


Fig. 2. Phase voltage waveform of the NPC inverter.

symmetry, the Fourier series expansion of the line to neutral voltage of phase leg “a” of the NPC inverter is

$$V_{ao} = \sum_{m=1}^{\infty} b_m \sin(m\omega t), \quad (2)$$

$$b_m = \begin{cases} 0 & \text{when } m \text{ is even} \\ \frac{2V_{dc}}{m\pi} \sum_{k=1}^N (-1)^{k+1} \cos(m \alpha_k) & \text{when } m \text{ is odd} \end{cases} \quad (3)$$

By properly computing the switching angles $\alpha_1, \dots, \alpha_n$, n number of harmonics can be eliminated. In this proposed work that uses five switching angles, four non-triplen harmonics (5th, 7th, 11th, and 13th order) can be eliminated as follows:

$$b_1 = \frac{2V_{dc}}{\pi} \sum_{k=1}^N (-1)^{k+1} \cos(\alpha_k),$$

$$b_5 = \frac{2V_{dc}}{5\pi} \sum_{k=1}^N (-1)^{k+1} \cos(5 \alpha_k) = 0,$$

$$b_7 = \frac{2V_{dc}}{7\pi} \sum_{k=1}^N (-1)^{k+1} \cos(7 \alpha_k) = 0,$$

$$b_{11} = \frac{2V_{dc}}{11\pi} \sum_{k=1}^N (-1)^{k+1} \cos(11 \alpha_k) = 0,$$

$$b_{13} = \frac{2V_{dc}}{13\pi} \sum_{k=1}^N (-1)^{k+1} \cos(13 \alpha_k) = 0. \quad (4)$$

$$A_0 = \frac{M \times 2V_{dc}}{\pi}, \quad (5)$$

where A_0 is the magnitude of the desired fundamental value and M is the modulation index. Notably,

$$0 \leq M \leq 1.$$

Solving the above nonlinear transcendental equations using iterative methods require a proper initial guess. Hence, self-adaptive improved firefly algorithm (SAIFA) is proposed to obtain optimum switching angles to eliminate specified non-triplen low-order harmonics and to obtain the desired fundamental value. Triplen harmonics need not be eliminated because they disappear as a result of the nature of the three-phase circuit.

IV. SAIFA

Most of the modern optimization algorithms are inspired by nature, and such algorithms are collectively known as metaheuristic algorithms. Among the 11 popular metaheuristic algorithms utilized for optimization, FA is the best in terms of execution speed when applied to a micro controller. FA, which is inspired by fireflies or lightning bugs, was developed by Yang [16]. Fireflies exhibit a peculiar behavior, which when modelled in a mathematical background leads to solutions in the optimization domain. The use of simple algebraic procedures is either time consuming or impossible in this domain.

The behavior of fireflies exhibits three advantageous rules. The first rule is that fireflies are unisex in nature. Being unisex, their attraction to each other in the pursuit of their movements are sex independent. The question of crossover is avoided, and this is an advantage over the genetic algorithm. The second rule is that each firefly is attracted to nearby and brighter fireflies; this condition occurs as a function of the distance between the individual firefly and the neighboring brighter one. An interesting feature of fireflies is that if they experience difficulty distinguishing flies with more brightness than their own, they tend to exhibit an apparently random motion. Their entire movement can be an ordered and governed one based on the parameters that can be sensed only by the flies but are not visible to human eyes (e.g., brightness of their light).

The third rule is that when realized as an optimization algorithm, the value of the objective function associated with each firefly is related to the brightness of the individual firefly. An appropriate fitness function is formulated in such a manner that will maximize the fundamental voltage and eliminate the low-order harmonics.

$$F(\alpha_1, \alpha_2 \dots \alpha_N) = (b_1 - A_0)^2 + b_5^2 + \dots b_n^2 \quad (6)$$

The essence of selective harmonic elimination is the estimation of a certain number of switching instants. In this study, SAIFA is proposed [17] to obtain the optimal switching instants. SAIFA is better than the original FA because SAIFA overcomes the tendency of FA to converge at the local minima. The inclusion of a new mutation

operator in SAIFA significantly enhances its performance.

A. Pseudo Code for the Implementation of Improved FA

We assign the constants of FA, namely, $\beta_{min}=0.2$, $\beta_{max}=1$, $\gamma=1$, $p=2$, and maximum number of iterations=200. The steps of the proposed algorithm are shown below.

Generate initial population of fireflies randomly, i.e., the switching angles

$\alpha_{m,firefly}^k = [\alpha_{m,1}^k, \alpha_{m,2}^k, \dots, \alpha_{m,N}^k]$ satisfying Eq. (1), where $m = 1, \dots, N_{firefly}$, $N = \text{no. of switching angles}$

Initialize maximum iteration (ite_max) as stopping criteria

Set initial iteration, $k=1$

While ($k < \text{ite_max}$)

 Compute light intensity (fitness value) for all fireflies using Eq. (6) and store the best fitness value in variable Gbest.

 For $m = 1, \dots, N_{firefly}$

 If $\text{minimum}(Gbest) < \text{fitness}(\alpha_{m,firefly}^k)$

 Calculate the distance r_{ij} and β using Eqs. (7) and (8)

$$r_{mn}^k = \|\alpha_{n,firefly}^k - \alpha_{m,firefly}^k\|$$

$$= \sqrt{\sum_{i=1}^N (\alpha_{n,firefly}^k - \alpha_{m,firefly}^k)^2} \quad (7)$$

$$\beta^k = (\beta_{max} - \beta_{min})e^{-\gamma(r_{mn}^k)^p} + \beta_{min} \quad (8)$$

 Adaptively tune μ using Eq. (9)

$$\mu^{k+1} = \left(\frac{0.5}{k_{max}}\right)^{1/k_{max}} \mu^k \quad (9)$$

 Update decision variables α_m^k using Eq. (10)

$$\alpha_{mod,firefly}^k = \begin{cases} \alpha_{m,firefly}^k + \beta^k (\alpha_{n,firefly}^k - \alpha_{m,firefly}^k) + \\ \mu^k |\alpha_{max} - \alpha_{min}| (\text{rand}_{1 \times N}(\cdot) - 0.5); \\ \text{if } FF(\alpha_{n,firefly}^k) < FF(\alpha_{m,firefly}^k) \\ \alpha_{m,firefly}^k; \text{ otherwise} \end{cases} \quad (10)$$

 Else

$$\alpha_{mod,firefly}^k = \alpha_m^k$$

 End if

 End for

// mutation operation

Evaluate mutant fireflies $\alpha_{m,mut}^k$ for N fireflies using Eq. (11)

$$\alpha_{m,mut}^k = \alpha_{q1,firefly}^k + \begin{pmatrix} \text{rand1}(\cdot)(1 - \text{rand2}(\cdot))(\alpha_{q2,firefly}^k - \alpha_{q3,firefly}^k) + \\ \text{rand3}(\cdot)(1 - \text{rand4}(\cdot))(Gbest^k - \alpha_{q4,firefly}^k) \end{pmatrix} \quad (11)$$

For $i = 1 \dots N_{firefly}$

$$\begin{cases} \alpha_{m,mutnew}^k = \alpha_{m,mut}^k; \text{ if } \text{rand1} < \text{rand2} \\ \alpha_{m,mutnew}^k = \alpha_{mod,firefly}^k; \text{ otherwise} \end{cases}$$

End for

Compute fitness value for $\alpha_{m,mutnew}^k$

// Selection operation

For $m=1 \dots N_{firefly}$

 If $\text{Fitness}(\alpha_{m,mutnew}^k) < \text{Fitness}(\alpha_m^k)$ then assign

$$\alpha_{m,firefly}^{k+1} = \alpha_{m,mutnew}^k$$

Else assign

$$\alpha_{m,firefly}^{k+1} = \alpha_{m,firefly}^k$$

Endif

End for

Compute fitness ($\alpha_{m,firefly}^{k+1}$) and update Gbest with minimum fitness value .

End while

Print the best firefly from Gbest as the optimal solution.

V. RESULTS AND DISCUSSION

A. Simulation Results

The application of FA in the natural balancing of the neutral point potential of the NPC inverter was developed as an *m* file in the MATLAB environment. The improved FA, after being developed in MATLAB, was run over 20 independent trials. The optimal switching angles for the modulation indices 0.6 and 0.8 were determined and tabulated in Table II. For the optimum switching angles, the harmonic spectrum pertaining to the output voltage of the inverter for the modulation indices (MI) of 0.6 and 0.8 is shown in Fig. 3 and 4.

The spectrum indicates that the amplitude of the fundamental value is as required for the given modulation indices. Harmonics up to the 13th order other than the triplen harmonics were eliminated.

The neutral current waveform for the modulation indices of 0.6 and 0.8 is shown in Fig. 5. This current slightly varies around zero because of nearly perfect balancing of the DC link capacitor voltages and because of the proper symmetrical switching scheme adopted in SHEPWM.

Table IV shows a comparison of THD for line and phase voltage THD as provided in [19] for the modulation indices of 0.5 and 0.9 with the three switching angles shown in Table III. The three methods considered for comparison are criteria-based modulation (CBM) [19], SHE using numerical method [3], and synchronous optimal pulse width modulation (SOPWM) [20]. The table shows that proposed method produces better results than the three other methods.

Fig. 6 and 7 show the harmonic spectrum for the line and phase voltage for MIs of 0.9 and 0.5, respectively, with three switching angles. The proposed method produces smaller THD values than the three other methods in addition to the elimination of 5th and 7th order harmonics. In the other three methods, these harmonics are much higher for the switching angles provided in [19] for the MIs of 0.5 and 0.9. Hence, the proposed method produces a globally optimum solution for the elimination of harmonics and THD.

B. Experimental Results

A suitable experimental hardware was fabricated with FPGA Spartan 6A DSP. For the digital control of power electronic converters, microcontrollers and DSPs are utilized

TABLE II
SWITCHING ANGLES FOR MI OF 0.6 AND 0.8

Sl. No.	MI	Switching Angles (degrees)				
		α_1	α_2	α_3	α_4	α_5
1.	0.8	18.30	48.15	53.35	82.19	87.36
2.	0.6	34.87	38.36	50.24	59.91	64.93

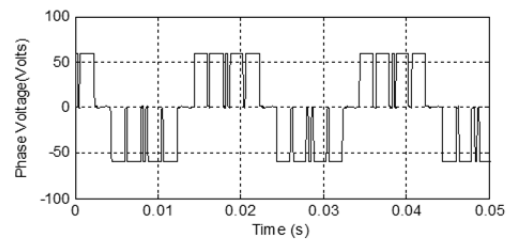
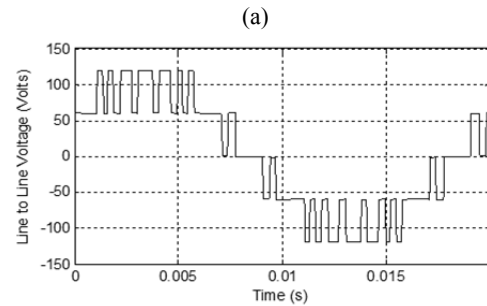
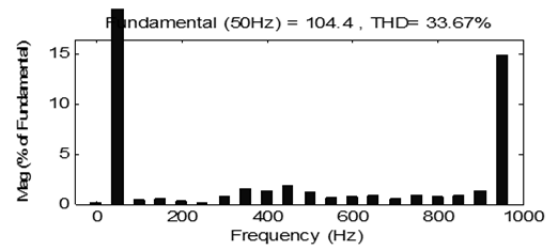
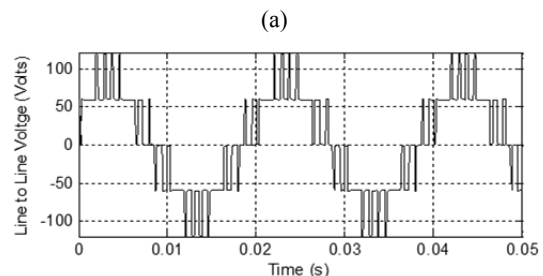
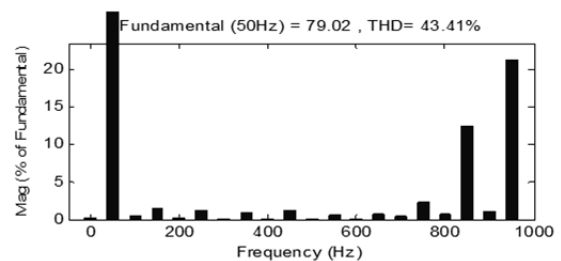


Fig. 3. (a) Harmonic spectrum. (b) Output line voltage. (c) Phase voltage waveform for modulation index of 0.8.



(b)

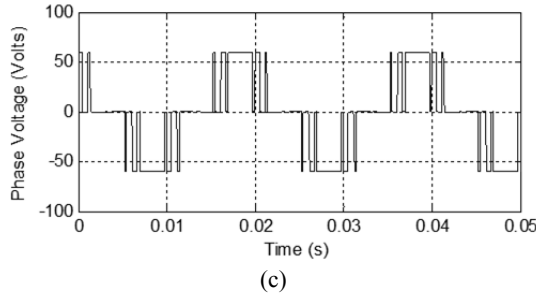


Fig. 4. (a) Harmonic spectrum. (b) Output line voltage. (c) Phase voltage waveform for MI of 0.6.

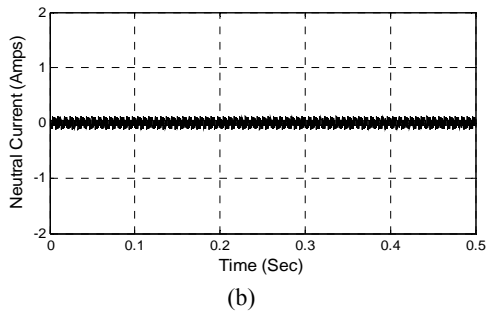
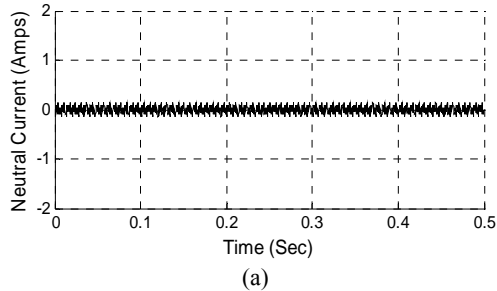


Fig.5. Neutral current for MI of (a) 0.8 and (b) 0.6.

TABLE III
SWITCHING ANGLES FOR MI OF 0.5 AND 0.9

MI	Switching angles obtained from the proposed method (in degrees)		
	θ_1	θ_2	θ_3
0.5	15.07	80.12	83.91
0.9	50.06	62.27	71.13

TABLE IV
THD COMPARISON OF LINE AND PHASE VOLTAGE FOR MI OF 0.5 AND 0.9

MI	Method	THD (%)	
		Phase Voltage	Line Voltage
0.9	CBM [19]	42.3	29.1
	SHE [3]	58.8	57.1
	SOPWM [20]	47.0	30.3
	Proposed Method	45.05	23.95
0.5	CBM [19]	98.4	60.5
	SHE [3]	105.4	81.6
	SOPWM [20]	112.0	71.6
	Proposed Method	86.81	47.37

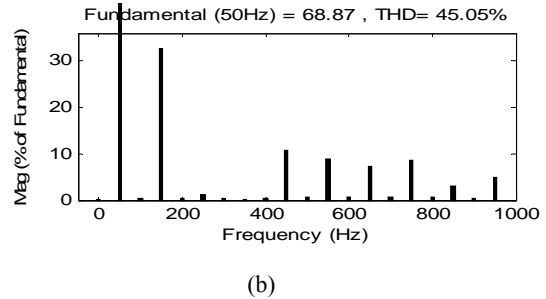
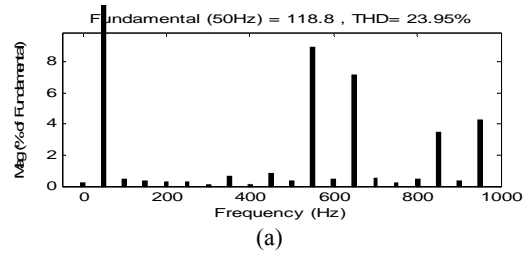


Fig. 6. (a) Line voltage spectrum. (b) Phase voltage spectrum for MI of 0.9 using the proposed FA.

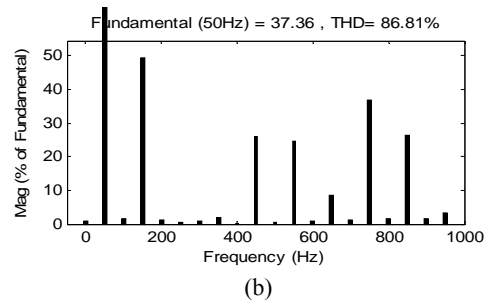
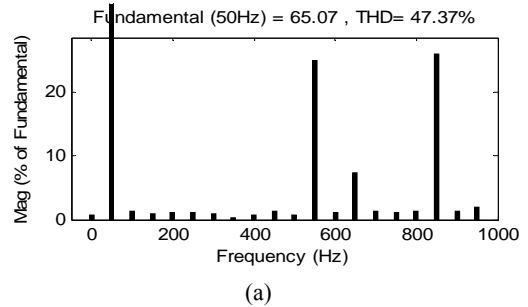


Fig. 7. (a) Line voltage spectrum. (b) Phase voltage spectrum for MI of 0.5 using the proposed FA.

when the number of PWM pulses generated are limited. Hence, FPGA is a good solution for the implementation of PWM algorithms in high-power converters.

1) *FPGA Controller*: The SPARTAN 6A DSP board generates the 12 required switching pulses for the 12 IGBTs used in the NPC inverter. The optimum switching angles obtained from FA offline were entered into the FPGA kit by using the user interface increment/decrement push buttons. Xilinx XC6SLX25 Spartan 6A DSP FPGA is the core of the system. It contains 24,051 logic cells, a 48 bit accumulator, 229 KB dynamic RAM, 38 DSP48A1 slices, and 52×18 Kb block random access memory (BRAM). The ISE12.1

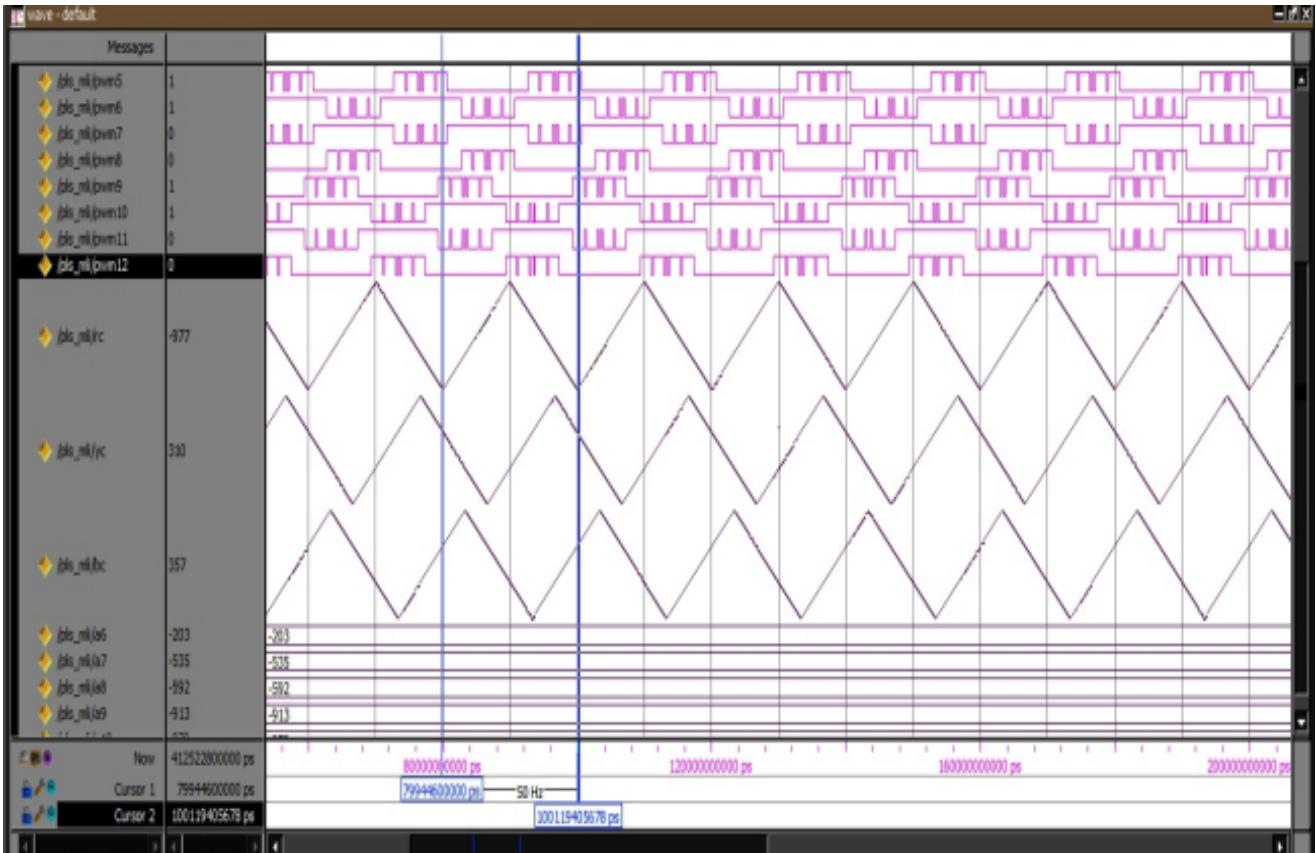


Fig. 8. Carrier waves phase shifted by 120° for the three phases of the NPC inverter.

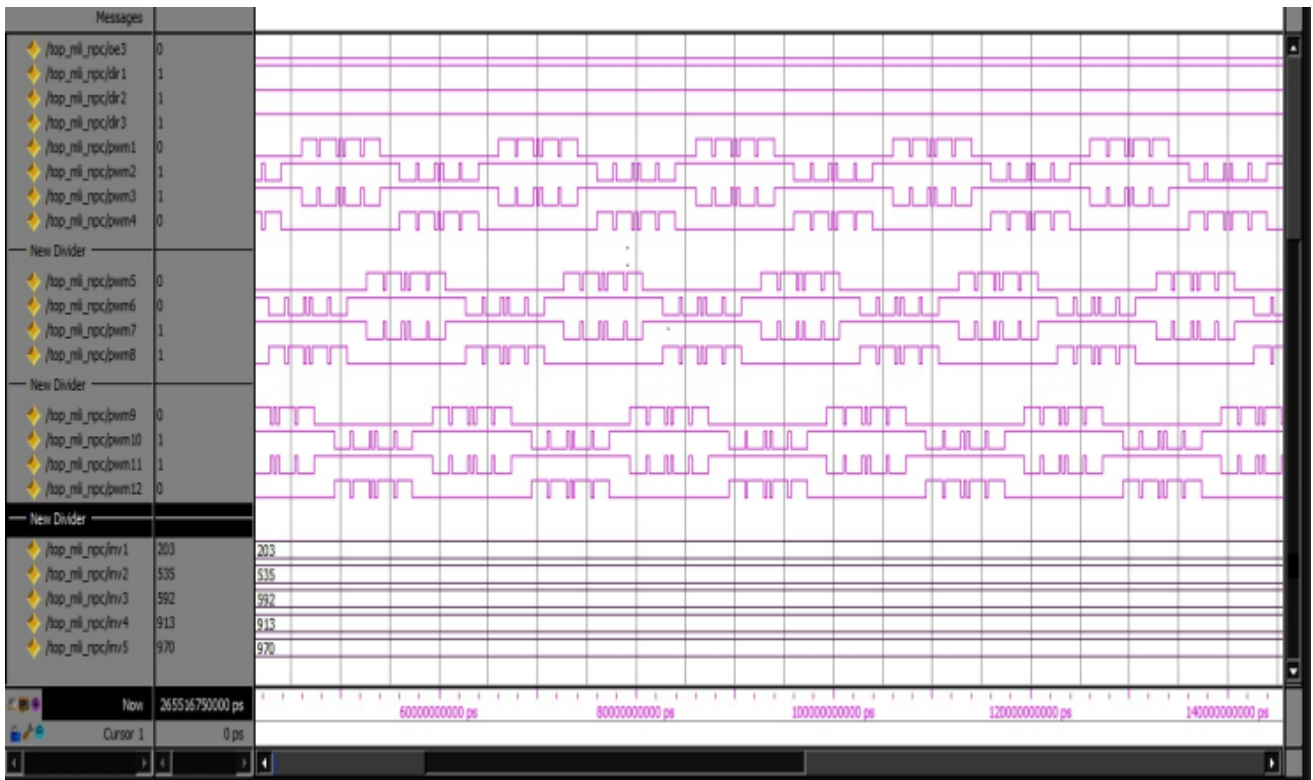


Fig. 9. Gating pulses generated for the 12 switches of the NPC inverter.



Fig. 10. Experimental setup of the proposed work.

TABLE V

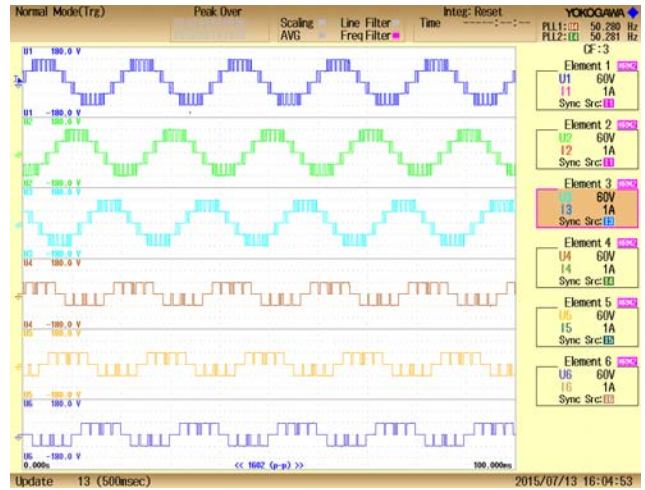
COMPARISON OF SIMULATION AND EXPERIMENTAL RESULTS OF INDIVIDUAL HARMONIC COMPONENTS AND THD

MI	V _{rms} (volts)	b ₅	b ₇	b ₁₁	b ₁₃	THD (%)
Simulation						
0.8	73.84	0.2	1.53	0.65	0.80	33.67
0.6	55.88	1.15	0.89	0.53	0.71	43.41
Experimental						
0.8	74	0.11	1.08	1.174	0.143	30.06
0.6	54.94	0.69	0.33	0.33	0.43	37.93

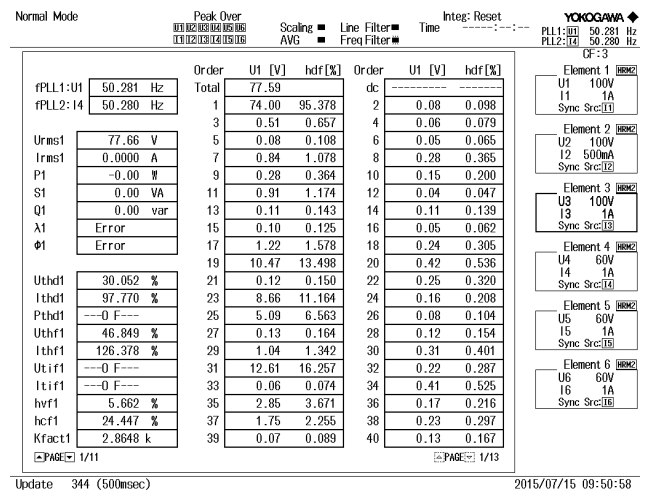
platform has been utilized to perform synthesis, placement, and routing operations. A 20 MHz external clock generator was used to generate the required clocking signal. The carrier generator was implemented in FPGA using an up-down counter. The counter counts from zero to the maximum value m and then counts down to zero. Thus, the triangular generator counts a total number of $2m$ in each half cycle of the output period. As the half cycle period is 0.01 s, the count $2m$ is calculated as $2m = \frac{20 \times 10^6}{100}$, which is equal to 200,000; count m is reduced to 1000.

Fig. 8 shows the three carrier waves with a phase shift of 120° generated for the three phases of the NPC inverter. The switching angles $\alpha_1 \dots \alpha_5$ are converted into constants using the conversion $\frac{\alpha \times 1000}{90}$ and then compared with the carrier waveform for generating gate pulses. Fig. 9 shows the gating pulses generated for the 12 switches of the NPC inverter.

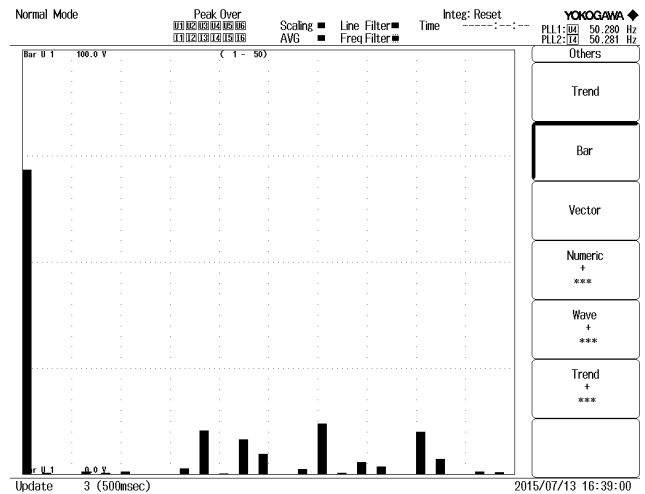
2) *Experimental Setup*: Fig. 10 shows the experimental setup of the three-phase three-level NPC inverter for the proposed algorithm. The power circuit of the NPC inverter consists of 12 IGBTs and 6 ultra-fast power diodes with a rating of 600 V/40 A. It has an input and output voltage rating of 300 V DC and 200 V AC, respectively. However, for the implementation, the input voltage provided is 120 V DC, and resistive load is connected at the output. Table V shows the



(a)

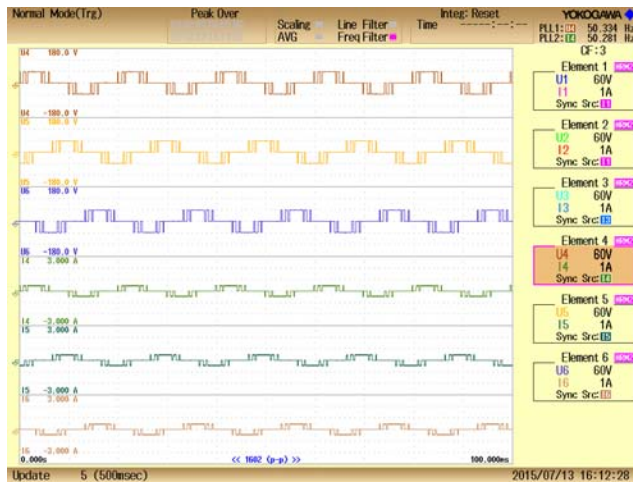


(b)

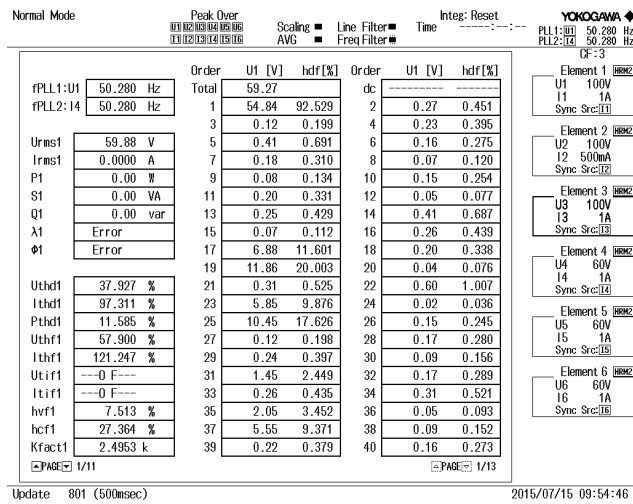


(c)

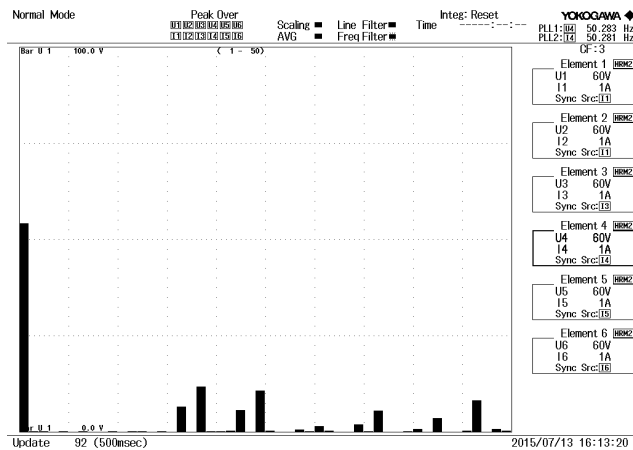
Fig. 11. (a) Output line and phase voltage waveform. (b) Individual harmonic component. (c) Harmonic spectrum of the three-level inverter for MI of 0.8.



(a)



(b)



(c)

Fig. 12. (a) Output line and phase voltage waveform. (b) Individual harmonic component. (c) Harmonic spectrum of the three-level inverter for MI of 0.6.

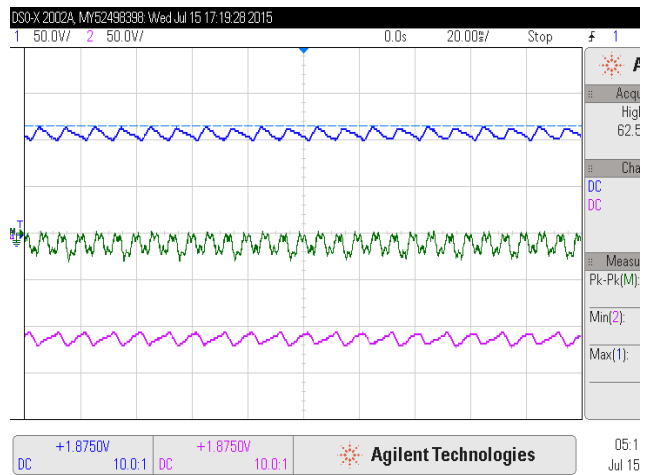


Fig. 13. Neutral point potential variation in the NPC inverter.

THD and individual harmonic components for the MIs of 0.8 and 0.6 obtained in both the simulation and hardware.

Table V proves that the experimental results agree well with those of the simulation and thus prove the validity of the proposed method. The experimental results measured with a Yokogawa power harmonic analyzer are shown in Fig. 11 and 12 for MIs of 0.8 and 0.6, respectively. The harmonic spectrum explicitly shows that non-triplen low-order harmonics up to the 13th order are eliminated at the output voltage.

Fig. 13 shows the two DC link capacitor voltages and the neutral point potential of the NPC inverter for MI of 0.8. The peak-to-peak neutral point voltage is 6.6 V for a DC input of 120 V and ± 10 V as reported in [21] for the same MI and DC input using variable common mode injection PWM. These results prove that in the proposed method, natural balancing of the neutral point potential is achieved because of the optimum switching pattern.

VI. CONCLUSION

An improved FA was developed, and its capability to determine the switching angles required for selective harmonic elimination in a three-level NPC inverter was demonstrated. Aside from rendering the required amplitude of the fundamental voltage, the proposed methodology also achieves the balancing of the voltages across the capacitors of the DC link. With regard to the extended application of the proposed scheme, it can be utilized in converter blocks on either sides of HVDC links. Various FACTS devices, such as STATCOM and SSSC, can be configured in the NPC inverter using the proposed technique. FA is as good as other optimization algorithms but has the additional advantages of fast convergence toward a robust solution and easy implementation in MATLAB. The simulation and experimental verifications proved the effectiveness of the proposed approach.

REFERENCES

- [1] I. Colak, E. Kabalci, and R. Bayindir "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, Vol. 52, No. 2, pp. 1114-1128, Feb. 2011.
- [2] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama "A survey on neutral point clamped inverters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.
- [3] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part I – Harmonic elimination," *IEEE Trans. Ind. Appl.*, Vol. IA-9, No. 3, pp. 310-317, May/June. 1973.
- [4] W. Fei, Y. Zhang, and X. Ruan, "Solving the SHEPWM nonlinear equations for three-level voltage inverters based on computed initial values," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, pp. 1084-1088, 2007.
- [5] W. Fei, X. Ruan, and B. Wu, "A generalized formulation of quarter-wave symmetry SHE-PWM problems for multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 24, No. 7, pp. 1758-1766, Jul. 2009.
- [6] S. R. Pulikanti, M. S. A. Dahidah, and V. G. Agelidis, "Voltage balancing control of three-level active NPC converter using SHE-PWM," *IEEE Trans. Power Del.*, Vol. 26, No. 1, pp. 258-267, Jan. 2011.
- [7] S. R. Pulikanti, G. Konstantinou, and V. G. Agelidis, "DC link voltage ripple compensation for multilevel active neutral point-clamped converters operated with SHE-PWM," *IEEE Trans. Power Del.*, Vol. 27, No. 4, pp. 2176-2184, Oct. 2012.
- [8] E. Ozdemir, S. Ozdemir, and L. M. Tolbert, "Fundamental-frequency-modulated six-level diode-clamped multilevel inverter for three-phase stand-alone photovoltaic system," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 11, pp. 4407-4415, Nov. 2009.
- [9] K. Lee and G. Nojima, "Quantitative power quality and characteristic analysis of multilevel pulsewidth-modulation methods for three-level neutral-point-clamped medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, Vol. 48 No. 4, pp. 1364-1373, Jul./Aug. 2012.
- [10] Y. Zhang, Z. Zhao, and J. Zhu, "A hybrid PWM applied to high power three-level inverter-fed induction-motor drives," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 8, pp. 3409-3420, Aug. 2011.
- [11] H. Lou, C. Mao, D. Wang, and J. Lu, "PWM optimisation for three-level voltage inverter based on clonal selection algorithm," *IET Electr. Power Appl.*, Vol. 1, No. 6, pp. 870-878, Nov. 2007.
- [12] K. El-Naggar and T. H. Abdelhamid, "Selective harmonic elimination of new family of multilevel inverters using genetic algorithms," *Energy Convers. Manag.*, Vol. 49, No. 1, pp. 89-95, Jan. 2008.
- [13] A. M. Amjad, Z. Salam, and A. M. A. Saif, "Application of differential evolution for cascaded multilevel VSI with harmonics elimination PWM switching," *Int. J. Electrical Power and Energy Systems*, Vol. 64, pp. 447-456, Jan. 2015.
- [14] K. Shen, D. Zhao, J. Mei, L. M. Tolbert, J. Wang, M. Ban, Y. Ji, and X. Cai, "Elimination of harmonics in a modular multilevel converter using particle swarm optimization based staircase modulation strategy," *IEEE Trans. Industrial Electron.*, Vol. 61, No. 10, pp. 5311-5322, Oct. 2014.
- [15] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia, and S. H. Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 27, No. 4, pp.635-646, Apr. 2012.
- [16] X. S. Yang, *Nature-Inspired Metaheuristic Algorithms*, Luniver Press, 2008.
- [17] T. Niknam, R. Azizipناه- Abarghooee, and A. Roosta "Reserve constrained dynamic economic dispatch: A new fast self-adaptive modified firefly algorithm," *IEEE Syst. J.*, Vol. 6, No. 4, pp. 635-646, Dec. 2012.
- [18] S. Nageswari and V. S. Kumar, "Field programmable gate array implementation of variable common mode Injection PWM for three-level inverters," *Computers and Electrical Engineering*, Vol. 40, No. 4, pp.1238-1258, May 2014.
- [19] J. Kfir, Dagan, and R. Rabinovici, "Criteria-based modulation for multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 30, No. 9, pp. 5009-5018, Sep. 2015.
- [20] A. Rathore, J. Holtz, and T. Boller, "Synchronous optimal Pulse width modulation for low-switching-frequency control of medium-voltage multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2374-2381, Jul. 2010.
- [21] S. Nageswari and V. S. Kumar, "VCMIPWM scheme to reduce the neutral-point voltage variations in three-level NPC inverter," *IETE Journal of Research*, Vol. 60, No. 6, pp. 396-405, Nov. 2014.



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