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A Hardware-in-the-loop Platform for Modular Multilevel Converter Simulations

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Abstract

In this paper, a hardware-in-the-loop simulation platform for MMCs is established, which connects a real time digital simulator (RTDS) and a designed MMC controller with optical fiber. In this platform, the converter valves are simulated with a small time step of 2.5 microsecond in the RTDS, and multicore technology is implemented for the controller so that the parallel valve control is distributed between different cores. Therefore, the designed controller can satisfy the requirements of real-time control. The functions of the designed platform and the rationality for the designed controller are verified through experimental tests. The results show that different modulation modes and various control strategies can be implemented in the simulation platform and that each control objective can been tracked accurately and with a fast dynamic response.

Key words: Hardware-in-the-loop simulation, MMC controller, Modular multilevel converter, Multicore technology

I. INTRODUCTION

High Voltage Direct Current (HVDC) transmission based on a MMC (modular multilevel converter) has become one of the most attractive VSC-HVDC technologies because of its modularity and scalability [1]-[3]. MMC-HVDC has a lot more advantages than two-level or three-level VSC-HVDCs, such as lower harmonic components at the Alternating Current (AC) side of the converter [4], greater reduction of the switching frequency, fewer losses [5] and operation consistency for the switching devices in series in an arm is not necessary [6]. There has been extensive research on MMC systems, and most of this research has been concentrated on mathematical modeling [7]-[9], modulation mode [10]-[12], and control strategies [13]-[16]. Physical verification plays an important role in testing control devices, planning the primary system and engineering operation, since it is closer to the practical project.

In order to obtain a large power capacity, high redundancy, and low total harmonic distortion (THD), a single MMC station with hundreds of voltage levels generally consists of thousands of sub-modules. It is difficult to establish a MMC primary system with a large number of sub-modules for simulation, especially for experimental verifications based on real physical devices.

Most of the physical primary systems mentioned in the existing literature are for 2 to 17 levels [12], [17]-[19]. In [20]-[21], 40 to 49 level prototypes drastically improve the ability of physical verification, while this achievement is based on reductions of the voltage value. Furthermore, the number of voltage levels is still much smaller than that in actual projects such as the Trans Bay Cable project, which has more than 200 levels. Additionally, for a large-power MMC controller, it is a big challenge to transmit massive capacitor voltages, trigger signals and then accomplish the large amount of computations caused by the balancing control.

Considering the problems existing in the realization of a MMC primary system and controller, a hardware-in-the-loop simulation platform for MMCs is established between a RTDS simulator and a physical MMC controller, in which the primary system is simulated in the RTDS and the control task is

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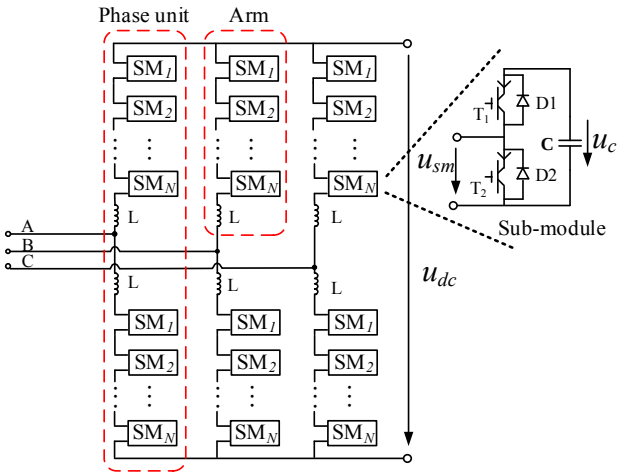

Fig. 1. The topology of MMC-HVDC converter.

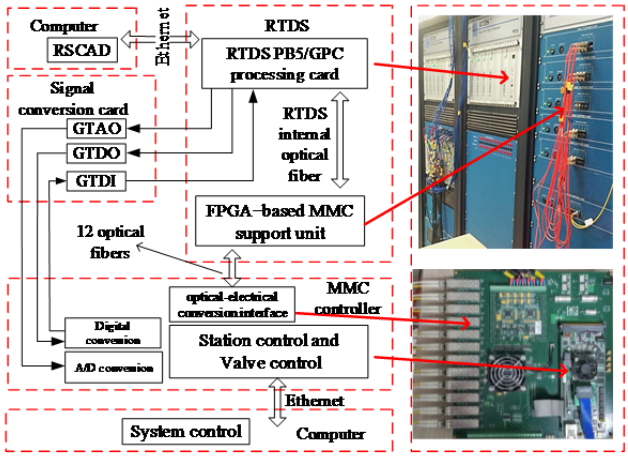

Fig. 2. The structure of the Hardware-in-the-Loop Simulation Platform for MMC.

performed on the designed physical controller. There are several advantages to the proposed hybrid simulation platform. First, it can precisely simulate the characteristics of a MMC system in a real-time digital simulator and it can conveniently simulate different types of faults on the AC side and DC side. Second, different control strategies can be implemented and tested to determine the physical controller flexibly. In addition, in the real-time digital simulator, the converter station can be connected into a large power grid, which is able to provide test circumstances similar to practical operating conditions. Third, the platform can be easily utilized for the design of the primary system and for tests of the control system.

On this platform, the converter valves are simulated with a small time step of 2.5 microsecond, which makes it qualified for high precision simulation of a MMC system with hundreds of voltage levels. By adopting an 8-core DSP and distributing the parallel valve control between different cores, the designed controller meets the requirements of real-time control calculation. In this paper, several experiments have been implemented on this hardware-in-the-loop platform. First, steady state experiments are carried out to verify the rationality of the established platform and its ability to test different control strategies. Second, DC loop current suppressing experiments are performed to verify the effect of suppressing control. Third, the dynamic performance of the designed controller is examined by power and voltage step experiments. Finally, a single phase to ground fault experiment is carried out to validate the ability to simulate faults on the designed platform.

The remaining parts of this paper are organized as follows. Section II briefly introduces the topology of the MMC. The configuration information of the hardware-in-the-loop simulation platform is detailed in Section III. The principle of the designed controller and the adopted control strategies are described in section IV. Several steady and transient experiments are presented in section V, and section VI draws conclusions.

II. Topology of an MMC

The topology of an MMC-HVDC converter is shown in Fig. 1. It is composed of six arms. For an MMC system with (N+1) levels, each arm consists of N sub-modules (SMs) and an arm reactor L. Each phase has two arms: an upper arm and a lower arm. The IGBTs of the SMs are triggered by the control system to form a multilevel, near-sinusoidal stepped waveform at the converter AC side by inserting the capacitor voltages of the corresponding SMs.

III. Configuration of the Platform

Two main parts make up the experimental platform as shown in Fig. 2. One is the RTDS simulator on which the primary system is simulated, and the other is the designed MMC controller which is connected to the RTDS by optical fibers. A computer running RSCAD is connected to the RTDS simulator by Ethernet, and the RSCAD is a graphical user interface for driving the RTDS simulator. It can be used to monitor the converter system. The system controller is interconnected to the MMC controller through Ethernet, whose functions are human-computer interaction, parameter adjustment, and the issue of system instructions.

The AC part of the primary system is simulated in the RTDS PB5/GPC processing board and the MMC converter is simulated in the FPGA-based MMC support unit. The operating data of the AC system and the control signals of the breakers are transmitted by a signal conversion card. The operating data and the trigger signals of the MMC station are transmitted by optical fibers.

The FPGA-based MMC support unit platform is implemented on a Xilinx ML-605 FPGA board. On this board, a Virtex 6 family chip is used which features 240k logic cells, 14-kb block RAM, 768 DSP48 blocks, and 24-Gb transceivers GTX providing up to a 6.6-Gb/s data rate. It is found that three

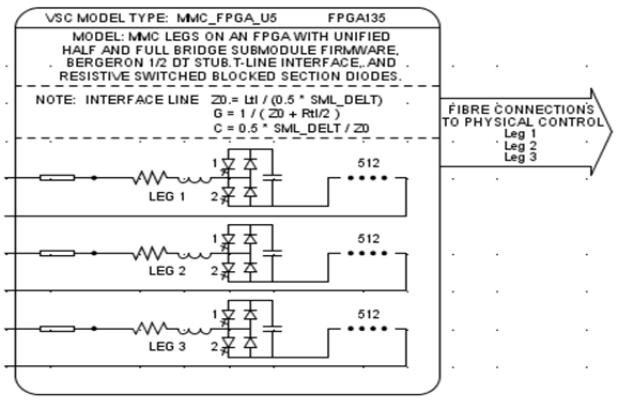

Fig. 3. The component of rtds_vsc_FPGA_U5.

separate valve models, each containing 512 SMs, can be simulated on a single FPGA with a small time step of 2.5 microsecond [22]. The typical drawback of using FPGA-based hardware for computation in simulation is the need to re-synthesize the FPGA layout whenever the computation requirements change. Fortunately, the RTDS simulator avoids this time-consuming re-synthesis requirement while allowing the user to change the type of SM (half or full), the number of SMs, the SM capacitor size, the SM discharge time-constant, and all of the other parameters. This tremendously improves the simulation efficiency.

The valve model component MMC_FPGA_U5 running on the FPGA-based MMC support unit is shown in Fig. 3.

The single MMC station consists of two components: three-phase upper arms and three-phase lower arms. For the MMC_FPGA_U5 component, some internal faults can be simulated including reactor turn-to-turn faults, capacitor shorting faults, partial loss of capacitor faults, and short faults between two points of the valve.

IV. Design of the MMC Controller

A. The Structure of the MMC Controller

In this paper, a controller is designed according to the requirements of the MMC control strategy and the interfaces of the RTDS simulator. The structure of the MMC controller is presented in Fig. 4. It can be divided into three layers: system control, station control, and valve control.

In Fig. 4, u_r denotes the modulation wave. The subscripts a, b and c represent abc phases, respectively. The subscript p and n represent the upper and lower arms, respectively. u_s is the AC side voltage. i_s is the AC side current, and u_c is the capacitor voltage of the corresponding SM.

The system control and man-machine interface of the controller are implemented on a computer, and connect with next layer controller by the Ethernet interface. The function of the system control is to ensure that the converter system switches smoothly between different operating modes and different operating points. Under normal conditions, the

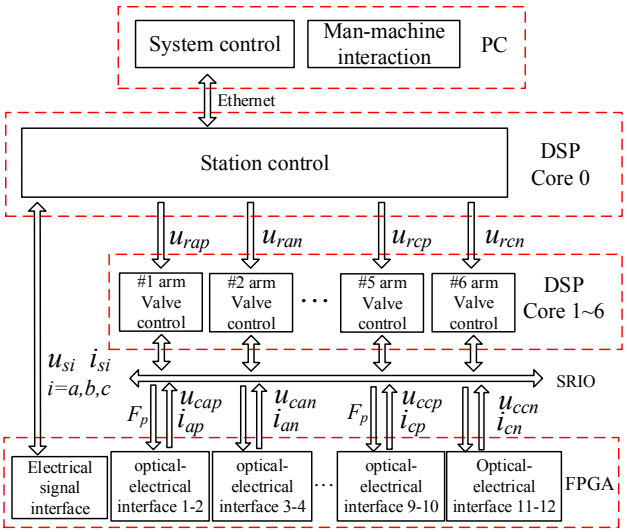

Fig. 4. The structure of MMC controller.

operating instructions issued by the dispatcher are not directly used as input reference values of the station controller. To improve the reliability of the system, the operating instructions should be preprocessed by corresponding strategies to avoid overshooting. In addition, the man-machine interface is in charge of adjusting the parameters of the controller, as well as monitoring the key variables and the other needed parameters.

The station control receives the reference values from the system control, and generates the modulation waves u_{rij} ($i=a$, b, c, $j=p$, n) of the six arms. The mission of the valve control is to receive the modulation wave produced by the station control, then creating the firing pulse words of the sub-modules through an appropriate modulation method, and balancing the capacitor voltages of the sub-modules. Because the valve controls of the six arms are independent from each other, parallel technology is adopted to enhance the computational efficiency. A Keystone infrastructure 8 core DSP produced by TI corporation is used in this paper, where the 0th core is in charge of the station control and circulating current suppression and the 1st~6th cores are in charge of the valve controls of the six arms separately. By utilizing this parallel structure, the calculation efficiency of the controller can be improved, and the data between station and the valve control can be flexibly transmitted in the DSP. A main-auxiliary type communication structure between cores is designed in this paper to transmit data between the station control and the valve controls. After finishing the station control computation, the main core is communicated with the auxiliary cores (1st~6th cores) through inter-core interruption and inter-core registers. As a result, the modulation wave of each arm will be transmitted into the corresponding auxiliary cores. The auxiliary cores only take responsibility for independent valve control calculation, and there is no communication between the valves.

The voltage and current at the AC side are outputted as a

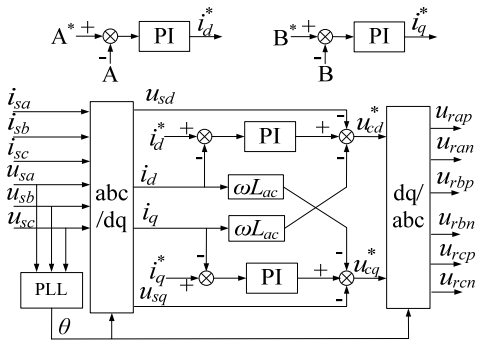

Fig. 5. Station control.

-10~10V analog signal from the RTDS to the controller through a GTAO card, and the controller drives the A/D chips to sample the analog signal by the FPGA. The A/D chip features 16-bit conversion and supports sample rates up to 250ksps per channel. The status signals of the breakers at the AC side are outputted as 0 or 5V electrical signal from the RTDS to the controller through the GTDO card. After voltage conversion, the signal of the breaker status is detected and identified by the FPGA. Moreover, the breaker control signals are converted to 0 or 5V electrical signal by the FPGA, which drives the GTDI card to control breakers.

The capacitor voltage of the sub-modules u_{cij}, the arm current i_{ij} and the trigger signal F_p are transmitted by optical fibers. The controller finishes fiber-optic communication by driving the optic-electrical conversion module. Each arm has two fibers, which use the Aurora communication protocol. The transmission speed is 2.0Gbit/s.

In order to realize data communication between the DSP and the FPGA, a Serial Rapid I/O interface is adopted in this paper, in which 4 full-duplex ports together constitute the 4x mode series protocol and each port's baud rate is 2.5Gbps.

B. The Station Control Strategies

In this paper, traditional direct current control based on a PI regulator is used as the inner loop control method. In the form of *dq* coordinates, dynamic models of the converter are shown in (1).

$$L_s \frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} u_{sd}-u_{cd} \\ u_{sq}-u_{cq} \\ u_{s0} \end{bmatrix} - R\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} 0 & -\omega L_s & 0 \\ -\omega L_s & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \quad (1)$$

where L_s is the ac equivalent inductance. i_d, i_q and i_0 represent the *dq0* components of the AC current respectively. u_{sd}, u_{sq} and u_{s0} represent the *dq0* components of the point of common coupling (PCC) voltages. u_{cd} and u_{cq} represent the reference *dq* components of the converter voltages. *R* denotes the equivalent resistor of the arm, and ω is the angular frequency of the system.

In the steady state, the zero-axis components and the arm equivalent resistor can be ignored. Then, (1) can be simplified as (2).

$$\begin{aligned} L_s \frac{di_d}{dt} &= u_{sd} - u_{cd} - \omega L_s i_q \\ L_s \frac{di_q}{dt} &= u_{sq} - u_{cq} - \omega L_s i_d \end{aligned} \quad (2)$$

Equation (2) shows that i_d and i_q are inter-coupling. As shown in Fig. 5, a double closed-loop controller is used as the station control strategy in this paper.

The outer loop control aims to generate i^*_d and i^*_q denoting the reference *dq* components of the AC currents. In this paper, PI controllers for active power control, reactive power control and DC voltage control are used as the outer loop control. The inner loop control aims to generate u^*_{cd} and u^*_{cq} denoting the reference *dq* components of the converter voltages according to the output of the outer loop control. In this paper, the conventional direct current control based on PI regulators is used as the inner loop control. In Fig. 5, A^* and A represent the reference value and the measured value of the active power or DC voltage, respectively. B^* and B represent the reference value and the measured value of the reactive power, respectively.

C. Modulation and Capacitor Voltage Balancing

The two widely used modulation strategies, NLM [23] and CPS-SPWM [12], are adopted in this paper.

The principle of the NLM method is simple, and it has been applied on several practical engineering projects. The balancing voltage control based on NLM needs to sort all of the capacitor voltages. In each trigger circle, the sub-modules with lower voltages are charged, and the sub-modules with higher voltages are discharged. This principle can make the capacitor voltages of the sub-modules tend to be coincident. However, the switching frequency of IGBTs is very high because the frequently sorting makes the sub-modules switch continually. In addition, it takes a large amount of time to sort the large number of capacitor voltages in a MMC controller. In order to strike a balance between the switch frequency and the SM voltage ripple, several improved NLM methods have been proposed [24]-[26], which are able to reduce the switch frequency to a certain extent.

The advantage of CPS-SPWM is a lower switching frequency, and the switching frequency is basically double the carrier frequency f_c. However, the capacitor voltage of each sub-module is controlled individually in CPS-SPWM, and the number of voltage balancing controller is the same as the number of sub-modules.

Consequently, the two mentioned modulation methods possess both merits and demerits, and CPS-SPWM is rarely applied to MMC systems with a large number of levels. In order to study the effects of the two modulation methods working on MMC systems with a large number of levels, in this paper, the two modulation methods are implemented on the designed controller, and the controller is able to switch between the two modulation methods expediently.

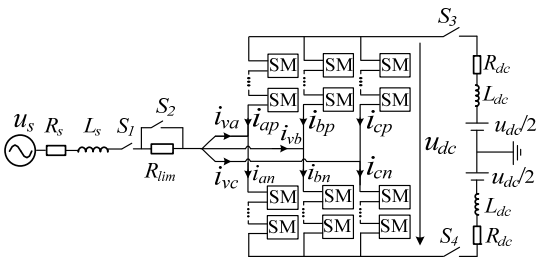

Fig. 6. Main circuit of test MMC system.

TABLE I
MAIN CIRCUIT PARAMETERS OF THE MMC SYSTEM

Parameters	Symbol	Value
Rated voltage of AC system	u_s	110 kV (L-L,RMS)
Resistor of AC system	R_s	0.314 Ω
Inductor of AC system	L_s	0.001 H
Equivalent resistor of DC line	R_{dc}	0.15 Ω
Equivalent inductor of DC line	L_{dc}	0.025 H
Current limiting resistor	R_{lim}	15 Ω
Rated DC voltage	u_{dc}	200 kV
SM capacitor	C	3000 uF
Arm inductor	L	0.004 H
SM number per arm	N	100
Rated SM voltage	u_c	2 kV

V. EXPERIMENTAL VERIFICATION

A. Experimental Environment

Several experiments are conducted to test the performances of the controller and the ability of the platform. Considering that only one MMC controller is used in this hardware-in-the-loop simulation platform, the experimental primary system includes only one single converter station as shown in Fig. 6.

When the control objectives are the active power and reactive power, the breaker S_3 and S_4 are closed, and the DC voltage is supported by two DC voltage sources. When the control objectives are the DC voltage and reactive power, the breaker S_3 and S_4 are opened, and the DC side is an open circuit. The positive direction of the arm current, the AC current, and the DC voltage are shown in Fig. 6. The DC loop current of phase A is defined as (3).

$$i_{acir} = \frac{i_{ap} + i_{an}}{2} \tag{3}$$

As shown in Fig. 6, the single MMC converter station is built in a RTDS simulator. The parameters of the main circuit are detailed in Table I.

B. Steady States Experiments

Two steady state experiments are carried out: one is for the NLM method and the other is for the CPS-SPWM method. In these two experiments, S_3 and S_4 are closed and the control objectives of the station control are the active power and the reactive power. The reference value of the active power is 400MW, the reference value of the reactive power is 30MVar and the carrier frequency is 200Hz.

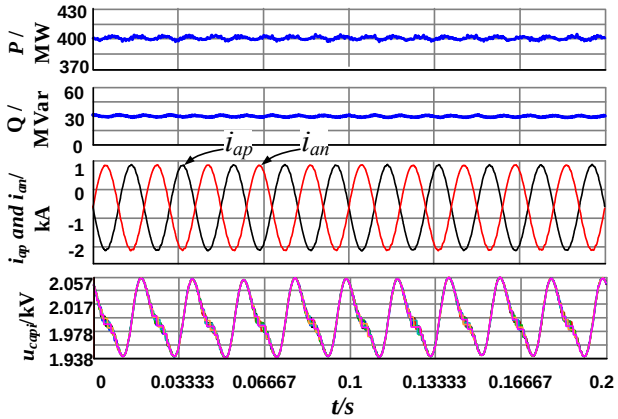

Fig. 7. Steady state experiment result with NLM method.

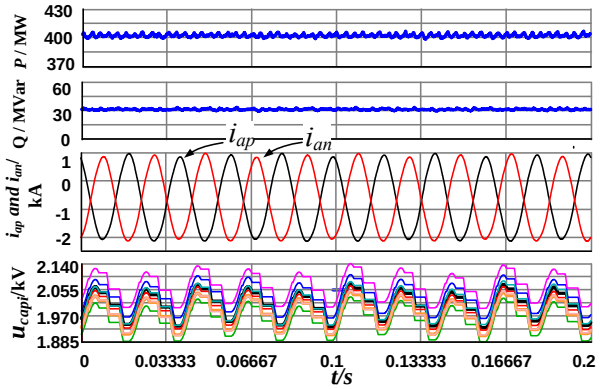

Fig. 8. Steady state experiment result with CPS-SPWM method.

The results of the NLM method are shown in Fig. 7. The active power is denoted by P and the reactive power is denoted by Q. The upper and lower arm currents of phase A are denoted by i_{ap} and i_{an}, and the capacitor voltages of the first eight sub-modules in the upper arm of phase A are denoted by u_{cap1}~ u_{cap8}.

Fig. 8 shows waveforms of P, Q, i_{ap}, i_{an}, and u_{cap1}~u_{cap8} when using the CPS-SPWM method.

The experiment results indicate that the active and reactive powers can trace their reference values accurately under both of the modulation methods.

Using the NLM method, the capacitor voltages of all of the sub-modules fluctuate consistently around the rated value, and the fluctuation is less than 5.95%.

Meanwhile, using CPS-SPWM method, the capacitor voltages of all of the sub-modules are not consistent. In addition, the deviation between the DC components of the capacitor voltage and its rated value is less than 2.88%, and the fluctuation is less than 6.38%.

Both of the modulation methods have a good effect on the capacitor voltage balancing control, and the NLM method has

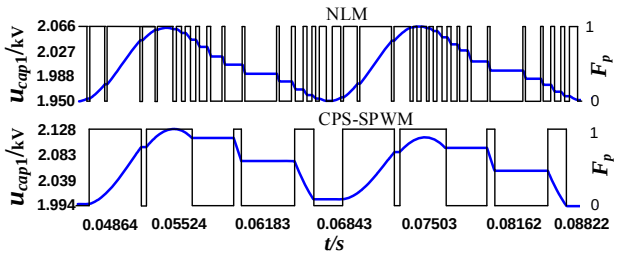

Fig. 9. The comparison of NLM and CPS-SPWM method.

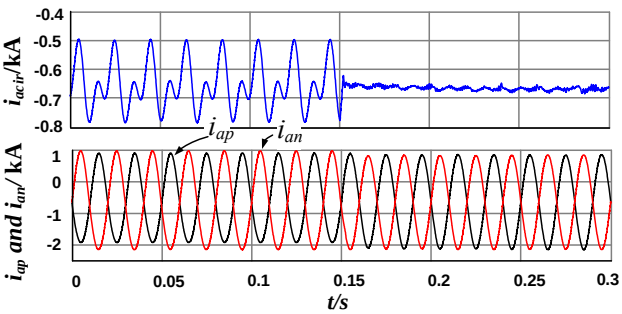

Fig. 10. The result of DC loop current suppressing.

been shown to have better performances in deviation and fluctuation.

Fig. 9 shows u_{cap1} and the corresponding firing pulse F_P in two cycles under the two modulation methods. This clearly indicates that the SM switches regularly in the CPS-SPWM method, and that its switching frequency is much lower than the switching frequency in the NLM method.

The above results show that the platform established in this paper is feasible for the experimental testing of MMC systems, and that the physical controller is able to test the features of various modulation and control strategies.

C. DC Loop Current Suppressing

In this experiment, the NLM method is chosen and the breakers S_3 and S_4 are closed. The objectives of the station control are the active power and reactive power. The reference values of the active power and reactive power are 400MW and 30MVar, respectively. In addition, the circulating current suppressing controller is started at 0.15s. The results of this experiment are shown in Fig. 10.

Where i_{acir} denotes the DC loop current of phase A. The fluctuation of i_{acir} is around 0.3kA before 0.15s. After the circulating current suppressing controller is started at 0.15s, the fluctuation of i_{acir} sharply drops to 0.02kA, which is only about 6.7% of the value of i_{acir} before 0.15s. The suppressing controller has an obvious and remarkable effect on the loop current. As a result, the distortion of the arm current i_{ap} and i_{an} has been significantly improved.

D. Power and Voltage Behavior Experiments

In order to test the step responses of the control strategy in the platform, two experiments are carried out with the CPS-SPWM modulation method.

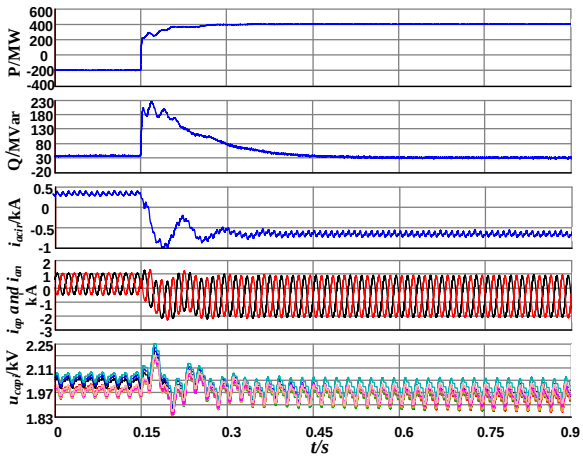

Fig. 11. The result of power step experiment.

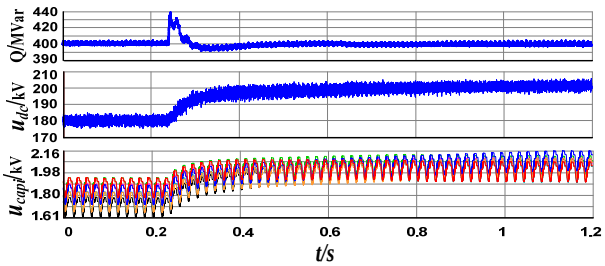

Fig. 12. The result of DC voltage step experiment.

One experiment is to test the response when the active power changes. S_3 and S_4 are closed and the active power jumps from -200MW to 400MW at 0.15s while the reactive power remains at 30MVar. The waveforms of P, Q, i_{ap}, i_{an}, and u_{cap1}~ u_{cap8} are shown in Fig. 11.

As shown in Fig. 11, the active power increases quickly and accurately tracks the reference. The reactive power is disturbed to a certain extent, and then reaches the steady state within 0.2s. The DC loop current of phase A fluctuates in the transient period. It changes from 0.33kA to -0.66kA under the control of the suppressing controller within 0.2s. The polarity of the DC components of the arm current is reversed with the change of the active power. After the reversal of the power flow, the fluctuation of the capacitor voltage gradually increases to transmit more active power.

The other experiment is to test the response when the DC voltage changes. S_3 and S_4 are opened and the control objectives of the station control are the DC voltage and the reactive power. The DC voltage jumps from 180kV to 200kV at 0.24s while the active power remains at 400MVar. Waveforms of Q, u_{dc} and u_{cap1}~u_{cap8} are shown in Fig. 12.

The DC voltage reaches to the reference value within 0.2s. The reactive power is slightly disturbed in the transient process and quickly returns to the steady state. The capacitor voltage of the sub-modules rises from 1.8kV to about 2.0kV within 0.2s to support the DC voltage.

E. Fault Experiment

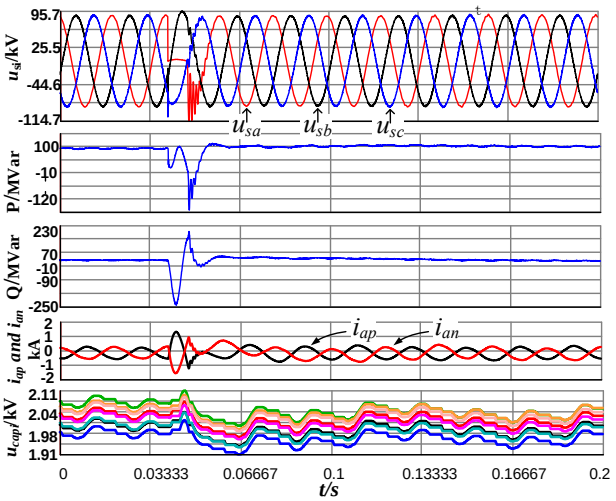

Fig. 13. The result of phase A to ground fault experiment.

To test the ability of fault simulation on the designed platform, a single phase to ground fault experiment on the AC side is carried out. In this experiment, the modulation method is CPS-SPWM and S_3 and S_4 are closed. The objectives of the station control are the active power and reactive power. The reference values of the active and reactive power are 100MW and 30MVar, respectively. The fault occurs at 0.04s in phase A and lasts for 0.005s. No protection action is taken for the fault.

Waveforms of u_{si}, P, Q, i_{ap}, i_{an} and u_{cap1}~ u_{cap8} are shown in Fig. 13.

As can be seen in Fig. 13, the operating state of the system has a sudden disturbance when the fault occurs. The increased current of the arm can damage the converter valves. After the clearance of the fault, the system quickly returns to the steady state. This experiment indicates that the MMC-HVDC system built in this platform is able to defend against some transient faults.

VI. Conclusion

In this paper, a MMC controller is designed and developed, and a hardware-in-the-loop simulation platform is established based on a RTDS simulator and the designed controller. The performance of the platform and its ability to test various control strategies was verified by several experiments. High precision simulations for MMC systems can be performed on this platform. By utilizing multicore technology and a main-auxiliary communication structure between cores, the designed controller satisfies the requirements of real time computation and communication. The proposed platform can be used in many fields, such as the design of the primary system for MMC-HVDCs, the test of control strategies, the optimization of control parameters, research on the interaction between a MMC-HVDC and a large power grid, etc.

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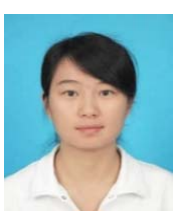

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