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Reduced Switch Count Topology of Current Flow Control Apparatus for MTDC Grids

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Abstract

The increasing demand for high voltage DC grids resulting from the continuous installation of offshore wind farms in the North Sea has led to the concept of multi-terminal direct current (MTDC) grids, which face some challenges. Power (current) flow control is a challenge that must be addressed to realize a reliable operation of MTDC grids. This paper presents a reduced switch count topology of a current flow controller (CFC) for power flow and current limiting applications in MTDC grids. A simple control system based on hysteresis band current control is proposed for the CFC. The theory of operation and control of the CFC are demonstrated. The key features of the proposed controller, including cable current balancing, cable current limiting, and current nulling, are illustrated. An MTDC grid is simulated using MATLAB/SIMULINK software to evaluate the steady state and dynamic performance of the proposed CFC topology. Furthermore, a low power prototype is built for a CFC to experimentally validate its performance using rapid control prototyping. Simulation and experimental studies indicate the fast dynamic response and precise results of the proposed topology. Furthermore, the proposed controller offers a real solution for power flow challenges in MTDC grids.

Key words: CFC, Current control, DC grids, MTDC, Power control, RCP

I. INTRODUCTION

Unlike in AC grids, power flow in any DC grid is determined mainly by grid cable resistances. A reliable and safe operation, in which cables are guaranteed to carry currents below their thermal limit even under sudden load changes, is difficult to achieve. Cables carrying currents over their limit for long periods may fail. Therefore, power (current) flow controllers are needed in DC grids. Currently, researchers and industry leaders are urged to focus on multi-terminal direct current (MTDC) grids as a solution to establish an interconnection among European grids [1]-[5]. Power flow control is one of the several major challenges that prevent the realization of MTDC grids [6], [7]. Other challenges include the absence of high voltage DC (HVDC) circuit breakers, protection schemes, and algorithms [8]-[10]; and HVDC DC to DC converters (DC transformers) [11]-[14]. The lack of practical, reliable and accurate current (power) flow control is a critical challenge for industry practitioners and researchers. Current approaches to achieving power flow control in MTDC are based on either modifying the control of the voltage source converters [15]-[24] or adding additional devices to the grid itself [25]-[30]. The insulated gate bipolar transistor (IGBT)-based current flow controller (CFC) concept presented in [29], [30] is adopted because it offers a promising solution to the power flow control problem. The present work presents a reduced switch count topology of the CFC to achieve accurate current flow control in MTDC grids with similar voltage stresses while cutting the cost and footprint in half. The CFC is connected in series to transmission cables to achieve functionalities such as balancing cable currents and current nulling in numerous cables and thereby ease the maintenance process. The main

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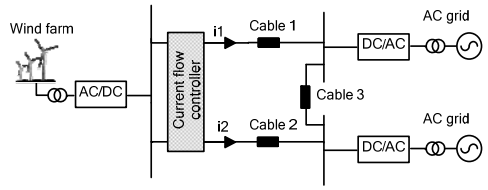


Fig. 1. A three terminal MTDC grid with CFC inserted in series.

advantage of the proposed CFC is its installation in series with the grid cables and isolation from the system ground (Fig. 1). Moreover, the voltage ratings of the capacitor and IGBT switches are relatively low in comparison with the grid voltage. This characteristic, in addition to the proposed reduced topology, leads to low manufacturing cost and footprint.

A simple control system based on the hysteresis band current control (HCC) technique is proposed for the CFC. HCC offers precise control and accurate results without the complexity of implementation or tuning. The complete operation and control of the proposed CFC are presented to balance the currents, set a current to a desired reference point, or null a current in a chosen cable. Simulation results illustrate the precise performance of the proposed CFC system. Moreover, experimental validation is carried out using advanced rapid control prototyping (RCP) by building a three-terminal DC grid with the CFC prototype to evaluate its functionality in different cases.

This paper is organized as follows. The theory of operation of the proposed reduced switch count topology for the CFC is discussed in Section II. The discussion includes possible operating modes with their switching states and mathematical modeling. The proposed control system is detailed in Section III. Computer simulations are carried out using the MATLAB/SIMULINK software package, and the results are demonstrated and analyzed in Section IV. The experimental validation of the proposed CFC system using the RCP technique is presented in Section V. Selected operating modes and functionalities are illustrated as well. Conclusions are provided in Section VI.

II. THEORY OF OPERATION

A. Operation of Current Flow Controller

The CFC consists of IGBT switches with parallel freewheeling diodes and capacitors, as shown in Fig. 2(a). Four IGBTs are inserted in series with each cable, and a capacitor is connected between both cables. The goal is to switch the capacitor in series such that it charges from the cable carrying a higher current and discharges from the other cable. This process can be controlled to achieve the desired operation, which could be balancing the currents in both cables, setting a current to a desired value, or nulling a current to zero. The speed and duration of switching the capacitor to charge/discharge from a cable depends on the set reference value, which is determined by the controller. Fig. 2(b) illustrates the proposed reduced switch count topology for the CFC, in which the numbers of switches and diodes are reduced by half. Two modes of operation are available for the CFC. In the first mode, i1 is the higher current, and Sa2 is switched on to allow current i2 to flow in cable 2 while connecting the capacitor in series to cable 1 to charge from it (Fig. 3(a)). This phase is followed by the switching on of Sb1 and Sb2 to allow the current i1 to flow in cable 1 and to connect the capacitor in series in cable 2 for discharging (Fig. 3(b)). In mode 2, when i2 is higher than i1, the operation is identical, except Sa1 is switched on instead of Sa2 (Figs. 4(a) (b)). The switching states of different IGBTs for the two modes of operation of the CFC are summarized in Table I.

B. Mathematical Modeling

To dynamically model a CFC using an averaging technique, we consider operation mode 1 illustrated in Fig. 3. As shown in this figure, i1 is higher than i2. The following equations describe the circuit of Fig. 3(a), in which the capacitor is charging from the line carrying the higher current, i1.

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + v_c + V_1 \quad (1)$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + V_2 \quad (2)$$

$$i_1 = C \frac{dv_c}{dt} \quad (3)$$

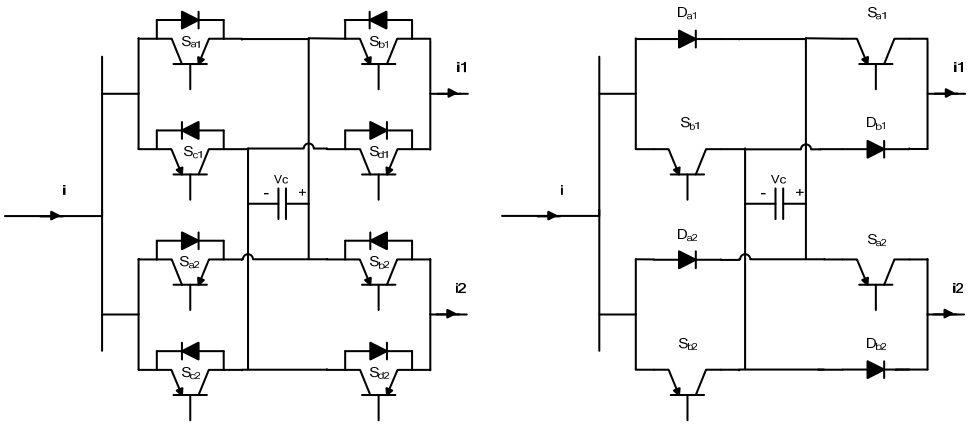
where r_1 and L_1 are the resistance and inductance of the first line, respectively; r_2 and L_2 are the resistance and inductance of the second line, respectively; v_c is the capacitor voltage; V is the voltage at the bus to which CFC is connected; and V_1 and V_2 are the voltages at the end terminals of the first and second lines, respectively. By defining $x^T = [i_1 \quad i_2 \quad v_c]$ as a state vector, where T refers to the transpose operation, equations (1), (2), and (3) can be arranged in a matrix form as

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & -1 \\ 0 & -r_2 & 0 \\ 1 & 0 & 0 \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B_1} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \quad (4)$$

Similarly, the state equations of Fig. 3(b), in which the capacitor is discharging into the line carrying the lower current i2, are written as follows:

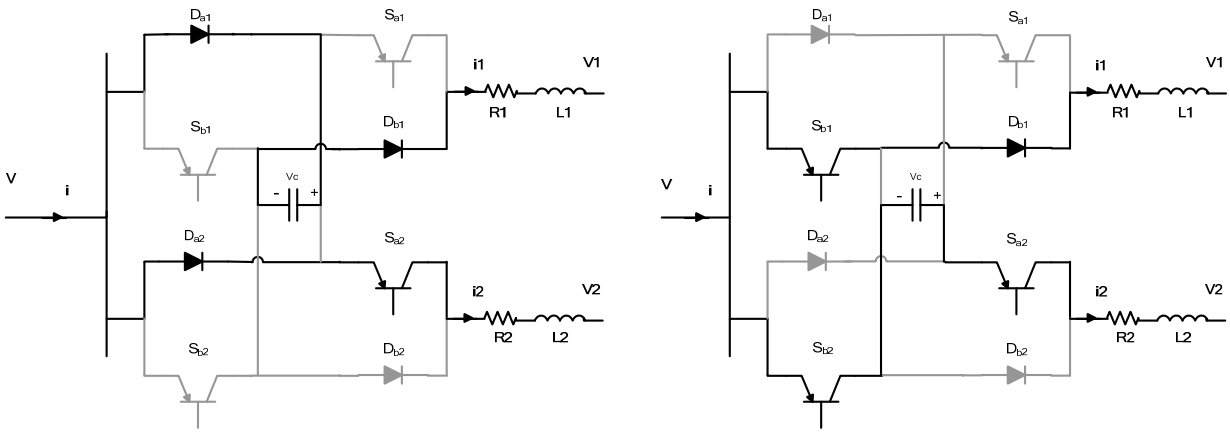
$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 \\ 0 & -r_2 & 1 \\ 0 & -1 & 0 \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B_2} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \quad (5)$$

Assume that the duty ratio of the charging mode of the operation is D. Multiplying (4) and (5) by D and (1-D), respectively, and adding the results to obtain the average model for the CFC when i1 >i2 yields the following:



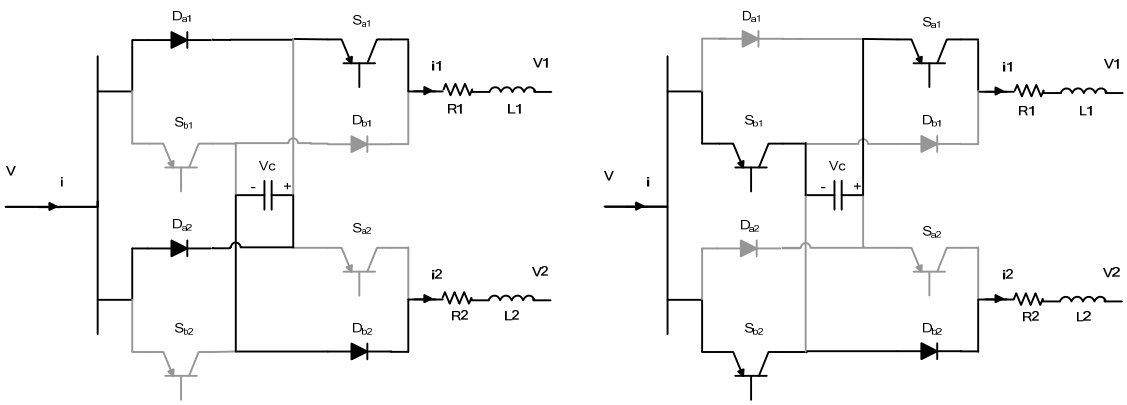
(a) (b)

Fig. 2. (a) CFC circuit topology [29]–[30], (b) proposed CFC reduced circuit topology.



(a) (b)

Fig. 3. (a) CFC operating in mode 1: charging from cable 1, (b) CFC discharging in cable 2.



(a) (b)

Fig. 4. (a) CFC operating in mode 2: charging from cable 2, (b) CFC discharging in cable 1.

TABLE I

SWITCHING STATES FOR CFC MODES OF OPERATION

Mode	Higher Current	Switching states			
		S_{a1}	S_{a2}	S_{b1}	S_{b2}
1	i_1	off	on	PWM	PWM
2	i_2	on	off	PWM	PWM

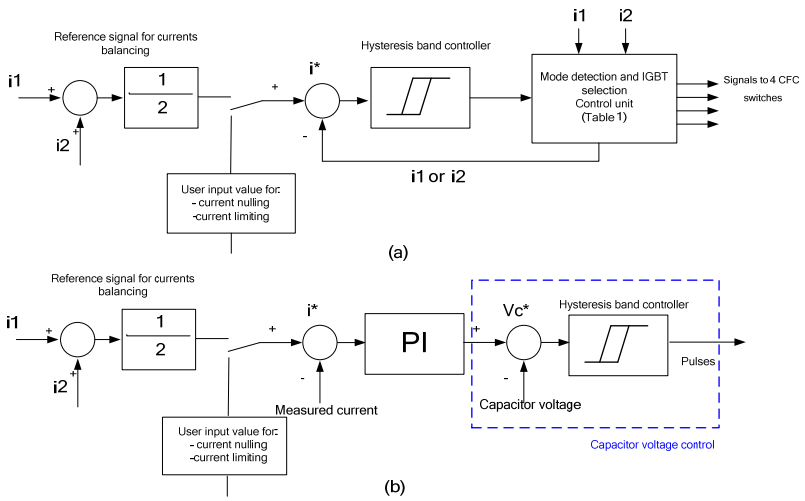


Fig. 5. (a) Proposed HCC control for the CFC, (b) proposed instantaneous voltage controller for CFC.

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & -D \\ 0 & -r_2 & 1-D \\ D & -1+D & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \quad (6)$$

where A=DA1+(1-D)A2 and B=DB1+(1-D)B2. At steady state, (6) is written as

$$\begin{bmatrix} -r_1 & 0 & -1 \\ 0 & -r_2 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ V_c \end{bmatrix} + \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix} = 0 \quad (7)$$

Solving (9), the DC steady-state value of the capacitor voltage can be expressed as

$$V_c = \frac{\frac{r_2}{r_1} D(V-V_1)+(V_2-V)(1-D)}{\frac{r_2}{r_1} D^2+(1-D)^2} \quad (8)$$

Equation (8) expresses the capacitor voltage as a function of network parameters and voltage drops across the cables connected to the CFC; this function represents the loading condition of the grid. The rated voltage of the CFC switches, which is equal to the rated capacitor voltage, can be estimated from (8).

To calculate the capacitor voltage ripple, (3) is integrated over the charging period as follows:

$$\int_0^{DT} i_1 \, dt = C \int_{V_{cmin}}^{V_{cmax}} v_c \quad (9)$$

where T refers to the switching period, which is the reciprocal of the switching frequency fs. Disregarding the current ripples compared with the average value, I1, results in the linear charging of the capacitor from the initial minimum voltage Vcmin to the maximum voltage Vcmax. The capacitor voltage ripple ΔV_c can be estimated from (9).

$$\Delta V_c = V_{cmax} - V_{cmin} = \frac{D\, I_1}{C\, f_s} \quad (10)$$

Equation (10) shows that increasing the capacitance reduces the capacitor voltage ripple. Equation (7) shows that the parameters of the DC grid and loading condition influence

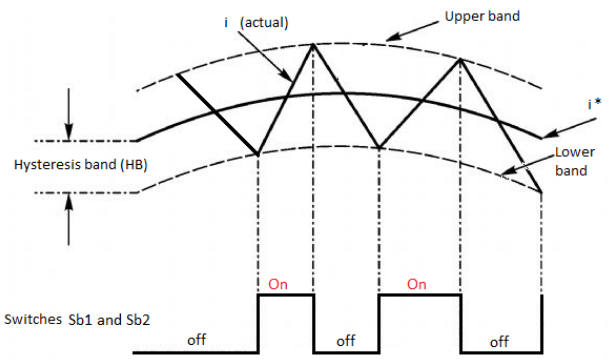


Fig. 6. Hysteresis band current control.

the line current, thus affecting the capacitor voltage ripple. The capacitor voltage ripple depends on the mode of operation as the charging current, which is I1 for mode 1, changes from mode 1 to mode 2. For mode 1, the capacitance can be roughly estimated from (8) and (10) to meet a required percentage voltage ripple, $\Delta V_{c\,pu} = \Delta V_c / V_c$, at the extreme deviations of the line currents. Similarly, the capacitance can be calculated for each mode of operation of the CFC. Finally, maximum capacitance is considered to meet the desired voltage ripple for all modes of operation. In the present study, the capacitance of the CFC is selected using trial and error, and, as implied by (10), higher capacitors produce smoother CFC performance and lower operating switching frequency.

III. Proposed Control of CFC Switches

Fig. 5(a) illustrates the proposed control system. It is based on the HCC technique to derive the PWM switches of the proposed CFC. In case of current balancing, the average value of both currents is calculated, and the result is set as a reference value for the controller, i*. The calculated reference value is compared with the measured actual value of the current that must be decreased, i1 or i2, which is set by the selection control unit. The error signal is considered as the

TABLE II
SIMULATION PARAMETERS

Parameter	Value
Grid voltage rating	320 kV
Capacitor 1	1 mF
Cable 1	1.5 Ω
	0.8 mH
Cable 2	2.35 Ω
	1.1 mH
Cable 3	2.42 Ω
	1.1 mH
Hysteresis band	5 A

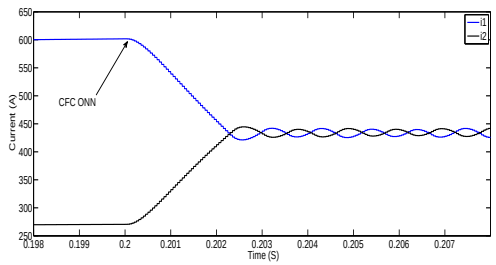


Fig. 7. Balancing currents i1 and i2 (mode 1).

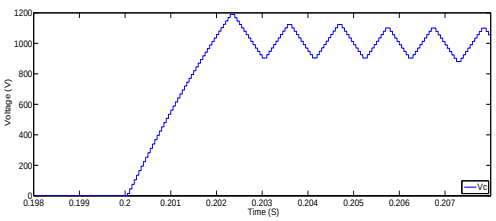


Fig. 8. CFC capacitor voltage.

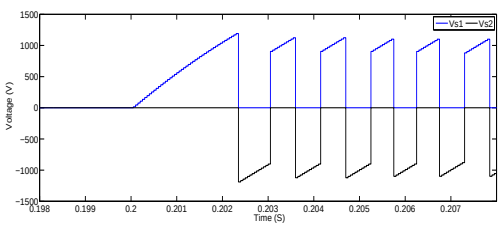


Fig. 9. Series voltages introduced by the CFC to both cables.

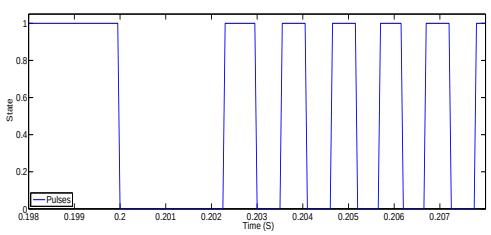


Fig. 10. HCC generated pulses.

input of the HCC (Fig. 5(a)). The on/off states determined by the HCC are assigned to the switches chosen by the IGBT selection control unit on the basis of the detected mode of operation (Table I). The HCC initially deactivates switches Sa to charge the capacitor from the cable carrying the highest current. When the actual current exceeds the reference current with the predefined hysteresis band (HB), the HCC activates switches Sa to disconnect the capacitor and allow it to discharge in the other cable. As a result, the actual current falls below the reference current based on the HB. The process is then repeated. Fig. 5(b) shows another control circuit that enables the application of capacitor voltage regulation. The error signal is passed through a proportional–integral (PI) controller, and its output is considered as the reference capacitor voltage Vc*, which is compared with the measured value and passed through an HB controller that produces the switching signals. This step is important in cases in which capacitor voltage must be limited to ensure that it does not exceed its rated value during operation. The principle of HCC is also illustrated in Fig. 6, which shows that the effects of varying the width of the HB on the switching frequency are noticeable. Switching frequency and accuracy depend mainly on the set value of the HB. The HB is inversely proportional to the switching frequency and accuracy. HCC offers many advantages, such as simplicity and ease of implementation. Moreover, its tuning and parameter settings are not as complicated as those of PI controllers. Similarly, external reference values can be applied directly to the proposed control system for current nulling and current setting. These two functions are useful in cases in which the current in the cable must be limited to a desired value or lowered to zero to disconnect the cable and facilitate maintenance.

IV. SIMULATION RESULTS

A simulation is carried out using the MATLAB/SIMULINK software package, and the results are presented in this section. An MTDC grid, similar to that in Fig. 1, is simulated to evaluate the dynamic and steady-state performance of the proposed control system of the CFC. The main simulation parameters are shown in Table II. As shown in this table, cables 1 and 2 carry currents i1 and i2, respectively. Two case studies are presented to evaluate the different features and operation modes of the proposed CFC.

A. Case 1: Balancing i1 and i2

This case study demonstrates a current balancing operation using the proposed CFC. Currents i1 and i2 are initially 0.6 and 0.27 kA, respectively. The CFC is set to operate at t = 0.2 s to charge the capacitor from cable 1 and discharge it in cable 2 to achieve the balanced operation. Currents i1 and i2 reach an average of 0.43 kA (Fig. 7), which indicates a fast performance without any overshoot. The capacitor voltage Vc and series voltages Vs introduced by the CFC to both cables are shown in Figs. 8 and 9, respectively. Fig. 9 shows that both series voltages Vs1 and Vs2 are equal but opposite in terms of direction as the capacitor charges from cable 1 and starts immediately discharging in cable 2. The gating signals generated by the HCC are presented in Fig. 10. As shown in

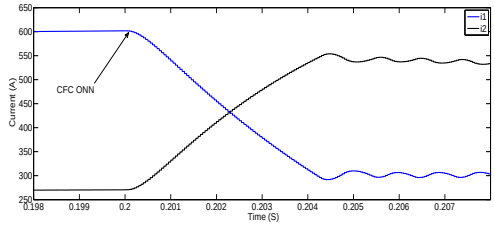


Fig. 11. Setting current i1 to 300 A.

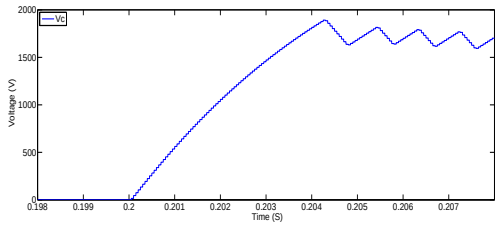


Fig. 12. Capacitor voltage.

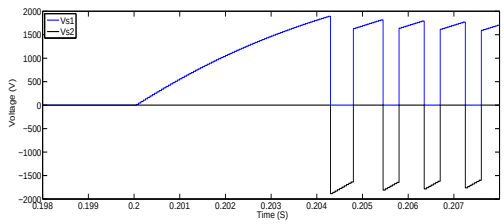


Fig. 13. Series voltages introduced by the CFC to both cables.

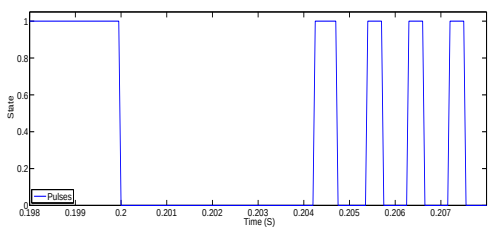


Fig. 14. HCC output pulses.

this figure, HCC produces an off gating signal from t = 0.2 s until the current i1 reaches the lower HB at t = 0.202 s. The results demonstrate one of the advantages of the CFC, that is, the capacitor and switches are subjected to an extremely small voltage (approximately 1 kV) relative to the grid voltage of 320 kV. The result is a low production cost and footprint for the CFC.

B. Case 2: Setting i1 to 0.3 kA

This case study limits the current i1 to 0.3 kA. As explained earlier, the user defines the reference value, which is 0.3 kA, and a similar control process is conducted. Currents i1 and i2 are shown in Fig. 11. The proposed control system of the CFC successfully performs the task, and current i1 is limited. Current i2 is increased to balance the sudden decrease in i1. The capacitor voltage and series cable voltages are shown in Figs. 12 and 13, respectively. The capacitor and series voltages are higher than those in case 1, as the capacitor must charge more in case 2 to achieve the reference

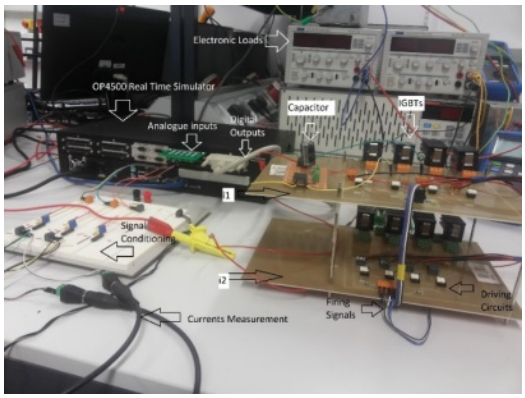


Fig. 15. Experimental RCP setup of the CFC.

TABLE III
EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	Value
Terminal 1	150 V DC power supply
Terminal 2	Electronic load
Terminal 3	Electronic load
Capacitor 1	1 mF
N-channel IGBT	70 A–600 V
Hysteresis band	5 mA

point. The capacitor and series voltage are approximately 2 kV, which is relatively low. Fig. 14 presents the gating signals produced by HCC in this case.

V. EXPERIMENTAL VALIDATION

A low power prototype of the CFC is built in the laboratory using low rating IGBT switches (Fig. 15). A three-terminal DC grid is constructed, with one terminal supplying DC and the other two connected to electronic (active) loads. The RCP technique is implemented using an OPAL RT OP4500 real-time simulator to control the CFC circuits in real time with the proposed control system. All cable currents are measured and connected as inputs to the OP4500 that outputs all gating signals to the CFC IGBT switches. The experimental prototype system parameters are shown in Table III.

A. Case 1: Balancing i1 and i2

To validate case 1, as explained earlier in the simulation results section, we present a similar case, in which i1 and i2 are balanced from the initial values of 1.8 and 1 A, respectively. The HB is set to 50 mA to demonstrate the operation of HCC (Fig. 6). The results in this case are shown in Fig. 16, which shows a clear gap between currents i1 and i2 after the balancing as they are oscillating around the average value 1.4 A as a result of the high HB set. This HB is then decreased to 5 mA in Fig. 17, which shows that the accuracy increases, and the switching frequency of the pulses increase significantly from 0.5 kHz to 4 kHz. The capacitor voltage Vc is also shown in both figures. Decreasing the HB

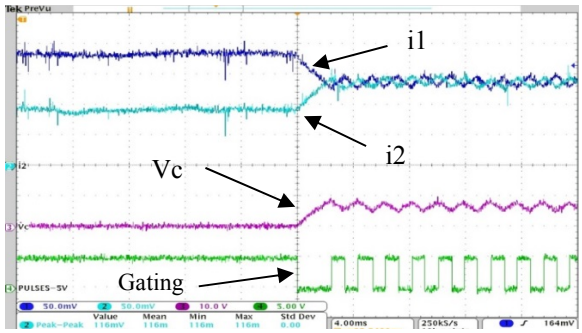


Fig. 16. Balancing i1 and i2 with HB=50 mA. X axis: 4 ms/Div and Y axis: 0.5 A/Div, 10 V/Div, 5 V/Div.

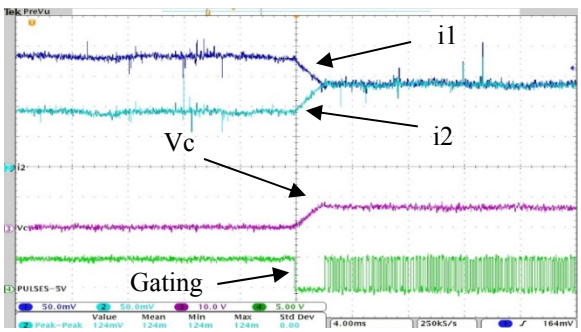


Fig. 17. Balancing i1 and i2 with HB = 5 mA. X axis: 4 ms/div and Y axis: 0.5 A/div, 10 V/div, 5 V/div.

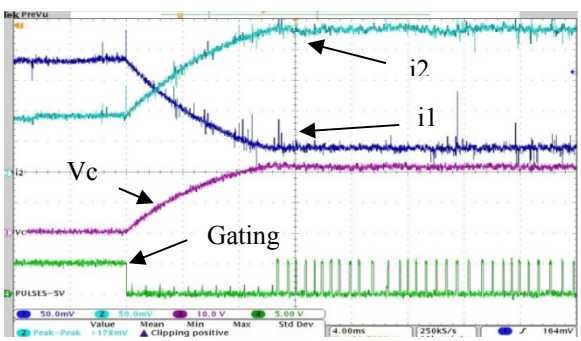


Fig. 18. Setting i1 to 400 mA. X axis: 4 ms/div and Y axis: 0.5 A/div, 10 V/div, 5 V/div.

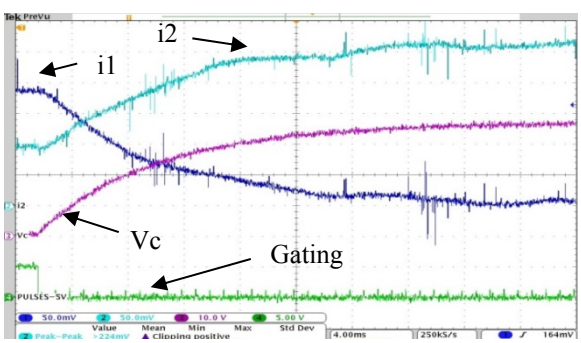


Fig. 19. Nulling current i1. X axis: 4 ms/div. and Y axis: 0.5 A/div, 10 V/div, 5 V/div.

results in a smooth balancing of the currents, but a higher switching frequency is incurred.

B. Case 2: Setting i1 to 0.4 and 0 A

The reference value is set to 0.4 A to validate the results obtained from case 2 of the simulation. i1 is successfully limited to 0.4 A, and i2 increases significantly to cover the decrease in i1 (Fig. 18). The capacitor voltage Vc is higher than that in case 1, as i1 decreases at a higher amount, in which case the capacitor has to charge more. The gating signals in this case are shown in Fig. 18. Another option is to set the reference value to zero to null the current flowing in the cable. The results of this case are shown in Fig 19, in which the capacitor is fully charged to block the current i1 and the gating signal is equal to zero to keep the capacitor connected. The success of the experimental operation demonstrates the validity of the proposed CFC and control strategy.

VI. Discussion

The simulated and experimental results validate the proposed topology and control strategy. They also show that reducing the HB results in increased switching frequency. A common practice is to set the HB in the range of 3% to 5% of the current magnitude. The performance improves as the ripples decrease; however, the switching losses increase, as expected for any power electronics converter. Hence, a CFC capacitor with high capacitance should be chosen because its application ensures a smooth operation with low voltage and current ripples while minimizing switching frequency and losses.

VII. Conclusions

This paper presents a reduced switch count topology for a CFC to achieve current limiting applications in DC grids, including multi-terminal HVDC systems. A simple control system based on the HCC technique is proposed for the CFC. The detailed operating modes and mathematical modeling are illustrated. Functionalities such as current balancing, current limiting, and current nulling of the proposed HCC-based CFC are discussed and evaluated accordingly. The fast dynamic response and accurate performance of the proposed system are investigated using computer software and experimental validation. As indicated in the results, the proposed CFC incurs low costs and a small footprint and thus serves as a promising solution for power flow control problems in next-generation DC grids.

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