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Control Strategy Design of Grid-Connected and Stand-Alone Single-Phase Inverter for Distributed Generation

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Abstract

Dual-mode photovoltaic power system should be capable of operating in grid-connected (GC) and stand-alone (SA) modes for distributed generation. Under different working modes, the optimal parameters of inverter output filters vary. Inverters commonly operate in GC mode, and thus, a small capacitance is beneficial to the GC topology for achieving a reasonable compromise. A predictive current control scheme is proposed to control the grid current in GC mode and thereby obtain high-performance power. As filter are not optimal under SA mode, a compound control strategy consisting of predictive current control, instantaneous voltage control, and repetitive control is proposed to achieve low total harmonic distortion and improve the output voltage spectrum. The seamless transfer between GC mode and SA mode is illustrated in detail. Finally, the simulation and experimental results of a 4 kVA prototype demonstrate the effectiveness of the proposed control strategy.

Key words: Distributed generation (DG), Grid connected, Predictive current control, Repetitive control, Single-phase inverter, Stand-alone power supply

I. INTRODUCTION

In the past two decades, renewable energy technologies have been proposed to relieve environmental pollution and achieve sustainable development [1], [2]. Renewable energies, including photovoltaic power energy, wind energy, and others, have been widely applied to distributed generation (DG) installations [3]. However, DG units often cannot directly support electrical appliances with the same frequency and amplitude as the grid. DG systems are thus connected to the utility grid (UG) through power electronic inverters. When unexpected power disruptions occur, grid-connected (GC) inverters should be capable of operating in stand-alone (SA) mode. A high-performance inverter that can operate in both SA mode and GC mode is needed to ensure the efficient utilization of DG units [4].

GC inverters can be achieved by various circuit topologies [5], but new designed circuit topologies cannot be widely adopted in commercial products [4]. A single-phase inverter with low cost and high efficiency (Fig. 1) shows a simple circuit topology and few components. A filter capacitor is necessary because the grid-interactive inverter should operate in SA mode [6]. Nevertheless, the filter capacitor can affect the quality of the grid current in GC mode, especially at low output power. As the inverter usually operates in GC mode, a small capacitor is beneficial to GC topology for achieving reasonable compromise. A low-pass filter with $L_f = 1.3\ mH$ and $C_f = 4.4\ \mu F$ is selected by considering the switching frequency and output fundamental frequency in Fig. 1 [7]. The value of the capacitor is smaller than that of the capacitor designed in [8]-[10] ($C_f = 14.25\ \mu F,\ 20\ \mu F,\ 75\ \mu F,$ respectively). The control objectives of the DG system in the present work are (1) to supply a sinusoidal output voltage at the load terminal (v_{inv}) in SA mode, (2) to transfer a sinusoidal grid current (i_g) to the UG in GC mode, and (3) to obtain a smooth transition between

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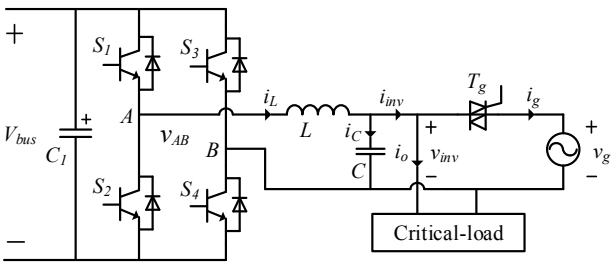


Fig. 1. Single-phase full-bridge inverter of dual mode.

the two modes. Many control approaches have been proposed to control DC/AC inverters. These methods include proportional-integral control, sliding-mode control, optimal multi-loop linear resonant control, linear control, backstepping control, and passivity-based control. Some control methods are only suitable for either SA mode or GC mode, whereas others are highly complex and difficult to realize and apply to industries. The present work proposes a novel control method for solving these problems. In GC mode, a predictive current control scheme is proposed to control the grid current and obtain a high-performance power. As the filter is not optimal in SA mode, a compound control strategy consisting of predictive current control, instantaneous voltage control, and repetitive control (RC) is proposed to achieve a low total harmonic distortion (THD) and improve the output voltage spectrum.

This paper is organized as follows. The description of the inverter, the control methods for SA and GC modes, and the details of the seamless transition between the two modes are explicated in Section II. The simulation results are presented in Section III to prove the usefulness of the proposed control strategies. The experimental results verifying the theoretical analysis are presented in Section IV. Finally, conclusions are drawn in Section V.

II. SYSTEM CONFIGURATION AND PROPOSED CONTROL STRATEGY

A. Single-Phase Inverter Description

Fig. 1 shows the conventional full-bridge inverter scheme. The pulse-width modulation (PWM) inverter framework includes four power switches (S_1, S_2, S_3, and S_4) and a low-pass filter (L and C). Critical load represents an output load in SA mode. V_{bus}, v_g, and v_{inv} are the voltages of the DC bus, utility grid, and inverter output, respectively. v_{AB} is the voltage between points A and B. i_L, i_c, i_{inv}, i_o, and i_g are the currents of the filter inductor, filter capacitor, inverter output, critical load, and UG, respectively. The GC switch (T_g) disconnects or reconnects the inverter output from and to the grid. When T_g is closed, the inverter is working in GC mode to transmit the power of DG units to the UG. Under utility interruptions or abnormal grid conditions, T_g is open, and the inverter provides power to the emergency load while operating in SA mode.

The DC–AC converter is a nonlinear system because of the presence of the solid-state switches. A nonlinear system must

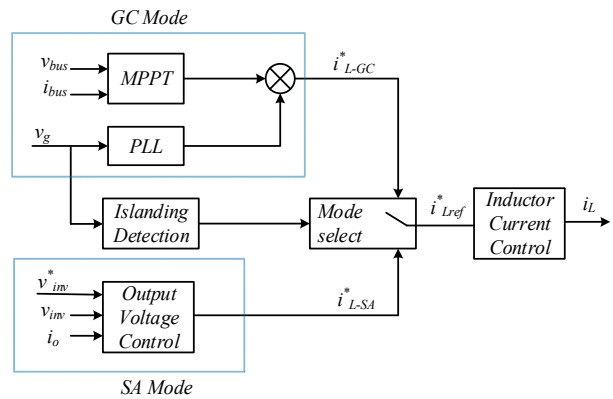


Fig. 2. System control block diagram.

be linearized around its operating point before the linear controller can be designed. The performance of the controlled system in the neighborhood of the operating point can be guaranteed if the designed controller is sufficiently robust. A wide system bandwidth equates to a large neighborhood. From Fig. 1, the inverter model is determined with the following differential equation:

$$v_{AB} = v_{inv} + L\frac{di_L}{dt} \tag{1}$$

$$v_{AB} = V_{bus} \times D \tag{2}$$

where D is the PWM duty cycle during one switching period.

B. System Control Method

The system control block diagram is shown in Fig. 2. Switching between GC mode and SA mode is determined via islanding detection. Although the current controllers in GC and SA modes are the same, the current commands are different. When the inverter is operated in GC mode, the current command i^*_{Lref} is equal to i^*_{L-GC}, which is determined via maximum power point tracking (MPPT) control and digital phase locked loop (PLL) control. Owing to the limited space in this paper, these two control methods are not discussed here, references are available in [11] and [12]. When the inverter is operated in SA mode, i^*_{Lref} is equal to i^*_{L-SA}, which is determined by the inverter output voltage controller. Next, the algorithm is analyzed in detail.

C. GC Mode

In GC mode, the inverter behaves as controllable current sources. The closed-loop control method manipulates the output current (i_g) with a high power factor. With the recently developed high-performance digital signal processor (DSP), a digital controller can be designed with high sampling rate that gradually approaches the switching frequency of a power converting system. Assume that the inverter is operating with a constant switching frequency, the switching period of which is a constant value T. During the switching period $[k, k+1]$, (1) and (2) can be rewritten in a discrete form as

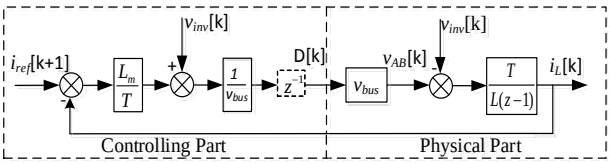


Fig. 3. Current control block diagram.

$$v_{AB}[k] = v_{inv}[k] + (i_L[k+1] - i_L[k]) * \frac{L}{T} \tag{3}$$

$$v_{AB}[k] = V_{bus}[k] \times D[k] \tag{4}$$

Substituting (4) into (3), $D[k]$ can be expressed as

$$D[k] = \frac{v_{inv}[k] + (i_L[k+1] - i_L[k]) * \frac{L}{T}}{V_{bus}[k]} \tag{5}$$

The controller is aimed at ensuring that the load current at the sampling point [*k+1*] is equal to the reference current value at point [*k+1*]. Thus, the control law (5) transforms into (6) [13]. This type of control is referred to as predictive current control.

$$D[k] = \frac{v_{inv}[k] + (i_{ref}[k+1] - i_L[k]) * \frac{L}{T}}{V_{bus}[k]} \tag{6}$$

Fig. 3 illustrates the employment of an inner current loop. z^{-1} is a control delay. The predictive controller requires full knowledge of system parameters. If model mismatch occurs in the control system, the mismatch influences the control accuracy. *Lm* is the parameters of the digital controller. Disregarding digital control delay, the input-to-output transfer function of the current control loop is

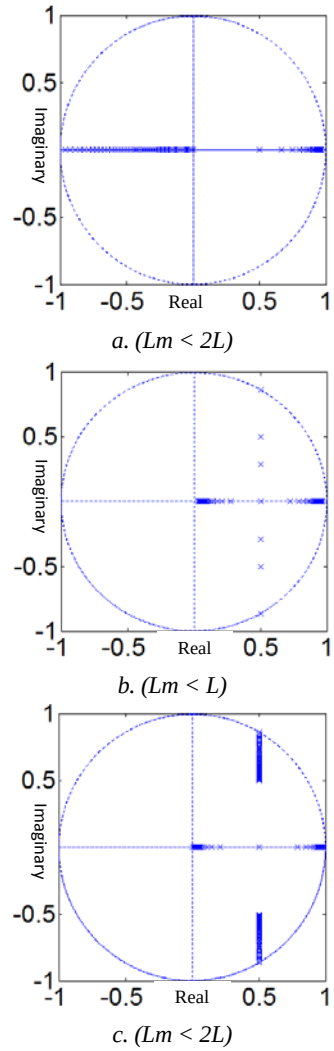
$$\frac{I_L(z)}{I_{ref}(z)} = \frac{1}{\frac{L}{L_m}(z-1)+1} \tag{7}$$

The root locus of the closed-loop system (7) is obtained, as shown in Fig. 4(a). The system poles are in the unit circle if *Lm* is less then *L*. When *Lm* is greater than *L*, it allows a deviation of 50%. No control delay is considered in (7). However, an actual digital control system has unavoidable control delay. If digital control delay is considered, the input-to-output transfer function of the current control loop is

$$\frac{I_L(z)}{I_{ref}(z)} = \frac{1}{\frac{L}{L_m}z(z-1)+1} \tag{8}$$

The root locus of the closed-loop system (8) is obtained, as shown in Fig. 4(b). The system is unstable when $L_m \geq L$. In order to ensure system stability, L_m must be less than *L*, which may cause poor stability margin and dynamic performance.

The goal of predictive current control is to reduce the error of the next control period to zero. However, as a result of sampling errors, model parameter deviation, and so on, reducing errors to zero is difficult. Thus, an improved algorithm is proposed. The current error converges to 0



a. (Lm < 2L)

b. (Lm < L)

c. (Lm < 2L)

Fig. 4. Root locus plot of inner loop.

automatically, and the stability margin of the system greatly improves. The control law is

$$i_e[k] = i_{ref}[k] - i_L[k] \tag{9}$$

$$D[k] = \frac{v_{inv}[k] + (i_{ref}[k+1] - i_L[k] - 0.5 * i_e[k]) * \frac{L_m}{T}}{V_{bus}[k]} \tag{10}$$

On the basis of (10), we can derive the input-to-output transfer function of the current control loop as follows:

$$\frac{I_L(z)}{I_{ref}(z)} = \frac{z-0.5}{\frac{L}{L_m}(z^3 - z^2) + 0.5z} \tag{11}$$

The root locus of the closed-loop system (11) is obtained, as shown in Fig. 4(c). The permissible range of the model parameters is the same as that in (7).

D. SA Mode

In SA mode, the output voltage (v_{inv}) should be controlled with a low THD. The control block diagram in SA mode is given in Fig. 5. Three controllers are included in the control

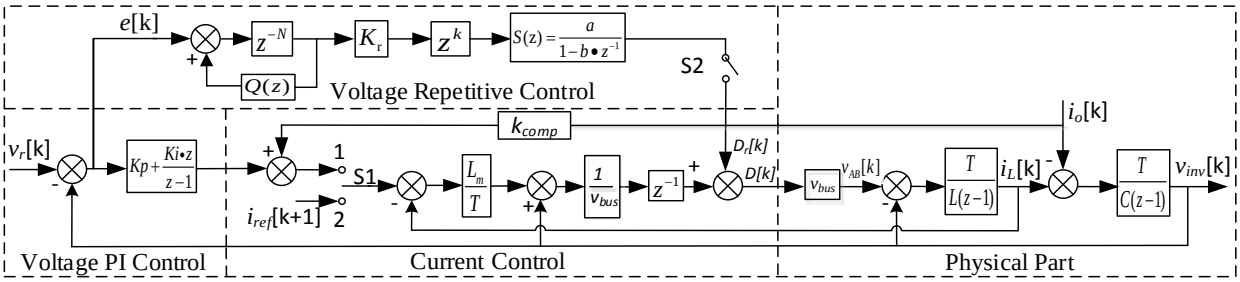


Fig. 5. Control block diagram of the grid-interactive inverter in off-grid mode.

loops: a current tracking controller, a voltage tracking controller, and a repetitive controller. The current control loop is the same as that in GC mode. The output voltage controller is used to regulate output voltage, with the reference voltage $v_r(z)$ being a sine waveform given by the DSP. The output of the voltage control loop is the reference current of the current control loop. Load disturbance rejection performance is improved by taking the load current as the feed-forward compensation in the current loop. k_{comp} is the compensation coefficient. The input-to-output transfer function of the voltage control loop becomes

$$\left|\frac{V_{\text{inv}}}{I_O}\right| = \frac{\frac{L}{KT}(z-1)^2 + (1-\text{k}_{comp})(z-1)}{\frac{LC}{KT^2}(z-1)^3 + \frac{C}{T}(z-1)^2 + K_p(z-1) + K_i z} \tag{12}$$

where K_i and K_p are the integral and proportional coefficients of the output voltage controller, respectively. As shown in (12), the inverter in SA mode is stable according to conventional control theory. The parameters are as follows: k_{comp} = 0.96, K_p = 2.5, and K_i = 0.03. Fig. 6 is the amplitude frequency response of V_{inv}/I_o. The control system achieves a strong anti-load disturbance performance.

In SA mode, the filter capacitor should be large to improve voltage quality. A small filter capacitor would negatively affect the output voltage, as voltage harmonics would not be filtered out effectively and the dead time in a PWM-based inverter would result in output waveform distortion and fundamental voltage loss, particularly when the output voltage is low. When the current reaches zero during the dead time and stays at zero during the remaining dead time, the output voltage cannot be controlled, and the phenomena of zero crossing becomes difficult to avoid, particularly when the filter capacitor is small. All repetitive disturbance is repeated for every switching operation. It can be solved via RC. RC, which originates from the internal model principle, provides a solution for eliminating periodic errors.

A plug-in-type modified repetitive controller is shown in Fig. 5. The result of the integration, denoted as $e[k]$, is then processed by the following units to generate D_r [14].

1) z^{-N} : time delay unit. It postpones the control action by one fundamental period so that time advances z^k units and the noncausal zero-phase-shift notch filter in $S(z)$ can be

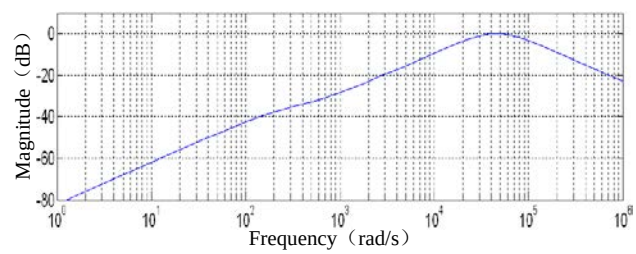


Fig. 6. Amplitude frequency response of V_{inv}/I_o.

realized. Let $N = f_s / f$ with f =50 Hz as the fundamental frequency of the reference signal $v_r(z)$, and let f_s=16k be the sampling rate, so N=320 is the order of the RC.

2) $S(z)$: compensator. It modifies the magnitude characteristic of the open-loop system for improved harmonic rejection.

3) z^k : time advance unit. Advances the control action by sample periods in the next fundamental period, thus compensating for the delay of compensator $S(z)$ and the inverter.

4) k_r : gain. Controls the magnitude of D_r.

Steady-state analysis shows that if the band-limit filter $Q(z)$ is a unit, no steady-state error occurs. Unfortunately, the Nyquist criterion reveals that a stable system cannot be established when $Q(z)=1$ .With this constraint, set $Q(z)=0.96$. According to [14], the designed parameters are a=0.2, b=0.8, k_r =1, and k=5.

E. Seamless Transfer

The detailed process of the seamless transfer between SA mode and GC mode is summarized as follows.

1) SA mode to GC mode:

a) Detect that the grid is operating in normal condition.

b) Adjust the reference voltage ($v_r(z)$) to match the frequency and phase of the grid voltage via digital PLL.

c) Once the load voltage is equal to the grid voltage, turn on T_g at the zero crossing of the grid voltage. The control model switches to GC mode.

d) Increase the reference grid current slowly from the load current to the desired value (decided by MPPT).

2) GC mode to SA mode:

TABLE I
SYSTEM PARAMETERS

Parameters	Values
Rated output power	4 kVA
Grid voltage	220 (rms)
Grid frequency (fs)	50 Hz
DC-link voltage (Vbus)	370 V
Switching/Sampling frequency (fsample)	16 kHz
Output filter inductance (L)	1.3 mH
Output filter capacitance (C)	4.4 μF

a) Detect a fault on the utility.

b) Change the reference current to load current.

c) Turn off T_g at the zero crossing of the load voltage. The control model then switches to SA mode.

III. SIMULATION RESULTS

To verify the effectiveness of the proposed control strategy, we construct a simulation model in power electronic simulation software with the system parameters given in Table I.

Fig. 7 shows the simulation results of SA mode. Figs. 7(a) and (c) show the simulation results of the double loop controlled and RC + double loop controlled PWM inverter under rated output power. RC can clearly reduce zero-crossing distortion. Fig. 7(b) shows that a large capacitor can reduce zero-crossing distortion but that a large filter capacitor can affect the grid current control in GC mode and increase hardware cost.

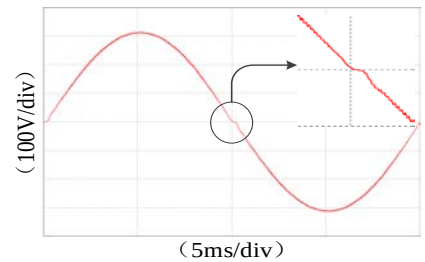
Fig. 7(d) shows that in the simulation of the load step of rated power, a large and relatively transient drop in voltage occurs, but the drop in RMS value is less than 2 V. Clearly, the proposed control method in SA mode is less sensitive to load variations.

Fig. 8(a) presents the simulation results for a transfer from GC mode to SA mode. As a result of the randomness of the grid fault and the mismatch of inverter output power and load power, load voltage and current undergo some inrush spikes during the transition period. This process is short, and the waveform returns to normal when the system switches to SA control mode.

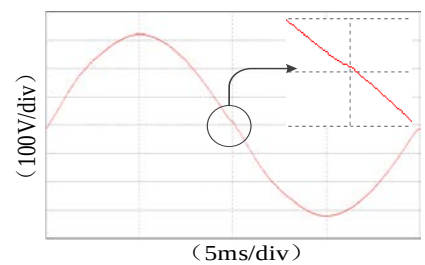
Fig. 8(b) presents the simulation results for a transfer from SA mode to GC mode. No sudden voltage change occurs across the emergency load. The load voltage and load current do not show any inrush spikes during the entire transition period, resulting in a smooth transition from SA mode to GC mode.

IV. EXPERIMENTAL RESULTS

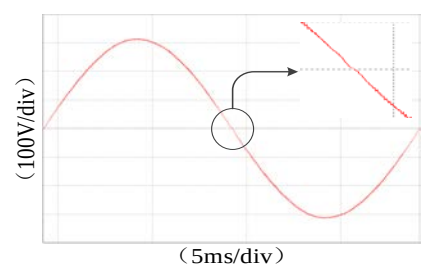
An experimental system is built in the laboratory to further verify the theoretical analysis and simulated results. The system parameters used in the experiment are the same as those



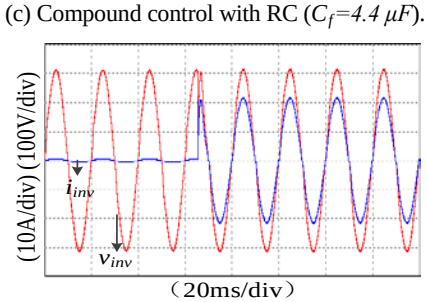
(a) Double loop control (C_f=4.4 μF).



(b) Double loop control (C_f=40 μF).



(c) Compound control with RC (C_f=4.4 μF).

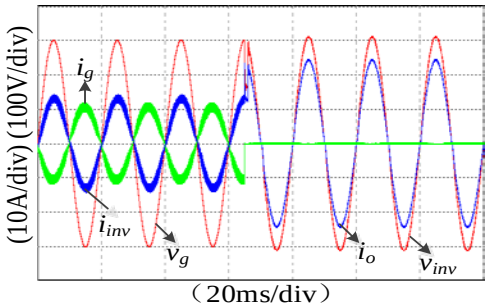


(d) Output power changes from 0 kVA to 4 kVA.

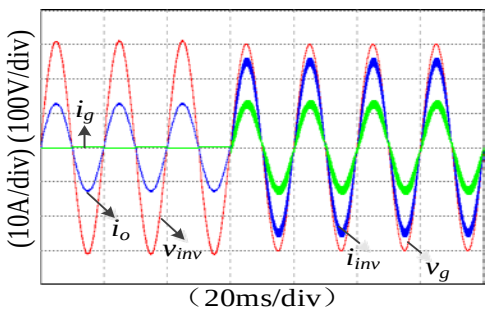
Fig. 7. Simulation waveforms of SA mode.

in the simulation model (Table I). The proposed control scheme is implemented with a DSP TMS320F2808 from Texas Instruments. The 16 kHz pulse-width modulated driving signals for the full-bridge inverter are generated by the DSP and peripheral logic circuits. The TMS320F2808 is essentially a 32-bit microcontroller with DSP architecture. Most of its instructions can be executed in one instruction cycle of 10 ns.

Figs. 9(a) and (b) show the experimental results at 4 kW load. With RC compensation, voltage distortion near the zero crossing is reduced, and the THD of the voltage decreases from 2.9% to 0.7%. Fig. 9(c) shows the experimental results for a rectifier load (2500 VA) with a power factor (PF) of 0.7. The THD of the voltage is 2.2%. Fig. 9(d) shows that the step response of the load changes from 0 kVA to 4 kVA. The

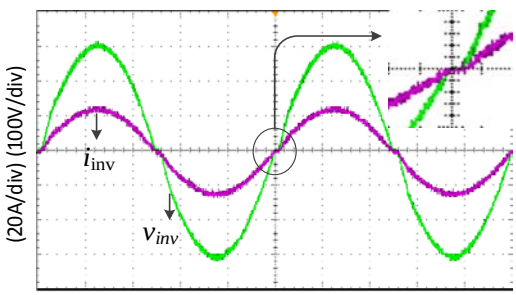


(a) GC mode to SA mode.

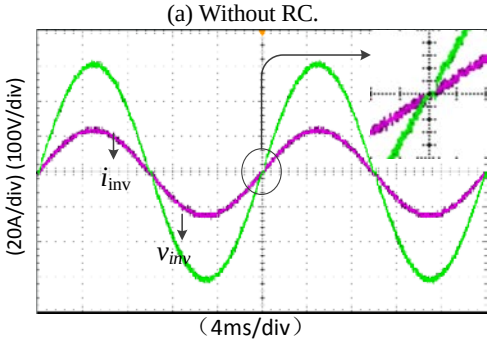


(b) SA mode to GC mode.

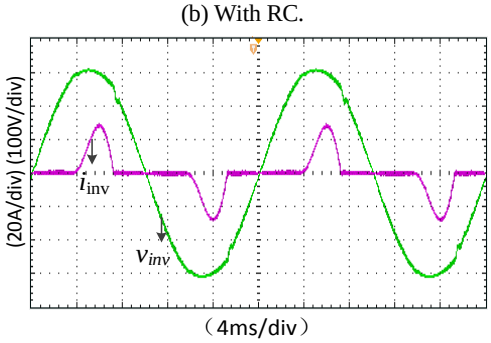
Fig. 8. Simulation waveforms of transfer control.



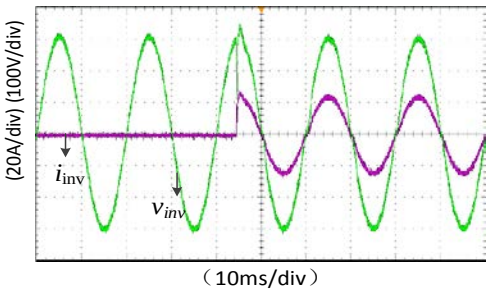
(a) Without RC.



(b) With RC.

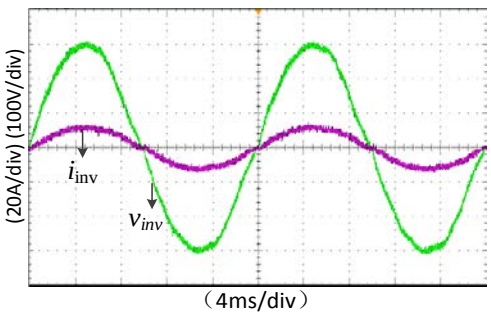


(c) Rectifying load.

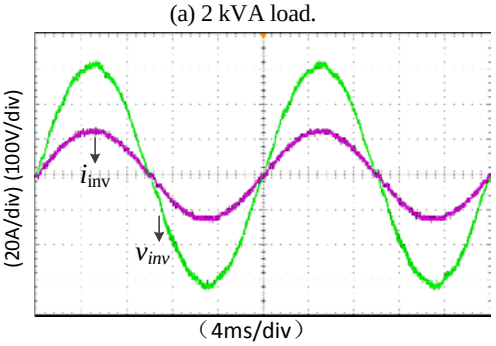


(d) 4 kVA load.

Fig. 9. Experimental waveforms of SA mode.



(a) 2 kVA load.



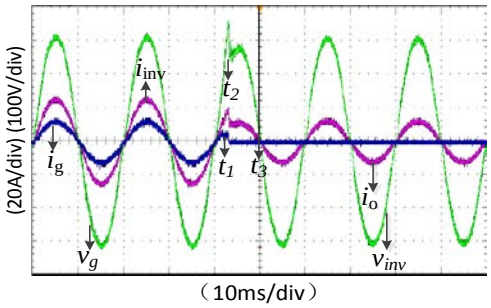
(b) 4 kVA load.

Fig. 10. Experimental voltage and current responses of GC mode.

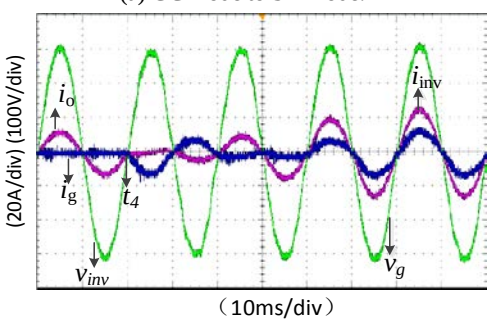
settling time of the system is 600 μs. The performance indexes in Fig. 9 indicate that the experimental results agree with the numerical simulations and that the proposed control method can provide favorable control performance under either regular operations or load variations.

Fig. 10 presents the experimental results in GC mode. The THD of the grid voltage is about 3.1%, but the THD of the grid current is only 1.8% (4 kVA GC power) and 2.5% (2 kVA GC power). The PF of the grid current is 1 (4 kVA GC power) and 0.998 (2 kVA GC power). The waveform quality of the grid current is good under the control method, even in polluted voltage.

Fig. 11 presents the experimental results of transfer control under a 2 kVA load. Fig. 11(a) shows the experimental results of the transition from GC mode to SA mode. The output power of the inverter is 4 kVA. i_{inv} is the inverter output current composed of load current and grid current. The grid is broken off at t_1. Because the output power of the inverter is greater

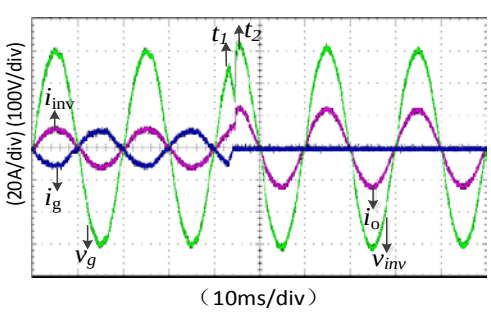


(a) GC mode to SA mode.

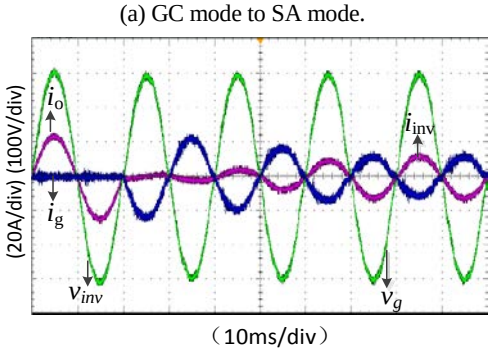


(b) SA mode to GC mode.

Fig. 11. Experimental waveforms of transfer control with 2 kVA load.



(a) GC mode to SA mode.



(b) SA mode to GC mode.

Fig. 12. Experimental waveforms of transfer control with 4 kVA load.

than the load power consumption, thus causing an inrush spike in the inverter output voltage. The grid fault is detected at t_2, and the control system switches the reference current value to the load current. T_g (bidirectional triode thyristor) is switched off at t_3 (zero crossing of the inverter voltage), and the control system switches to voltage control mode.

Fig. 11(b) shows the experimental results from SA mode to GC mode. When the grid is normal, the voltage of the inverter synchronizes with the grid voltage. T_g is switched on at the zero crossing of the grid voltage, and the control system switches to current control mode. The reference current increases from the current value. Load voltage and load current, which do not show inrush spikes during the entire transition period, exhibit a smooth transition from SA mode to GC mode.

Fig. 12 presents the experimental results of transfer control under a 4 kVA load. The output power of the inverter is 2 kVA in GC mode. Grid and inverter supply power to the load simultaneously. As load power is greater than the output power of the inverter, the inverter output voltage experiences an inrush spike when the grid breaks off at t_1. As in the analysis of Fig. 11, the value of the reference current switches to the value of the load current. Thereafter, the control system switches to voltage control mode at the zero crossing of the inverter voltage. The load voltage and load current do not show any inrush spikes during the entire transition period from SA mode to GC mode (Fig. 12(b)).

V. Conclusions

This study successfully developed a single-phase full-bridge inverter with a small filter capacitor. Predictive current control was applied to both SA and GC power supply modes. A compound control strategy was applied to SA mode. A novel seamless transfer between SA mode and GC mode was proposed. The proposed control method shows fast response characteristics in transient states, robust control performance, high power quality, and automatic transformation between SA mode and GC mode. The proposed control schemes are easily applied to other power conversion systems to satisfy high power quality demands.

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