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Performance Evaluations of Four MAF-Based PLL Algorithms for Grid-Synchronization of Three-Phase Grid-Connected PWM Inverters and DGs

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Abstract

The moving average filter (MAF) is widely utilized to improve the disturbance rejection capability of phase-locked loops (PLLs). This is of vital significance for the grid-integration and stable operation of power electronic converters to electric power systems. However, the open-loop bandwidth is drastically reduced after incorporating a MAF into the PLL structure, which makes the dynamic response sluggish. To overcome this shortcoming, some new techniques have recently been proposed to improve the transient response of MAF-based PLLs. In this paper, a comprehensive performance comparison of advanced MAF-based PLL algorithms is presented. This comparison includes HPLL, MPLC-PLL, QT1-PLL, and DMAF-PLL. Various disturbances, such as grid voltage sag, voltage flicker, harmonics distortion, phase-angle and frequency jumps, DC offsets and noise, are considered to experimentally test the dynamic performances of these PLL algorithms. Finally, an improved positive sequence extraction method for a HPLL under the frequency jumps scenario is presented to compensate for the steady-state error caused by non-frequency adaptive DSC, and a satisfactory performance has been achieved.

Key words: Grid-synchronization, Moving average filter (MAF), Phase-locked loop (PLL), Transient response

I. INTRODUCTION

The three-phase phase-locked loop (PLL) technique is widely used for accurate estimation of the phase-angle, frequency, and sequence components extraction of the grid voltages in power systems, which is crucial for the grid-integration of distributed generation (DG) systems, such as wind, PV, and flexible ac transmission systems (FACTS), as well as active power filters (APFs) [1]-[3]. However, a great challenge associated with PLLs is obtaining accurate and fast estimations of the phase angle and frequency under adverse grid voltage disturbance scenarios. According to European standard EN50160, typical voltage disturbance scenarios include voltage sag, flicker, harmonics distortion, phase-angle and frequency jumps, dc offsets and noise contaminations [4]. To achieve accurate grid-synchronization under grid disturbances, several new structures to enhance the performance of PLLs have been presented [5]-[14].

In addition to the use of these new structures, a more general approach to improving the performance of a PLL is to combine them with filters [15]-[36], such as extended Kalman filters (EKFs) [15], space vector filters (SVFs) [16], notch filters [17], digital filters [18], complex-coefficient filters (CCF) [19], the delayed signal cancellation (DSC) block method [20]-[24], and MAF-based methods [25]-[36]. Among these filtering techniques, DSC and MAF show similar filtering characteristics. They can almost completely block specific frequency signals. From the view point of the discrete implementation of DSC and MAF, they are both composed of a number of particular delay blocks. However,

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DSC is often used to improve the performance of a PLL under adverse grid conditions [23]. In [24], a comparison of MAF and DSC, as well as their derived methods, was presented in terms of the dynamic response, steady-state performance, required data size, and harmonic and noise immunity capability. In [25], the dqCDSC-PLL and the MAF-PLL algorithms were shown to be mathematically equivalent under certain conditions.

The MAF technique is the most popular and widely used technique (it can be used in the natural *abc* coordinates, the $\alpha\beta$ coordinates and the *dq* coordinates) owing to its simple digital realization, low computational burden, and effectiveness under grid disturbance conditions [26]. However, the open-loop bandwidth of a PLL is drastically reduced after incorporating a MAF into its structure. This may be beneficial in terms of stability, but it degrades the dynamic performance of the PLL. To solve this problem, some advanced MAF-based PLL algorithms have been presented [27]-[36].

In [26], a detailed analysis and design guideline of a MAF-PLL and its frequency adaptive implementation were presented, in which a performance comparison of the well-tuned MAF-based PLL with a PI controller and the PID controller was presented. It was shown that the PID-type MAF-PLL has a higher bandwidth, which means a faster dynamic response while decreasing the noise immunity and disturbance rejection capability. In [27] a critical comparison between PLLs and FLLs based on the MAF, CDSC and DSOGI filtering techniques was presented. It is shown that these kinds of filtering techniques can all effectively remove noise, harmonics and negative sequence, and that the initial phase angle detector with a MAF-based PLL shows the best performance under frequency and phase angle jump scenarios. A novel MAF-based PLL consisting of a frequency detector and an initial phase was presented in [28], in which the effect of discrete sampling on the MAF is analyzed and a linear interpolation is employed to enhance the performance of the MAF. In [29], an enhanced MAF (EMAF) algorithm was presented, which shows superior performance in terms of response time, transient overshoot, computational load, harmonics and noise immunity compared with the DSC algorithm.

In [30], a MAF and a weighted least squares estimation (WLSE) scheme based PLL was proposed, in which the MAF was used to filter out all of the odd-order harmonics and to help the WLSE detect the fundamental positive-sequence components accurately even under heavily distorted grid conditions. In [31], a MAF was used as a perfiltering stage in the *dq*-frame (PMAF-PLL) to remove the negative sequence and odd-order harmonic components, and then an enhanced method was proposed to improve the steady-state performance under frequency varying conditions. Furthermore, a small-signal model of the PMAF-PLL was presented, and it has been shown that the PMAF-PLL and the space-vector Fourier transform-based PLL (SVFT-PLL) are theoretically equivalent. In [32], a novel design of a low-gain PLL introducing an adaptive MAF before the loop-filter (LF) and its discrete domain model were presented. Compared with the conventional high gain SRF-PLL, the phase and voltage frequency error is reduced and the phase angle tracking is faster and more accurate.

In [33], a quasi-type-1 PLL (QT1-PLL) was presented. In this structure, the proportional integral (PI) controller was replaced by a simple gain. Thus, a larger open-loop bandwidth can be realized. However, the QT1-PLL cannot filter out the dc offset or even order harmonics. In order to tackle this problem, a hybrid PLL (HPLL) was presented in [34]. In this HPLL, delayed signal cancellation (DSC) is used in the $\alpha\beta$ axis to eliminate the dc offset and even order harmonics. The phase error compensation (PEC) method was adopted for the QT1-PLL and HPLL to achieve zero steady-state error when frequency jumps occur. In [35], a MAF-PLL with a phase-lead compensator (MPLC-PLL) was presented. With a phase-lead compensator in the control loop, the dynamic response of the standard MAF-PLL can be effectively improved without deteriorating its disturbance rejection capabilities. A differential MAF-PLL (DMAF-PLL) was presented in [36]. With this approach, a special loop filter structure was used to eliminate the negative sequence 2nd order harmonics in order to reduce the window length of the MAF and to significantly improve the dynamic performance of the PLL.

The main objective of this paper is to provide performance evaluations (including the transient response and disturbance rejection capabilities) of four MAF-based PLLs (QT1-PLL, HPLL, MPLC-PLL, and DMAF-PLL) by analytical comparisons and experimental results. The steady-state and dynamic performances of these algorithms are compared in terms of settling time, phase tracking error and overshoots. Experimental results show that the QT1-PLL and MPLC-PLL lack the rejection capabilities of dc offset and even order harmonics. These are the main shortcomings of these algorithms, which can be overcome by employing a DSC in the $\alpha\beta$ coordinates or a MAF in the *abc* coordinates. In the last section, an amplitude error compensation (AEC) method is proposed to achieve zero steady-state error for the positive sequence amplitude estimation under frequency jump conditions. Extensive experimental results are provided for validation. This facilitates the practical application of these MAF-based PLLs for achieving accurate grid-synchronization of the three-phase grid-connected PWM inverters and distributed generators (DGs) in smartgrids.

II. Overview of MAF-Based PLLs

In this Section, a brief overview of the MAF is outlined. In

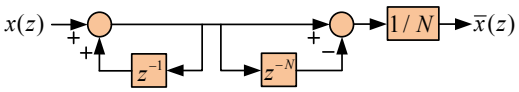

Fig. 1. The realization of MAF in z-domain.

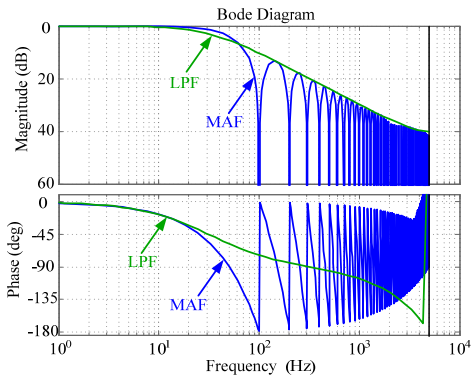

Fig. 2. Bode diagram comparison of MAF and first-order LPF.

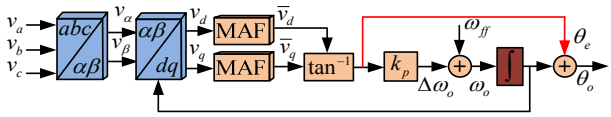

Fig. 3. Block diagram of the QT1-PLL proposed in [33].

addition, four MAF-based PLL algorithms and discrete models are described.

A. Moving Average Filter (MAF)

The transfer function of the MAF can be obtained simply in the *s*-domain and the *z*-domain as [19]:

$$G_{MAF}(s)=\frac{\bar{x}(s)}{x(s)}=\frac{1-e^{-T_\omega s}}{T_\omega s}\approx\frac{2}{T_\omega s+2} \tag{1}$$

$$G_{MAF}(z)=\frac{\bar{x}(z)}{x(z)}=\frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}} \tag{2}$$

where T_ω represents the window length. In addition, $T_\omega=NT_s$, T_s is the sample time that is set to 0.0001 s, and N is an integer. Transfer function (1) shows that the MAF requires a time equal to its window length to gather data and reach steady-state conditions. Therefore, a smaller window length results in a faster dynamic response of the MAF-based PLL algorithms.

As shown in (2), the application of a MAF in the z-domain is computationally efficient with simple delay blocks [26], as shown in Fig. 1. From the aforementioned analysis, the delay factor N can be set as a constant to remove the fixed frequency signal or as frequency adaptive according to the equation $N=round\ (m\pi/\omega_0 T_s)$, in which the MAF is used to remove the odd-order harmonic for m=1, and to remove the dc offset for m=2. The detailed discrete-time realization was discussed in [26].

Using the transfer functions (1) and (2), a bode diagram of a MAF and a low-pass filter (LPF) is shown in Fig. 2, in which T_ω is set to 0.01 s (N=100) and the corresponding cutoff frequency in the LPF is 200 rad/s. This shows that the even order harmonics are effectively eliminated since the MAF has a high attenuation at these harmonic frequencies.

B. QT1-PLL

Fig. 3 shows the general structure of the QT1-PLL, in which a MAF cascading a proportional controller act as the loop filter. Thus, from the view point of the structure, the QT1-PLL is a type-I PLL, which has a high stability margin compared with the typical MAF-PLL (in which a MAF and a PI controller act as the loop filter). However, the main disadvantage of a conventional type-I PLL lies in the phase tracking error under the grid frequency step condition.

As shown in Fig. 3, three-phase grid voltages with a dc offset and harmonics can be defined as (here, the symmetrical load is taken into consideration, which corresponds to the -5th, +7th, -11th, and +13th order harmonics):

$$\begin{cases} v_a=V_{a,dc}+\sum\limits_{h=1,-5,7\ldots}[V_h^+\cos(\theta_h^+)+V_h^-\cos(\theta_h^-)] \\ v_b=V_{b,dc}\sum\limits_{h=1,-5,7\ldots}[V_h^+\cos(\theta_h^+-\frac{2\pi}{3})+V_h^-\cos(\theta_h^-+\frac{2\pi}{3})] \\ v_c=V_{c,dc}+\sum\limits_{h=1,-5,7\ldots}[V_h^+\cos(\theta_h^++\frac{2\pi}{3})+V_h^-\cos(\theta_h^--\frac{2\pi}{3})] \end{cases} \tag{3}$$

where $V_h^+(V_h^-)$ and $\theta_h^+(\theta_h^-)$ are the amplitude and phase-angle of the hth harmonic components of the positive- (negative-) sequence of the input voltages, respectively. $V_{a,dc}$, $V_{b,dc}$ and $V_{c,dc}$ are the dc offset added to the phase-a, phase-b and phase-c voltages, respectively.

Applying the Clarke transformation to (3), v_α and v_β can be written as:

$$\begin{cases} v_\alpha=V_{\alpha,dc}+\sum\limits_{h=1,-5,7\ldots}[V_h^+\cos(\theta_h^+)+V_h^-\cos(\theta_h^-)] \\ v_\beta=V_{\beta,dc}+\sum\limits_{h=1,-5,7\ldots}[V_h^+\sin(\theta_h^+)-V_h^-\sin(\theta_h^-)] \end{cases} \tag{4}$$

$$\begin{cases} V_{\alpha,dc}=(V_{a,dc}-0.5V_{b,dc}-0.5V_{c,dc}) \\ V_{\beta,dc}=\frac{\sqrt{3}}{2}(V_{b,dc}-V_{c,dc}) \end{cases} \tag{5}$$

Then, applying the Park transformation to (4), v_d and v_q can be written as:

$$\begin{cases} v_d=g(\theta_0')+\sum\limits_{h=1,-5,7\ldots}[V_h^+\cos(\theta_h^+-\theta_0')+V_h^-\cos(\theta_h^-+\theta')] \\ v_q=h(\theta_0')+\sum\limits_{h=1,-5,7\ldots}[V_h^+\sin(\theta_h^+-\theta_0')-V_h^-\sin(\theta_h^-+\theta')] \end{cases} \tag{6}$$

where $g(\theta_0')$ and $h(\theta_0')$ are the oscillating terms caused by the grid voltage dc offset, where:

$$\begin{cases} g(\theta_0')=V_{\alpha,dc}\cos(\theta_0')+V_{\beta,dc}\sin(\theta_0') \\ h(\theta_0')=-V_{\alpha,dc}\sin(\theta_0')+V_{\beta,dc}\cos(\theta_0') \end{cases} \tag{7}$$

Under a quasi-locked condition ($\theta_1^+=\theta_0'$), (6) can be rewritten as:

$$\begin{cases} v_d=V_1^++f(\omega_n,2\omega_n,6\omega_n\ldots) \\ v_q=V_1^+(\theta_1^+-\theta_0')+f(\omega_n,2\omega_n,6\omega_n\ldots) \end{cases} \tag{8}$$

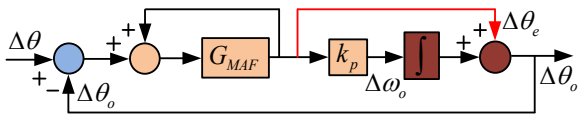

Fig. 4. Small-signal model of the QT1-PLL [33].

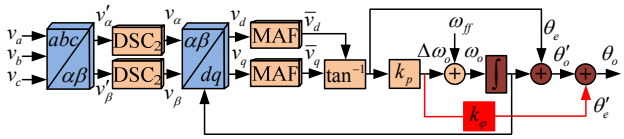

Fig. 5. Block diagram of the HPLL proposed in [34].

where ω_n is the fundamental angular frequency. Through the use of a MAF, the oscillating term $f(\omega_n, 2\omega_n, 6\omega_n\ldots)$ can be nearly removed. As mentioned earlier, a type-I PLL cannot achieve zero steady-state error when a frequency jump occurs. Hence, the phase tracking error of a type-I PLL under a frequency jump is expressed as [33]:

$$\theta_e = \frac{\Delta\omega_i}{k_p} \tag{9}$$

From equation (9), by selecting a sufficiently high value for k_p, the phase error θ_e can be reduced to a very small value. However, this selection increases the PLL's bandwidth remarkably which is not preferred under distorted and unbalanced grid voltage conditions. Notice that the average value of $\Delta\omega_o$ is equal to $\Delta\omega_i$ under locked conditions. Thus, as highlighted in Fig. 3, the phase tracking error is added to the output of the PLL to realize zero steady-state tracking error when a frequency jump occurs.

Fig. 4 shows a small signal model of the QT1-PLL. Since the s-domain transfer function has been expressed in [33], and considering practical application, the open-loop transfer function in the z-domain is expressed as:

$$G_{ol}^{QT1}(z) = \left(\frac{G_{MAF}(z)}{1-G_{MAF}(z)}\right)\left(\frac{z-1+T_s k_p}{z-1}\right) \tag{10}$$

As shown in (8), where the lowest oscillating frequency is ω_n=50 Hz (in a 50 Hz system) by selecting T_ω=0.02 s (i.e., N=200), the oscillating term can be removed completely. However, this selection may lead to a slow dynamic response. In order to achieve a tradeoff between the response speed and the filtering capability, the window length of the MAF is set to 0.01 s (i.e., N=100), which means that the MAF block cannot remove the fundamental frequency oscillation caused by the dc offset.

C. HPLL

Fig. 5 shows the general structure of the HPLL presented in [34] to overcome the main drawback of the QT1-PLL under dc offset and even-order harmonics scenarios. The main difference between the HPLL and the QT1-PLL is the application of delay signal cancellation (DSC) in the $\alpha\beta$ axis ($\alpha\beta$DSC). From Fig. 5, the $\alpha\beta$DSC input signals v'_α and v'_β are shown in (4). In order to filter out the dc offset ($V_{\alpha,dc}$, $V_{\beta,dc}$),

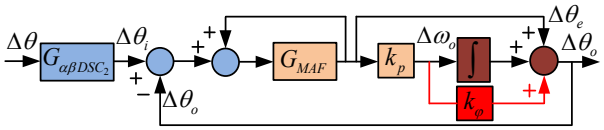

Fig. 6. Small-signal model of the HPLL [34].

the transfer function of the $\alpha\beta$DSC applied in the HPLL can be defined in the Laplace-domain as [23]:

$$G_{\alpha\beta\mathrm{DSC}_2}(s) = \frac{1}{2}(1-e^{-\frac{T}{2}s}) \tag{11}$$

where T=0.02 s is the fundamental period of the grid voltages.

Substituting $s=j\omega$ into (11), yields:

$$G_{\alpha\beta\mathrm{DSC}_2}(j\omega) = \left|\sin(\frac{\omega T}{4})\right| \angle(\frac{\pi}{2} - \frac{\omega T}{4}) \tag{12}$$

From (12), it can be observed that the $\alpha\beta\mathrm{DSC}_2$ operator has a unity gain and zero phase-shift at 50 Hz, and provides zero gain at zero frequency and all of the even order harmonic frequencies. This implies that $G_{\alpha\beta\mathrm{DSC2}}$ blocks all of the dc offset and even order harmonics.

Therefore, v_α and v_β can be written as:

$$\begin{cases} v_\alpha = \sum\limits_{h=1,-5,7\ldots} [V_h^+ \cos(\theta_h^+) + V_h^- \cos(\theta_h^-)] \\ v_\beta = \sum\limits_{h=1,-5,7\ldots} [V_h^+ \sin(\theta_h^+) - V_h^- \sin(\theta_h^-)] \end{cases} \tag{13}$$

Generally, $G_{\alpha\beta\mathrm{DSC2}}$ can be designed to be frequency adaptive to achieve zero steady-state error under the frequency jump scenario. However, this feedback loop makes it rather difficult to ensure system stability. In order to solve this problem, the phase error is compensated by the PLL output. In order to compensate the phase shift caused by the $G_{\alpha\beta\mathrm{DSC2}}$ block under frequency jump scenarios, assuming that $\Delta\omega_i$ is the deviation value of the grid frequency from the nominal grid frequency, the phase shift can be obtained as:

$$\angle\alpha\beta\mathrm{DSC}_2(j\omega_i) = -\frac{T}{4}\Delta\omega_i \tag{14}$$

This phase-error can be easily compensated, as shown in Fig. 5, where $k_\varphi = T/4$ can be selected.

The small signal model of the HPLL is shown in Fig. 6. The open-loop transfer function in the z-domain can be derived as:

$$G_{ol}^{HPLL}(z) = \left(\frac{G_{MAF}(z)}{1-G_{MAF}(z)}\right)\left(1 + k_p k_\varphi + \frac{T_s k_p}{z-1}\right) \tag{15}$$

Since the dc offset has been removed by $G_{\alpha\beta\mathrm{DSC2}}$, the lowest frequency that needs to be filtered out is $2\omega_n$=100 Hz. Therefore, the window length of the MAF is set to T_ω=0.01 s.

D. MPLC-PLL

Fig. 7 shows the general structure of the MPLC-PLL derived from the conventional MAF-PLL. The phase-lead compensator, as highlighted by G_c in Fig. 7, is applied in the control loop to effectively compensate the control delay caused by the MAF. The expressions of v_d and v_q are shown

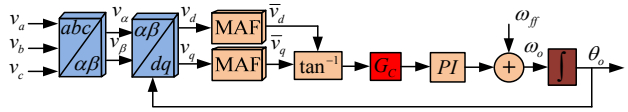

Fig. 7. Block diagram of the MPLC-PLL proposed in [35].

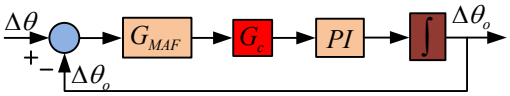

Fig. 8. Small-signal model of the MPLC-PLL [35].

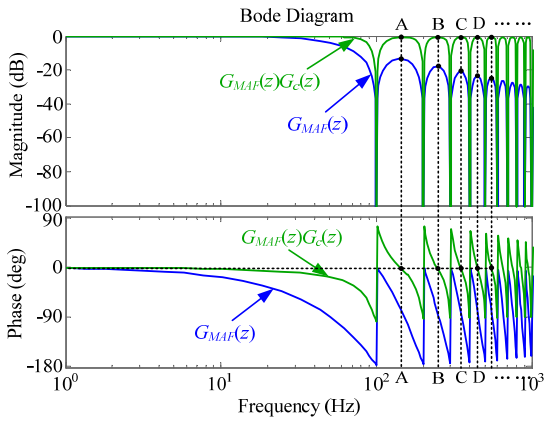

Fig. 9. Bode diagram of the MAF and the cascade connection of MAF and phase-lead compensator.

in (8). The transfer function of this compensator can be derived as:

$$G_c(z) = k\frac{1-rz^{-1}}{1-r^N z^{-N}} \tag{16}$$

where r is the attenuation factor, N is defined in equation (2), and $k=(1-r^N)/(1-r)$.

The small signal model of the MPLC-PLL is shown in Fig. 8. The open-loop transfer function in the z-domain can be derived as:

$$G_{ol}^{MPLC}(z) = G_{MAF}(z)G_c(z)PI(z)\frac{T_s}{z-1} \tag{17}$$

where the window length T_ω is set to 0.01 (i.e., N=100, this selection also ignores the dc offset), and the attenuation factor r is set to 0.99.

From Fig. 9, it can be observed that MAFs with and without the phase-lead compensator have similar filtering features at frequency $f=100n$ (n=1, 2, 3, …). However, under other grid frequencies, especially at the frequency points A, B, C, D, and so on, a MAF with the phase-lead compensator may almost pass all of these frequency signals without any change compared with the typical MAF. This means that the phase-lead compensator actually amplifies the frequency signal $f\neq100n$ (n=1, 2, 3, …), which decreases the frequency adaptive of the MPLC-PLL under harmonics in off-nominal frequency scenarios.

E. DMAF-PLL

Fig. 10 shows the general structure of the DMAF-PLL.

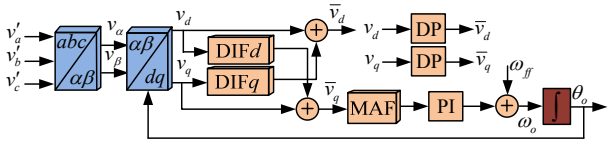

Fig. 10. Block diagram of the DMAF-PLL proposed in [36].

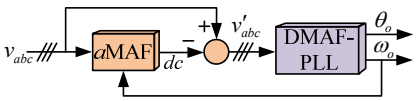

Fig.11. Block diagram of DMAF-PLL used in the experiment.

The 'DP' represents the decoupling transfer function. The expressions of v_α and v_β are shown in (13). Fig. 11 shows the block diagram of the PLL structure used in the experiment, where one additional MAF (hereafter called *a*MAF) is added before the DMAF-PLL. Therefore, the DMAF-PLL input signal $v_{abc}^{'}$ is free of dc offset.

In [36], the *a*MAF block is designed to be frequency-adaptive using the rounding-down method $N=round(m\pi/\omega_0 T_s)$, where m=2. Although this structure can effectively filter out the dc offset, the *a*MAF requires a time interval of 0.02 s to reach the steady-state condition. In Fig. 10, the transfer functions of DIF*d* and DIF*q* are:

$$G_{DIFd}(s) = -\frac{s}{2\omega_n}, G_{DIFq}(s) = \frac{s}{2\omega_n} \tag{18}$$

Since v_q has a 90° phase lag compared with v_d, it can be obtained that $v_d/v_q=j$. Thus, substituting $s=j\omega$ into (18) and performing a simple mathematical operation [36], it is possible to get:

$$G_{DP}(j\omega) = 1+\frac{j(-j\omega)}{2\omega_n} = 1+\frac{\omega}{2\omega_n} \tag{19}$$

Substituting $\omega=-2\omega_n$ into (19), the value of DP becomes zero, which implies that the DP eliminates the negative sequence 2nd order harmonics. Therefore, from (4), $\bar{v}_d$ and $\bar{v}_q$ can be expressed as:

$$\begin{cases} \bar{v}_d = V_1^+ + f(6\omega_n...) \\ \bar{v}_q = V_1^+(\theta_h - \theta_0') + f(6\omega_n...) \end{cases} \tag{20}$$

From (20), the lowest order harmonics that needs to be blocked is the 6th order harmonic. Then, T_ω is reduced to 1/300 s from 0.01 s, which significantly improves the response speed.

The small signal model of the DMAF-PLL is shown in Fig. 11. The decoupling transfer function *DP* in the *z*-domain can be denoted as:

$$G_{DP}(z) = Z\{G_{DP}(s)\} \tag{21}$$

Therefore, the open-loop transfer function of the DMAF-PLL in the z-domain can be written as:

$$G_{ol}^{DMAF}(z) = G_{DP}(z)G_{MAF}(z)PI(z)\frac{T_s}{z-1} \tag{22}$$

It should be noted that the window length T_ω in the MAF is calculated as 1/300, which results in approximately N=33.

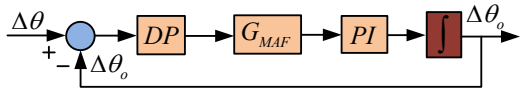

Fig. 12. Small-signal model of the DMAF-PLL [36].

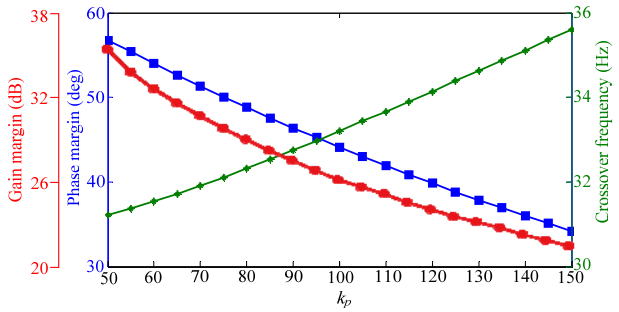

Fig. 13. The PM, CF, and GM of (5) as a function of k_p in z-domain.

Thus, when the grid voltages are contaminated by harmonics, a small ripple may exist in the estimated frequency and phase angle.

III. Parameters Design Guidelines

In this Section, the control parameters design method of the MAF-based PLL is presented. Then, the frequency domain analysis of the PLL algorithms is outlined.

In order to simplify the parameters design procedure, the parameters k_p and k_i are designed in the s-domain. Then a discrete model and z-domain bode diagrams are used to test and adjust the control parameters. Therefore, the stability and disturbance rejection capabilities of the PLLs are ensured. The expression of the MAF is approximated by a LPF, as shown in (1), and the PI regulator is denoted as k_p+k_i/s. Thus, for the QT1-PLL, the open-loop transfer function can be derived as:

$$G_{ol}(s) \approx \frac{2}{T_\omega}\frac{(s+k_p)}{s^2} \tag{23}$$

From (23), the proportional gain k_p is the only parameter that needs to be designed in the QT1-PLL and HPLL, since the MAF window lengths have already been selected. Hence, the closed- loop transfer function can be derived as:

$$G_{cl}(s) \approx \frac{2}{T_\omega}\frac{(s+k_p)}{s^2+(2/T_\omega)s+2k_p/T_\omega} \tag{24}$$

By comparing to the standard second order system, it is possible to obtain:

$$2/T_\omega = 2\xi\omega_n',\ 2k_p/T_\omega = \omega_n'^2 \tag{25}$$

where ξ is the damping factor, and ω_n' is the natural frequency.

Substituting T_ω=0.01 s and ξ=0.707 into (25), yields k_p≈100. The next step is to adjust k_p on the basis of the real transfer function in the z-domain, as shown in (10) and (15). Since the value of k_φ in (15) is small, the expressions (10) and (15) are almost identical.

Thus, the phase margin (PM), crossover frequency (CF), and gain margin (GM) of (10) as functions of k_p are derived, as shown in Fig. 13. It can be seen that when k_p varies from 50 to 150, the PM (blue line) varies from 56.7° to 34.2°, and the GM (red line) varies from 35.9 dB to 21.9 dB, which is suitable to ensure a sufficient stability margin. The CF (green line) shows a relatively smooth change (from 31.2 Hz to 35.5 Hz), which is much higher than the conventional PLLs, and a fast dynamic response can be guaranteed. Therefore, k_p=92 is selected for the QT1-PLL and k_p=94 is selected for the HPLL.

TABLE I
Parameters of the MAF-Based PLL Algorithms

	QT1-PLL	HPLL	MPLC-PLL	DMAF-PLL
N(MAF)	100	100	100	33
k_p	92	94	177.71	250
k_i	--	--	15791	26041
r	--	--	0.99	--
k_φ	--	0.005	--	--
$N(a$MAF)	--	--	--	*round* $(2\pi/\omega_0 T_s)$
$n(\alpha\beta$DSC)	--	2	--	--

As for the MPLC-PLL, a cascade connection of the MAF and a phase-lead compensator provides a gain that is close to unity with a near zero phase shift in a low frequency range [35]. Therefore, the transfer function (17) can be approximated by a typical type-2 system. It can be obtained that:

$$k_p = 2\xi\omega_n',\ k_i = \omega_n'^2 \tag{26}$$

In (26), by selecting ξ=0.707 and ω_n'=2π20rad/s, k_p and k_i can be calculated.

For the DMAF-PLL, the DP is ignored at first. When the MAF is replaced by a LPF, the standard design procedure presented in [38] can be applied to design the parameters of the DMAF-PLL. Therefore, the transfer function of the DMAF-PLL is derived as:

$$G_{ol}^{DMAF} \approx \frac{2}{T_\omega}\frac{(k_p s+k_i)}{s^2(s+2/T_\omega)} \tag{27}$$

According to the symmetrical optimum method, k_p and k_i can be expressed as:

$$2/T_\omega = b\omega_c,\ k_p = \omega_c,\ k_i = \omega_c^2/b \tag{28}$$

where ω_c is the cutoff angle-frequency, and b is a constant which should be 2.4 [37]. In [36], T_ω=0.0033 s, and ω_c is set to 250 rad/s. Therefore, k_p and k_i can be calculated. According to the aforementioned parameters design method, the control parameters of the four MAF-based PLL algorithms are summarized in Table I.

A bode diagram of the QT1-PLL, HPLL, MPLC-PLL, and DMAF-PLL is obtained by using the open-loop transfer functions of (10), (15), (17), and (22), as shown in Fig. 14. It can be noticed from Fig. 14 that the QT1-PLL (blue solid line) and the HPLL (green dot line) show almost the same frequency response, because the difference between QT1-PLL and the HPLL lies mainly in coordinate transformation instead of the control loop. The crossover frequencies (CFs)

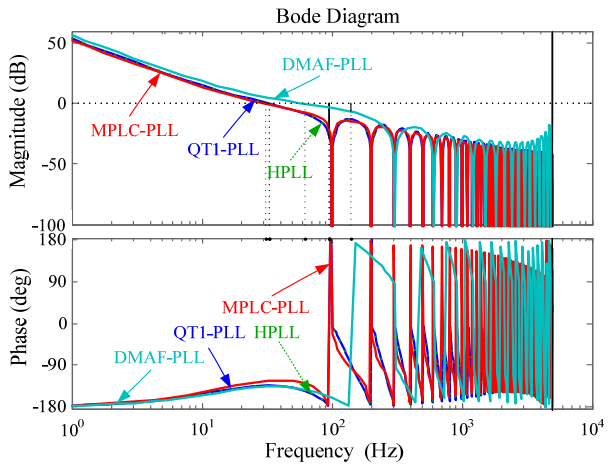

Fig. 14. Bode diagram of open-loop transfer functions of the MAF-based PLLs.

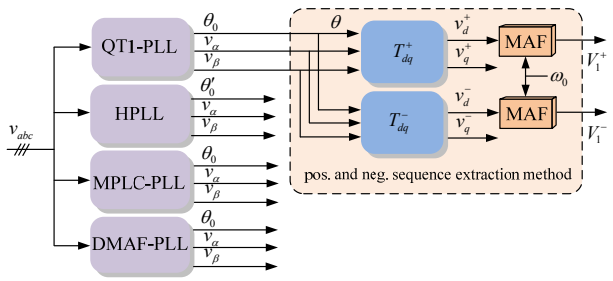

Fig. 15. Block diagram of the fundamental frequency positive and negative sequence amplitude extraction.

of the QT1-PLL and the HPLL are both 32.9 Hz, which ensures a relatively fast dynamic response. The GM and PM are 27.6 dB and 45.5°, respectively, which ensures a sufficient stability margin of these PLLs.

The MPLC-PLL (red solid line) shows a similar frequency response compared with the QT1-PLL and HPLL. In addition, the CF of the MPLC-PLL is approximately 30.7 Hz, which is much higher compare with the conventional MAF-based PLL. The GM and PM are 20.4 dB and 55°, respectively, which is the desired stability margin. However, the DMAF-PLL shows a different frequency response compared with the other three PLL algorithms due to the difference between the MAF window lengths. The CF of the DMAF-PLL is the highest (about 62 Hz) due to its small window length and high proportional gain. In addition, the system GM and PM are 6.61 dB and 37.7°, respectively.

In the high frequency range, the four PLLs show similar amplitude-frequency characteristics. The DMAF-PLL algorithm almost blocks the high frequency components of the integer multiples of 300 Hz. However, for the other three PLLs, it is 100 Hz.

IV. Sequence Extraction Methods

Fig. 15 shows a block diagram of the fundamental frequency positive (pos.) and negative (neg.) sequence

Fig. 16. Photo of the experimental set-up [38, 39].

amplitude extraction. The extraction method is shown in the dotted frame in which four input signals θ, v_α, v_β, and ω_0 are required. For the HPLL, it should be noticed that the phase-angle used for amplitude extraction is θ_d' (not θ_0). If θ_0 is used, the input voltage should be v_α' and v_β' (not v_α, and v_β). However, this selection makes the extraction procedure sluggish. The signals mentioned in this section are all shown in the corresponding block diagram of each PLL. The transformation matrix to extract the positive and negative sequence is expressed as:

$$T_{dq}^{+}=\begin{bmatrix}\cos(\theta) & \sin(\theta)\\ -\sin(\theta) & \cos(\theta)\end{bmatrix},\ T_{dq}^{-}=\begin{bmatrix}\cos(\theta) & -\sin(\theta)\\ \sin(\theta) & \cos(\theta)\end{bmatrix} \quad (29)$$

Thus, v_d^+ and v_d^- can be expressed as:

$$v_d^+=\begin{cases}V_1^+ + f(2\omega_n, 6\omega_n \ldots) & \text{HPLL, DMAF-PLL}\\ V_1^+ + f(\omega_n, 2\omega_n, 6\omega_n \ldots) & \text{QT1-PLL, MPLC-PLL}\end{cases} \quad (30)$$

$$v_d^-=\begin{cases}V_1^- + f(2\omega_n, 6\omega_n \ldots) & \text{HPLL, DMAF-PLL}\\ V_1^- + f(\omega_n, 2\omega_n, 6\omega_n \ldots) & \text{QT1-PLL, MPLC-PLL}\end{cases} \quad (31)$$

where f is the oscillating term caused by the unbalanced grid voltage, harmonics, and dc offset.

The MAF window length is set to be frequency adaptive (the estimated period is $2\pi/\omega_0$). Therefore, the accuracy of the frequency estimation affects the accuracy of the positive and negative sequence components extraction to a large extent.

V. Experimental Results and Discussions

The aim of this section is to evaluate the performances of the four PLLs under different grid voltage disturbance scenarios which are generated by a grid simulator using a three-phase voltage source inverter (VSI) controlled in the voltage control mode (VCM) [38]. To validate the analysis, an experimental prototype was built based on a 2.2 kW Danfoss inverter controlled in the VCM using a LCL output filter with a resistive load, where the capacitor voltage of the LCL filter was controlled to synthesize the virtual grid conditions. The inverter PWM frequency was set to 10 kHz in order to evaluate the PLL algorithms with a discrete time-step of 100 microseconds, as analyzed in this paper.

A dSPACE1006 platform was utilized to implement the

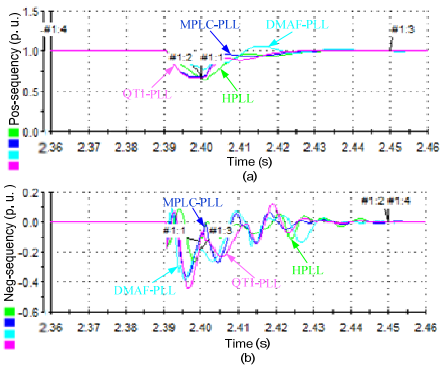

Fig. 17. Estimated pos. and neg. sequence amplitudes under +90° phase-angle jump.

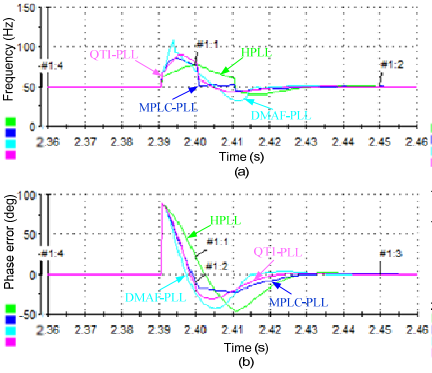

Fig. 18. Estimated frequency and phase error under +90° phase-angle jump.

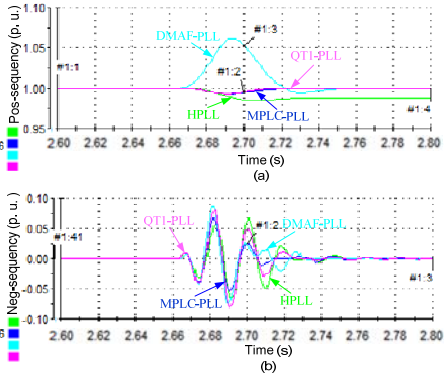

Fig. 19. Estimated pos. and neg. sequence amplitudes under frequency jump of +5 Hz.

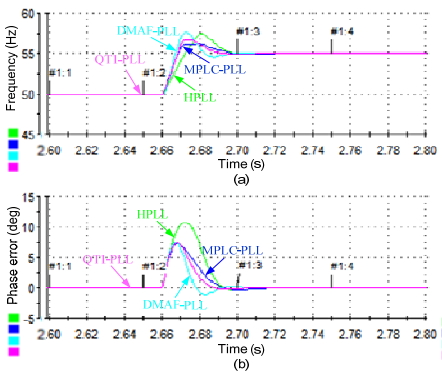

Fig. 20. Estimated frequency and phase error under frequency jump of +5 Hz.

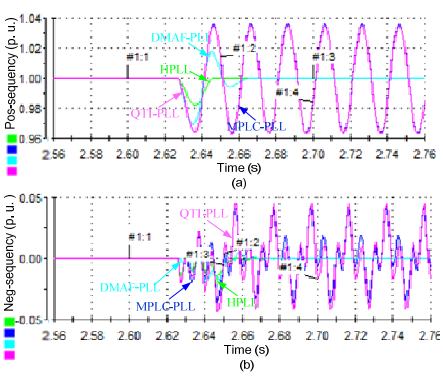

Fig. 21. Estimated pos. and neg. sequence amplitudes under dc offset.

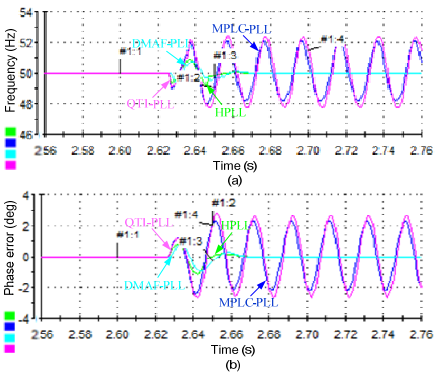

Fig. 22. Estimated frequency and phase error under dc offset.

Simulink-based control algorithms and the compiled executable file was downloaded to the dSPACE1006 controller to extract real-time grid-synchronization signals. The binary word size was only several kilobytes (kB) when the VCM was adopted for the inverter control and the four PLL algorithms were implemented, which facilities practical implementation in both fixed point and floating point digital signal processors (DSPs) [see Fig. 16] [39]. Detailed comparisons of the four PLL under different grid disturbance scenarios are shown in Table II and Table III.

Case 1. Performance Comparison under 90° Phase-Angle Jumps

Fig. 17 shows the positive and negative sequence amplitudes, and Fig. 18 illustrates the estimated frequency and phase estimation error under phase-angle jumps of +90°. It can be noticed all of the PLLs can achieve zero steady-state error of the amplitude, frequency and phase in 2.5 cycles. However, the DMAF-PLL shows an overshoot of 60 Hz in the estimated frequency, and the HPLL shows the smallest overshoot (about 28 Hz). In terms of phase-angle estimation, the HPLL shows an overshoot of about 50°, and the MPLC-PLL shows the smallest overshoot (about 20°).

Case 2. Performance Comparison under +5 Hz Frequency Jumps

Fig. 19 shows the positive and negative sequence amplitudes under frequency jumps of +5 Hz. It can be seen that all of the PLLs can achieve zero steady-state error in the positive sequence except for the HPLL, where the steady-state error is caused by the non-frequency adaptive DSC. In the negative sequence frame, all of the PLLs can achieve zero steady-state error in about 3 cycles.

Fig. 20 illustrates the estimated frequency and phase estimation error under frequency jumps of +5 Hz. Similar results are achieved for the four PLLs and the estimated frequency is locked to the rated value in about 2 cycles. The HPLL and the DMAF-PLL show similar overshoots of about 2.5 Hz. In terms of phase-angle estimation, the HPLL has the largest overshoot (12°), and other three PLLs show an overshoot of about 8°.

Case 3. Performance Comparison under DC Offset

Fig. 21 shows the positive and negative sequence amplitudes under dc offset. Due to the application of *a*MAF in the DMAF-PLL and DSC in the HPLL, the two PLLs can achieve zero steady state error in the positive and negative sequence amplitudes. However, for the QT1-PLL and the MPLC-PLL, noticeable fundamental frequency oscillations can be observed in the positive and negative sequence amplitudes. Fig. 22 illustrates the estimated frequency and the phase estimation error under dc offset. Because the MAF in the QT1-PLL and the MPLC-PLL cannot filter out the

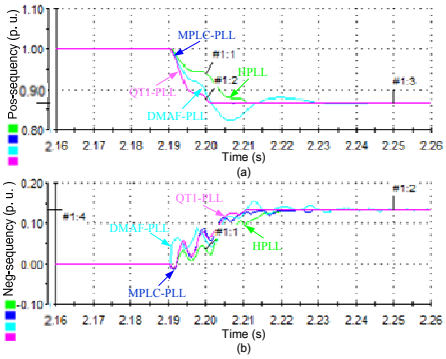

Fig. 23. Estimated pos. and neg. sequence amplitudes under single-phase voltage sag.

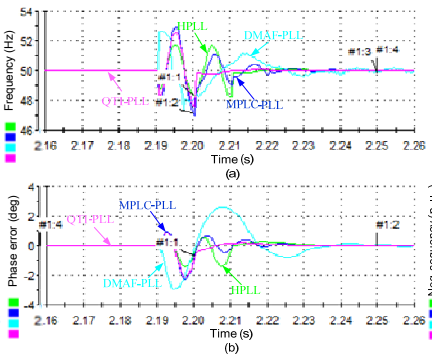

Fig. 24. Estimated frequency and phase error under single-phase voltage sag.

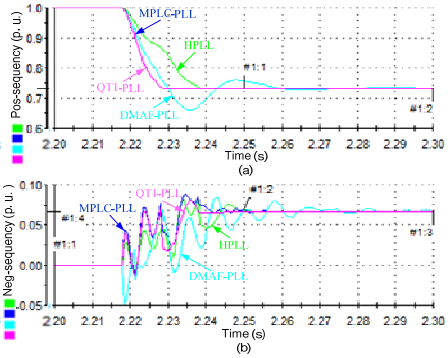

Fig. 25. Estimated pos. and neg. sequence amplitudes under two-phase voltage sag.

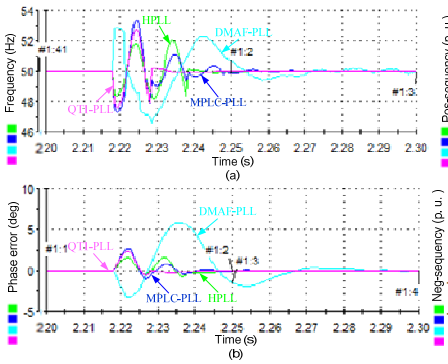

Fig. 26. Estimated frequency and phase error under two-phase voltage sag.

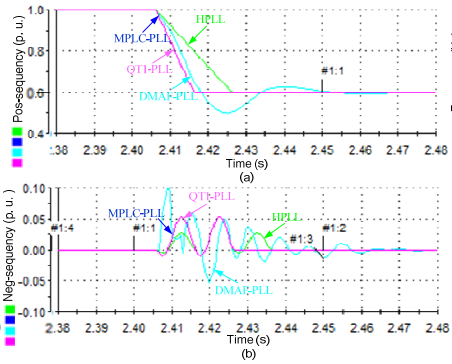

Fig. 27. Estimated pos. and neg. sequence amplitudes under three-phase voltage sag.

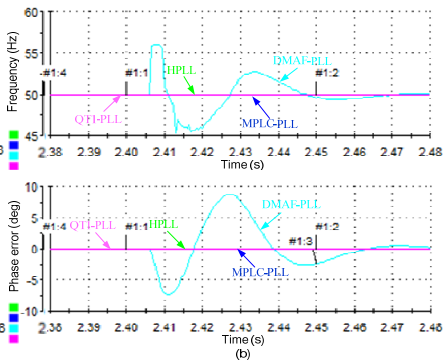

Fig. 28. Estimated frequency and phase error under three-phase voltage sag.

fundamental frequency oscillations caused by dc offset, the two PLLs show similar fluctuations both in the estimated frequency and the phase angle. For the HPLL, the estimated frequency is locked to the rated value in about one cycle. However, for the DMAF-PLL, a longer response time is needed (about 2 cycles) to achieve zero steady-state error due to the large window length of the *a*MAF.

Case 4. Performance Comparison under a 0.4 p.u. Single-Phase Voltage Sag

Fig. 23 shows the positive and negative sequence amplitudes under a 0.4 p.u. single-phase voltage sag. It shows that all of the PLLs achieve zero steady-state error in both the positive and negative sequence amplitudes, which shows the fastest dynamic response. However, the DMAF-PLL algorithm shows the slowest transient response due to the use of *a*MAF.

Fig. 24 illustrates the estimated frequency and phase estimation error under a 0.4 p.u. single-phase voltage sag. It can be seen that the QT1-PLL shows the shortest response time (less than one cycle). However, for the DMAF-PLL, the response time is greater than 2 cycles. For the HPLL and the MPLC-PLL, the setting time is about 2 cycles. Similar transient overshoots in the frequency can be observed in the QT1-PLL, the DMAF-PLL and the MPLC-PLL (about 3 Hz), while the HPLL shows a frequency overshoot of about 1.8 Hz.

Case 5. Performance Comparison under a 0.4 p.u. Two-Phase Voltage Sag

Fig. 25 shows the estimated positive and negative sequence amplitudes, and Fig. 26 illustrates the estimated frequency and the phase estimation error under a 0.4 p.u. two-phase voltage sag. Similar to the case of a single-phase voltage sag, all of the PLLs can achieve zero steady-state error in the positive and negative sequence amplitudes, frequency and phase, and the QT1-PLL and the DMAF-PLL show the fastest and slowest dynamic responses, respectively. The highest and lowest overshoot in frequency is found in the MPLC-PLL (about 3.5 Hz) and the HPLL (about 1.5 Hz), respectively.

Case 6. Performance Comparison under a 0.4 p.u. Three-Phase Voltage Sag

Fig. 27 shows the positive and negative sequence amplitudes, and Fig. 28 illustrates the estimated frequency and the phase estimation error under a 0.4 p.u. three-phase voltage sag. In the positive and negative sequence amplitudes, the experimental waveforms are similar to the cases of single-phase and two-phase voltage sags. The estimated frequencies and phase errors of the QT1-PLL, the MPLC-PLL and the HPLL are not affected by three-phase voltage sags. However, a high overshoot of about 6 Hz in the estimated frequency and a slow dynamic response of about 3 cycles is found in the DMAF-PLL, which is mainly due to the highly nonlinear system caused by the *a*MAF.

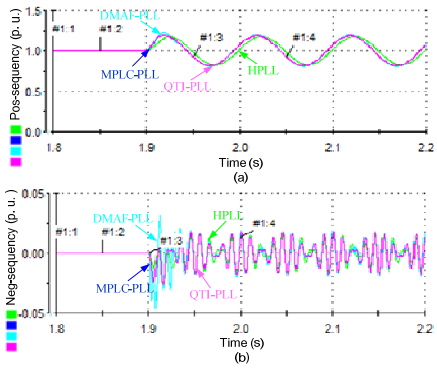

Fig. 29. Estimated pos. and neg. sequence amplitudes under voltage flicker.

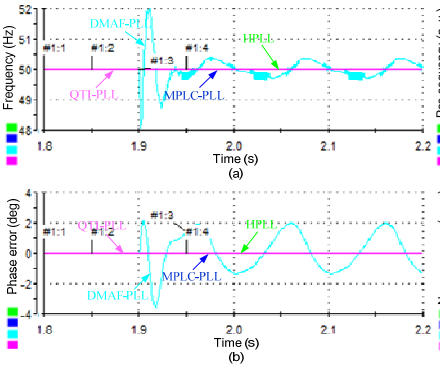

Fig. 30. Estimated frequency and phase error under voltage flicker.

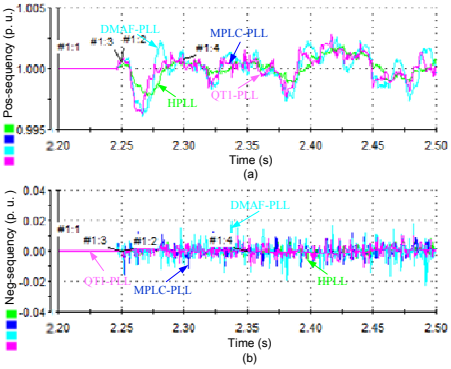

Fig. 31. Estimated pos. and neg. sequence amplitudes under noise contaminations.

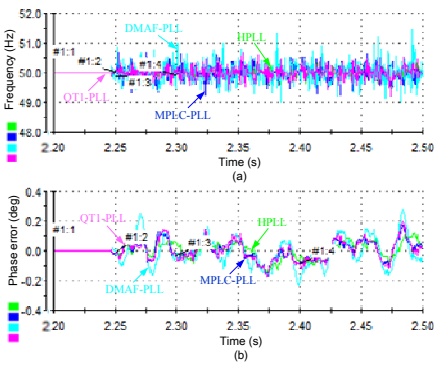

Fig. 32. Estimated frequency and phase error under noise contamination.

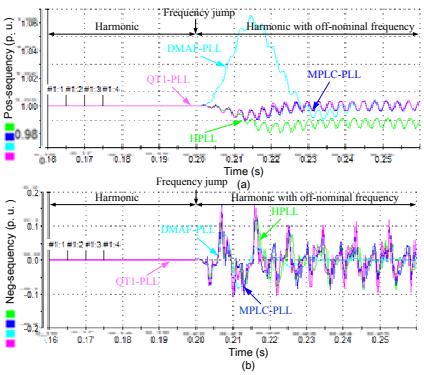

Fig. 33. Estimated pos. and neg. sequence amplitudes under harmonic with frequency jump.

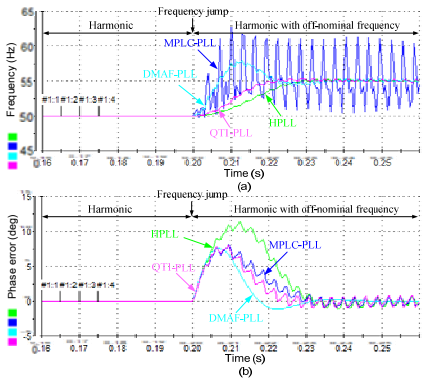

Fig. 34. Estimated frequency and phase error under harmonic with frequency jump.

Case 7. Performance Comparison under Voltage Flickers

Fig. 29 shows the positive and negative sequence amplitudes under voltage flickers. It can be observed that all of the PLLs fail to achieve zero steady-state error and an obvious ripple is found in both the positive and negative sequence amplitude.

Fig. 30 illustrates the estimated frequency and the phase estimation error under voltage flickers. Similar to the case of a three-phase voltage sag, all of the PLLs are not affected by the voltage flicker except for the DMAF-PLL, which shows steady-state oscillations both in the estimated frequency (about 1.5 Hz) and in the estimated phase angle (about 3.5°), which may also be caused by the *a*MAF.

Case 8. Performance Comparison under Noise Contaminations

To evaluate the noise immunity of the PLLs, a zero-mean Gauss white noise with a variance of σ^2=0.01 is added to the input. The signal-to-noise-ratio (SNR) is 10 log $(1/2\sigma^2)$ =17 dB. The noisy waveform is sampled at a rate of 100 kHz, and is then fed to a digital anti-aliasing filter. This high sampling rate is used to avoid the aliasing effects and to increase accuracy. A digital first-order LPF with a cutoff frequency of 4 kHz is considered as an anti-aliasing filter. The output of the anti-aliasing filter is down sampled to 10 kHz and is fed to the PLL.

Fig. 31 shows the positive and negative sequence amplitudes, and Fig. 32 illustrates the estimated frequency and phase estimation errors. It can be seen that all of the PLLs have similar peak to peak steady-state oscillations, for the estimated positive and negative sequence amplitude. They are about 0.005 p.u. and 0.04 p.u., respectively, for the estimated frequency and phase, which are about 2 Hz and 0.4°, respectively.

Case 9. Performance Comparison under Harmonics with a Frequency Jump

In order to analyze the frequency-adaptive performances of the four MAF-based PLLs, the harmonics (0.1 p.u. of the -5th, and 0.05 p.u. of the +7th, -11th, and +13th harmonics) with the frequency jump (+5 Hz) scenario are subjected to the grid voltage.

Fig. 33 shows the estimated positive and negative sequence amplitudes, and Fig. 34 illustrates the estimated frequency and phase estimation error. It can be seen that when the grid voltage only suffers from harmonics (before 0.2s), the four MAF-based PLLs can all achieve zero steady-state error in the amplitude, frequency and phase estimation. When a frequency jump occurs (0.2s), the DMAF-PLL shows the best steady-state performance with the lowest oscillation. However, the MPLC-PLL shows the biggest oscillation in the estimated frequency mainly because of the phase-lead

TABLE II
COMPARISON OF THE MAF-BASED PLLS UNDER PHASE/FREQUENCY JUMP AND VOLTAGE SAG

	QT1-PLL		HPLL		MPLC-PLL		DMAF-PLL	
	(a)	(b)	(a)	(b)	(a)	(b)	(a)	(b)
Phase-Angle Jump of +90°	36 ms	40 Hz	45 ms	25 Hz	38 ms	35 Hz	40 ms	60 Hz
Frequency Jump of +5 Hz	35 ms	1.7 Hz	37 ms	2.5 Hz	38 ms	1.3 Hz	40 ms	2.8 Hz
0.4 p. u. Single-Phase Voltage Sag	10 ms	2.5 Hz	20 ms	1.8 Hz	10 ms	3.2 Hz	43 ms	2.8 Hz
0.4 p. u. Two-Phase Voltage Sag	10 ms	2.8 Hz	20 ms	2.1 Hz	10 ms	3.4 Hz	41 ms	3.8 Hz
0.4 p. u. Three-Phase Voltage Sag	20 ms	0 Hz	20 ms	0 Hz	10 ms	0 Hz	42 ms	7.2 Hz

Note: (a) and (b) represent setting time and frequency overshoot, respectively.

TABLE III
COMPARISON OF THE MAF-BASED PLLS UNDER DC OFFSET, FLICKER, NOISE AND HARMONIC

	QT1-PLL		HPLL		MPLC-PLL		DMAF-PLL	
	(a)	(b)	(a)	(b)	(a)	(b)	(a)	(b)
DC Offset	4.6 Hz	5.2°	0 Hz	0°	4.0 Hz	4.5°	0 Hz	0°
Voltage Flicker	0 Hz	0°	0 Hz	0°	0 Hz	0°	1.5 Hz	3.3°
Noise	1.5 Hz	0.3°	1.5 Hz	0.2°	1.3 Hz	0.3°	1.9 Hz	0.5°
Harmonics without/with +5Hz	0/0.4 Hz	0°/1.6°	0/0.2 Hz	0°/1.5°	0/10.5 Hz	0°/1.4°	0.04/0.6 Hz	0.01°/0.05°

Note: (a) and (b) represent peak-to-peak frequency error and peak-to-peak phase error, respectively.

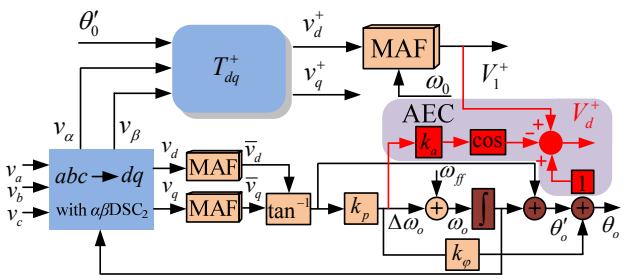

Fig. 35. Block diagram of HPLL with the proposed AEC.

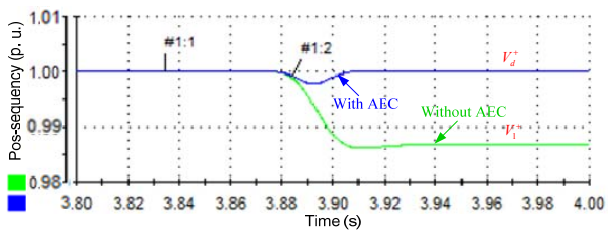

Fig. 36. Estimated positive sequence amplitude with and/or without AEC under frequency jump of +5 Hz.

compensator which actually amplifies the error signal under harmonics with the off-nominal frequency condition. The detail steady-state oscillation amplitude is shown in Table III.

VI. PERFORMANCE IMPROVEMENT OF THE HPLL USING AMPLITUDE ERROR COMPENSATION METHOD

From the above performance comparison, it can be seen that all four of the PLL have satisfactory performance under various disturbances. For the HPLL, when a frequency jump occurs, an improvement method should be made to eliminate the steady-state error in the positive sequence amplitude estimation since extraction of the positive sequence of fundamental components is critical for the grid-connected inverters in grid synchronization. Therefore, inspired by the phase-error compensation (PEC) in the HPLL, the amplitude error compensation (AEC) is proposed herein. From (12), the $\alpha\beta$DSC$_2$ output signal amplitude can be written as:

$$A = \sin(\frac{\omega + \Delta\omega_i}{4})T \tag{32}$$

Thus, the amplitude error caused by the $\alpha\beta$DSC$_2$ operator can be expressed as:

$$\Delta A = 1 - \cos(\frac{\Delta\omega_i T}{4}) \tag{33}$$

Since the average value of $\Delta\omega_o$ is equal to $\Delta\omega_i$ under the locked condition, the amplitude error at the output of the HPLL can be compensated by the online calculation of (33). A block diagram of the HPLL with AEC is shown in Fig. 35. V_d^+ indicates the positive sequence amplitude after the AEC and k_a=T/4. It should be noted that the AEC is not connected to the control loop and that the dynamics of the HPLL are unaffected.

Therefore, from Fig. 35, V_d^+ can be expressed as:

$$V_d^+ = 1 + V_1^+ - \cos(\frac{\Delta\omega_i T}{4}) \tag{34}$$

Experimental result with and without the AEC is shown in Fig. 36. This shows that the AEC effectively compensates the amplitude error and achieves zero steady-state error in about 1.5 cycles.

VII. CONCLUSION

In this paper, a detailed analysis and performance comparison of four MAF-based PLLs is presented. For the QT1-PLL, the introduction of the quasi-type-1 control structure effectively improves the dynamic response of the MAF-PLL. The lack of dc offset and even order harmonic rejection is the main disadvantages of this PLL algorithm. Apart from this, the QT1-PLL shows satisfactory steady-state and dynamic performance, and disturbance rejection capability under other grid voltage disturbance conditions.

The HPLL can be perceived as an improved version of the QT1-PLL algorithm. The application of the $\alpha\beta$DSC$_2$ block can effectively overcome the shortcomings of the QT1-PLL without jeopardizing its dynamic performance and filtering capability. However, the disturbance rejection capabilities of the HPLL and the QT1-PLL decrease with frequency deviations from their nominal values under a harmonic scenario caused by the non-frequency adaptive MAF and DSC. Then an associated drawback of the HPLL is the amplitude tracking error [see Fig. 19]. To tackle this problem, the amplitude error compensation (AEC) method is proposed in the last section. This method effectively compensates the amplitude error and ensures the accuracy of the positive sequence component extraction.

For the MPLC-PLL, cascading of the MAF and the phase-lead compensator results in a fast dynamic response of the SRF-PLL and improved disturbance rejection capability of the MAF-PLL while increasing the frequency estimation error under harmonics with the off-nominal frequency scenario. However, like the QT1-PLL the MPLC-PLL is also not suitable for grid-synchronization when the grid voltages contains dc offset and even order harmonics. Under other grid voltage disturbance scenarios, the MPLC-PLL can be a good choice.

For the DMAF-PLL, the window length of the MAF in the control loop is drastically reduced through the use of 'DP' which significantly improves the system dynamic response. The frequency adaptive *a*MAF (n=2 as shown in Section II Part A) ensures the best steady-state performance under harmonics with the off-nominal frequency scenario. However, it has the disadvantage of making the dynamic response sluggish and may even lead to system instability under some circumstances like voltage sag and flicker. Hence, it can be concluded that the DMAF-PLL can be used for grid-synchronization when the grid voltage is free from sag and flicker. The research findings of this paper may serve as a useful guideline for the grid-synchronization of three-phase grid-connected PWM inverters and distributed generators (DGs) in smart grids.

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