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DC-Link Voltage Balance Control in Three-phase Four-wire Active Power Filters

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Abstract

The three-phase four-wire shunt active power filter (APF) is an effective method to solve the harmonic problem in three-phase four-wire power systems. In addition, it has two possible topologies, a four-leg inverter and a three-leg inverter with a split-capacitor. There are some studies investigating DC-link voltage control in three-phase four-wire APFs. However, when compared to the four-leg inverter topology, maintaining the balance between the DC-link upper and lower capacitor voltages becomes a unique problem in the three-leg inverter with a split-capacitor topology, and previous studies seldom pay attention to this fact. In this paper, the influence of the balance between the two DC-link voltages on the compensation performance, and the influence of the voltage balance controller on the compensation performance, are analyzed. To achieve the balance between the two DC-link capacitor voltages, and to avoid the adverse effect the voltage balance controller has on the APF compensation performance, a new DC-link voltage balance control strategy for the three-phase four-wire split-capacitor APF is proposed. Representative simulation and experimental results are presented to verify the analysis and the proposed DC-link voltage balance control strategy.

Key words: Active power filter, DC-link voltage balance, Voltage control strategy, Compensation performance

I. INTRODUCTION

In the past decades, with the rapid development of power electronics technology, power electronic devices have become wildly installed. Therefore, a large amount of harmonic current has been injected into the grid, which deteriorated the power quality and caused serious harm to power systems [1]. As a result, harmonic control has become a hot issue that has been widely studied [2]. Active power filters (APFs) are able to detect and compensate system harmonics and reactive power in real-time, which reduces the harmonic effect on the grid and ensures operation [3]. Among them, the three-phase four-wire shunt APF is an effective device for solving the harmonic problem in three-phase four-wire power systems, especially in commercial buildings and manufacturing plants [4].

In order to make an APF work properly, the DC-link voltage must be maintained at a sufficiently high value and it must be kept stable, which ensures that the APF can produce a compensating current that strictly follows the control requirements and achieves the desired compensation effect [5], [6]. Therefore, APF DC-link voltage control is important, which needs a detailed analysis and design. Fortunately, some published studies have investigated the DC-link voltage control in three-phase four-wire APFs [7]-[20]. However, these existing studies mainly focus on minimum DC-link voltage designs [7]-[10], DC-link voltage control strategies [11]-[13], adaptive DC-link voltage references values [14]-[16], the control algorithms applied to the DC-link voltage controller [17]-[20], and the DC-link voltage control along with the improvements of the current control strategy [21], [22]. The balance between the DC-link upper and lower capacitor voltages, which is a unique problem in three-phase four-wire split-capacitor APFs, had still not been studies or analyzed. Moreover, a discussion of the influence of the DC-link voltage balance and voltage balance controller on the compensation performance of a three-phase four-wire split-capacitor APF, is still absent. Due to the limitations among the exiting studies, this paper investigates the influence of the balance of the two DC-link capacitor voltages on the APF compensation performance, and the influence of the voltage balance controller on the APF compensation performance.

In addition, with the help of a harmonic detection algorithm

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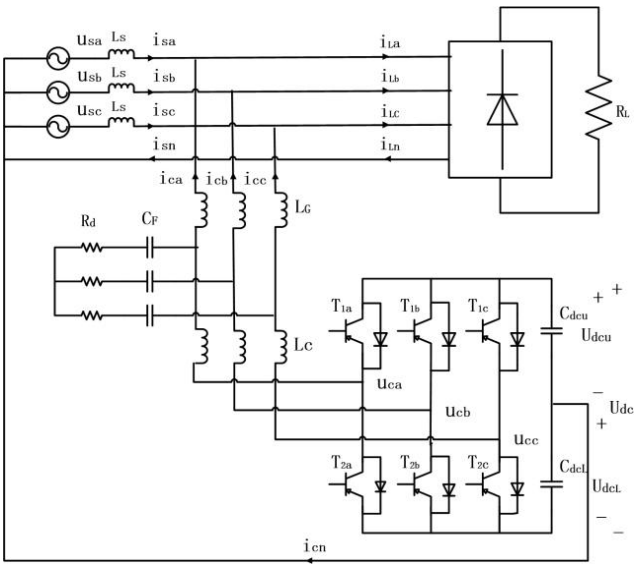


Fig. 1. The circuit of three-phase four-wire split-capacitor APF.

based on the instantaneous reactive power theory, the DC-link voltage can be effectively controlled by feedback of the DC-link voltage regulated signals as current components in the harmonic detection algorithm [10]-[20]. However, the previous studies seldom paid attention to the DC-link voltages balance control strategy in three-phase four-wire split-capacitor APFs. Only a few studies investigated an APF control algorithm together with a DC-link voltage balance control, where its DC-link voltages balance regulated signal is added to the 0 axis reference current in the dq0 coordinate [14], [18]. However, this strategy increases the complexity of the current computations, and reduces the stability and real-time characteristics in the current control. In addition, the added regulated signal may affect the compensation current control, deteriorating the compensation performance. In order to achieve a balance of the two DC-link capacitor voltages and to avoid the adverse effects from the voltage balance controller on the compensation performance, a new DC-link voltage balance control strategy for three-phase four-wire split-capacitor APFs is proposed.

The rest of this paper is organized as follows. In Section II, a three-phase four-wire split-capacitor shunt APF is illustrated. According to an analysis and mathematical deduction, the influence of the balance of two DC-link capacitor voltages and the influence of the voltage balance control on APF performance are both presented. In Section III, a DC-link voltage control balance strategy for three-phase four-wire split-capacitor APFs is described. Then, simulation and experimental verifications of the analysis and the proposed DC-link voltage balance control strategy are presented in Section IV and Section V. Finally, some conclusions are given in Section VI.

II. Analysis of the DC-Link Voltage in Three-Phase Four-Wire Split-Capacitor SAPFs

The circuit of a three-phase four-wire split-capacitor shunt APF is shown in Fig. 1. u_{SX} is the grid voltage, and u_{CX} is the inverter voltage. i_{SX} , i_{LX} and i_{CX} are the grid currents, load currents and compensating currents, respectively, where the subscript 'x' denotes phases a, b, c and n. C_{dcU} and C_{dcL} are the upper and lower DC-link capacitors. U_{dcU} and U_{dcL} are the upper and lower DC-link capacitor voltages, respectively. L_S is the grid inductor that is normally neglected due to its relatively low value. The non-linear load is composed of a three-phase rectifier and a resistance R_L, which acts as a harmonic producing load. A LCL filter composed of L_C, L_G, and C_F is used to filter out the harmonics at the switching frequency. R_d is used to suppress the resonance peak of the LCL filter at the resonance frequency and to maintain the stability of the system.

A. The Influence of the Balance of the DC-Link Voltages on the APF Compensation Performance

According to Fig. 1 and Kirchhoff's voltage law (KVL), the following equations can be obtained using the state space average method:

$$\begin{cases} L\dfrac{di_{Ca}}{dt} = U_{Ca} - U_{Sa} \\ L\dfrac{di_{Cb}}{dt} = U_{Cb} - U_{Sb} \\ L\dfrac{di_{Cc}}{dt} = U_{Cc} - U_{Sc} \\ C\dfrac{dU_{dc1}}{dt} = S_a i_{Ca} + S_b i_{Cb} + S_c i_{Cc} \\ C\dfrac{dU_{dc2}}{dt} = (S_a - 1) i_{Ca} + (S_b - 1) i_{Cb} + (S_c - 1) i_{Cc} \end{cases} \quad (1)$$

where S_a, S_b, and S_c are the switch functions for the three-phase bridge arms. When the upper switch is on and the lower switch is off, S_x=1, whereas S_x=0 when the lower switch is on and the upper switch is off, and 'x' denotes phases a, b, and c.

For a detailed analysis, the following equation can be obtained according to (1):

$$L\frac{di_{Cx}}{dt} = U_{Cx} - U_{Sa} = S_x U_{dcU} + (S_x - 1) U_{dcL} - U_{Sx} \quad (2)$$

where the subscript 'x' denotes phases a, b, and c.

When the DC-link upper and lower voltages are precisely controlled and the upper capacitor voltage are exactly equal to the lower capacitor voltage, $U_{dcU} = U_{dcL} = 0.5U_{dc}$, and (2) becomes:

$$L\frac{di_{Cx}}{dt} = \frac{(2S_x - 1)U_{dc}}{2} - U_{Sx} \quad (3)$$

On the other hand, when the upper and lower DC-link capacitor voltages are not equal, $U_{dcU} \neq U_{dcL}$, assuming that:

$$\begin{cases} U_{dcU} = U_{dc}/2 + \Delta u \\ U_{dcL} = U_{dc}/2 - \Delta u \end{cases} \quad (4)$$

where Δu is difference between the DC-link upper and lower capacitor voltages.

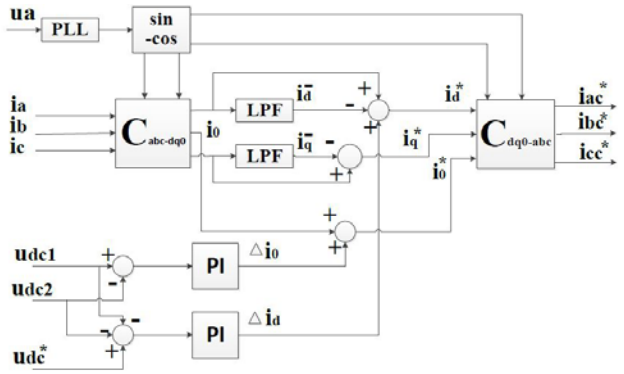


Fig. 2. Harmonic detect module with DC-link voltage control.

Substituting (4) into (2), the equation becomes:

$$\begin{aligned} L\frac{di_{Cx}}{dt} &= S_x(\frac{U_{dc}}{2}+\Delta u)+(S_x-1)(\frac{U_{dc}}{2}-\Delta u)-U_{Sx} \\ &= \frac{U_{dc}S_x}{2}+S_x\Delta u+\frac{U_{dc}S_x}{2}-S_x\Delta u-\frac{U_{dc}}{2}+\Delta u-U_{Sx} \\ &= (S_x-\frac{1}{2})U_{dc}-U_{Sx}+\Delta u \end{aligned} \tag{5}$$

By carrying out an integral operation in a switching periodic Ts, (5) turns to:

$$i_{Cx}=\frac{1}{L}\int_t^{t+Ts}[(S_x-\frac{1}{2})U_{dc}-U_{Sx}+\Delta u]dt \tag{6}$$

As can be seen from (6), the voltage difference Δu becomes a disturbance term, which may affect the control accuracy of the compensation currents, and then affect the APF compensation performance. In addition, it brings risk and potential harm to the capacitors and control system in unbalance DC-link voltages situations.

B. The Influence of the DC-Link Voltage Balance Control on the APF Compensation Performance

In order to eliminate the DC-link voltage difference, the effects on the compensation reference current and compensation performance caused by the voltage difference Δu must be restrained and the upper and lower DC-link voltages must be controlled at $U_{dcU} = U_{dcL} = 0.5U_{dc}$. Generally, the APF DC-link voltage can be stabilized by installing a DC voltage source or by increasing the DC-link capacitor. However, these methods increase the system cost and power loss, and they are not of engineering significance.

Therefore, with the help of a harmonic detection algorithm based on the instantaneous reactive power theory, the DC-link voltage can be effectively controlled by voltage control loops, feeding back the DC-link voltage regulated signals as current components in the harmonic detection algorithm. The conventional harmonic detect module with the DC-link voltage control is shown in Fig. 2, where $T_{abc\text{-}dq0}$ is the transformation matrix from abc coordinates to dq0 coordinates, and $T_{dq0\text{-}abc}$ is the transformation matrix from dq0 coordinates to abc coordinates. U_{dc} is the actual DC-link voltage, and U_{dc}* is the reference DC-link voltage. U_{dcU} and U_{dcL} are the upper and lower DC-link capacitor voltages, respectively. Δi_d is the total DC-link voltage regulated signal, and Δi_0 is the upper and lower DC-link voltage balance regulated signal. i_{La}, i_{Lb}, i_{Lc} are load currents, while i_{ca}*, i_{cb}*, i_{cc}* and i_{cd}*, i_{cq}*, i_{c0}* are the reference compensation currents in abc coordinates and dq0 coordinates, respectively.

The difference between the actual DC-link voltage and the reference value is regulated by the voltage controller, and the signal after regulation is added to the active component referent current in the dq0 coordinates. Moreover, the difference between the upper and lower DC-link voltage is also regulated by the voltage balance controller, and the signal after regulation is added into the 0 axis referent current in the dq0 coordinates. Through this DC-link voltage control strategy, the DC-link voltage will be maintained at the reference value U_{dc}, and the upper and lower DC-link voltages can be stable at $U_{dcU} = U_{dcL} = 0.5U_{dc}$.

According to the harmonic detection algorithm with the DC-link voltage control in Fig. 2, the DC-link voltage control signals Δi_d and Δi_0 are added to the reference currents in the dq0 coordinates, and affect the final reference currents $i_{c\text{-}final}$* in the dq0 coordinates i_{cd}*, i_{cq}*, i_{c0}*. Therefore, the final reference currents in the dq0 coordinates can be written as:

$$\begin{aligned} i^*_{c-final} &= i^*_c+\Delta i_d+\Delta i_0 \\ \begin{bmatrix} i^*_{cd} \\ i^*_{cq} \\ i^*_{c0} \end{bmatrix} &= \begin{bmatrix} \sum_{n=1}^{\infty} I_{cdn}\cos n\omega t \\ \sum_{n=1}^{\infty} I_{cqn}\cos n\omega t \\ \sum_{n=1}^{\infty} I_{c0n}\cos n\omega t \end{bmatrix} + \begin{bmatrix} -\sum_{n=1}^{\infty}\Delta I_d\cos n\omega t \\ 0 \\ \sum_{n=1}^{\infty}\Delta I_0\cos n\omega t \end{bmatrix} \\ &= \begin{bmatrix} \sum_{n=1}^{\infty}[I_{cdn}-\Delta I_d]\cos n\omega t \\ \sum_{n=1}^{\infty} I_{cqn}\cos n\omega t \\ \sum_{n=1}^{\infty}[I_{c0n}-\Delta I_0]\cos n\omega t \end{bmatrix} \end{aligned} \tag{7}$$

According to (7), the final reference currents i_{ca}*, i_{cb}*, i_{cc}* in the abc coordinates can be obtained by:

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = T_{dq0-abc}\begin{bmatrix} i^*_{cd} \\ i^*_{cq} \\ i^*_{c0} \end{bmatrix} \tag{8}$$

Substituting (7) into (8), the final reference currents in the abc coordinates can be written as:

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = T_{dq0-abc}\begin{bmatrix} \sum_{n=1}^{\infty} I_{cdn}\cos n\omega t \\ \sum_{n=1}^{\infty} I_{cqn}\cos n\omega t \\ \sum_{n=1}^{\infty} I_{c0n}\cos n\omega t \end{bmatrix} + T_{dq0-abc}\begin{bmatrix} -\sum_{n=1}^{\infty}\Delta I_d\cos n\omega t \\ 0 \\ \sum_{n=1}^{\infty}\Delta I_0\cos n\omega t \end{bmatrix} \tag{9}$$

Considering (9), both the total DC-link voltage regulated signal Δi_d and the DC-link voltage balance control signal Δi_0 affect the final reference currents. Since the influence of the total DC-link voltage regulated signal Δi_d on the final reference currents had already been discussed in [18], this section focuses on the influence from the DC-link voltage balance control signal Δi_0. Therefore, according to (9), the DC-link voltage balance control signal Δi_0 increases the complexity of the 0 axis current computations in the dq0 coordinates, reducing the stability and real time characteristics of the current control. In addition, assuming that the harmonic detection module can detect harmonic currents accurately, means that the first part of the final reference currents are exactly the harmonic currents that need to be compensated. However, the DC-link voltage balance control signal Δi_0 added to the 0 axis makes the reference compensation currents deviate from the actual harmonic currents.

In addition, the upper and lower DC-link voltage balance control signal in (9) can be written as:

$$\begin{aligned}\begin{bmatrix}\Delta i_{0a}\\ \Delta i_{0b}\\ \Delta i_{0c}\end{bmatrix} &= T_{dq0-abc}\begin{bmatrix}0\\ 0\\ \sum_{n=1}^{\infty}\Delta I_0\cos n\omega t\end{bmatrix}\\ &= \begin{bmatrix}\cos\omega t & -\sin\omega t & 1\\ \cos(\omega t-\frac{2\pi}{3}) & -\sin(\omega t-\frac{2\pi}{3}) & 1\\ \cos(\omega t+\frac{2\pi}{3}) & -\sin(\omega t+\frac{2\pi}{3}) & 1\end{bmatrix}\begin{bmatrix}0\\ 0\\ \sum_{n=1}^{\infty}\Delta I_0\cos n\omega t\end{bmatrix}\\ &= \begin{bmatrix}\sum_{n=1}^{\infty}\Delta I_0\cos n\omega t\\ \sum_{n=1}^{\infty}\Delta I_0\cos n\omega t\\ \sum_{n=1}^{\infty}\Delta I_0\cos n\omega t\end{bmatrix}\end{aligned} \quad (10)$$

According to (10), the nth component in the DC-link voltage balance control signal ΔI_0 in the dq0 coordinates will increase the nth component value in the abc coordinates. This scenario is observed in all of the a, b, c phases. It can be concluded from (7) and (10) that, the feedback DC-link balance control signal changes the final reference currents value and decreases the accuracy of them in both the dq0 and abc coordinates.

In addition, since the P controller is preferred and selected in the APF DC-link voltage controller due to the fact that no overshot exits in the DC-link voltage rise process for protecting system in addition to its simplicity and memory resource saving for the digital signal processor [16], [18]. The DC-link voltage control signal value ΔI_d, which is added to the active component referent current, can be written as:

$$\Delta I_0 = K_P \Delta U_{dc} = K_P (U_{dcU} - U_{dcL}) \quad (11)$$

Considering (11), with the same voltage difference ΔU_{dc}, ΔI_0 increases as the controller parameter K_p increase, and vice versa. It is well know that APF output compensation currents are controlled strictly to follow the final reference currents. A larger K_p makes the final reference currents deviate further from the actual harmonic currents value. Consequently, the APF output compensation currents following the final reference currents further deviate from the actual harmonic currents that need to be compensated. In this case, the APF steady-state compensation performance will be further deteriorated.

III. The Proposed DC-link Voltage Balance Control Strategy

According to the analysis above, the voltage difference between the upper and lower DC-link voltages may affect the control accuracy of the compensation currents and bring potential risk to the capacitors and control system. Nevertheless, the conventional solution, in which the difference between the upper and lower DC-link voltages is also regulated by a voltage controller, and the signal after regulation is added to the 0 axis referent current in the dq0 coordinates, may change the value and decrease the accuracy of the final reference currents. Furthermore, with an increase of the parameter value in the voltage controller, a larger deterioration in the final reference currents and the APF compensation performance occurs.

In order to solve this dilemma, a new DC-link voltage balance control strategy for three-phase four-wire split-capacitor APFs is proposed, as shown in Fig. 3. In the proposed control strategy, the upper and lower DC-link voltages are compared with the half reference DC-link voltage $0.5U_{dc}$. Then, the differences is regulated by the voltage controllers, and the regulated signals are both added into the active component reference current in the dq0 coordinates. Thus, the reference currents contain fundamental active current components, which ensure the energy exchange between the DC-link and AC-link of the APF and maintains the DC-link voltage at the reference level. In addition, the upper and lower DC-link voltages are both controlled at the half reference DC-link voltage, $U_{dcU} = U_{dcL} = 0.5U_{dc}$. In this way, the total DC-link voltage is stable at U_{dc}, and the DC-link voltage balance control loop, which is needed in the conventional control strategy, is not required and can be removed. This avoids the adverse effect from the voltage balance controller to the final reference currents and the compensation performance.

In addition, as discussed in Section II, the P controller is preferred and selected in the DC-link voltage controller. Furthermore, according to the DC-link voltage control signal value ΔI_d described in (11), the upper and lower DC-link voltage control signal values ΔI_{dU} and ΔI_{dL} in the proposed strategy can be written as:

$$\begin{cases}\Delta I_{dU} = K_P \Delta U_{dcU} = K_P (U_{dc}^*/2 - U_{dcU})\\ \Delta I_{dL} = K_P \Delta U_{dcL} = K_P (U_{dc}^*/2 - U_{dcL})\end{cases} \quad (12)$$

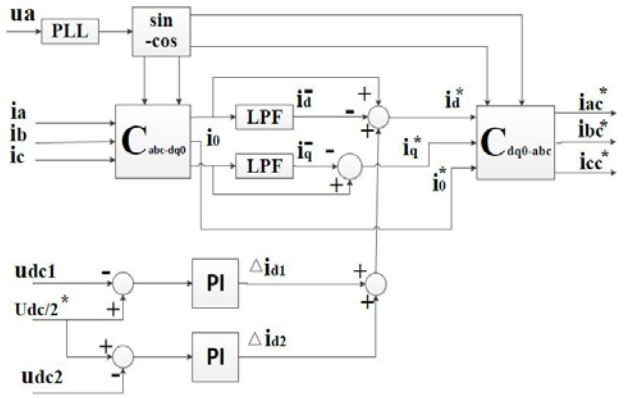


Fig. 3. The proposed DC-link voltage balance control strategy.

TABLE I
SYSTEM PARAMETERS

Grid Voltage	U_{sn}	220V
Grid Frequency	f	50Hz
Switching Frequency	f_S	9.6kHz
Inductor Filter	L	0.45mH
Equivalent Resistance	R	0.2ohm
DC-link Capacitance	C_{dcU} C_{dcL}	10000uF
Load Resistance	R_L	15ohm
DC-link Voltage	U_{dc}^*	740V

According to Fig. 3, the DC-link voltage control signal added into the active component reference current in the proposed strategy is:

$$\Delta I_d = \Delta I_{dU} + \Delta I_{dL} \tag{13}$$

Substituting (12) into (13), the DC-link voltage control signal in the proposed strategy changes to:

$$\begin{aligned}\Delta I_d &= K_P(U_{dc}^*/2 - U_{dcU}) + K_P(U_{dc}^*/2 - U_{dcL}) \\ &= K_P\left[(U_{dc}^*/2 + U_{dc}^*/2) - (U_{dcU} + U_{dcL})\right] \\ &= K_P(U_{dc}^* - U_{dc})\end{aligned} \tag{14}$$

Comparing (11) with (14), the DC-link voltage control signal value in the proposed strategy is equal to the value in the conventional strategy. In other words, the proposed strategy does not add an extra burden to the DC-link voltage regulated component. Meanwhile, compared to the conventional DC-link voltage balance control strategy, the voltage balance regulation signals added to the reference compensation currents in both the dq0 coordinates and the abc coordinates can be avoided in the proposed control strategy, preventing the effect from the voltage balance control signal on the final reference current values. In this way, on the premise of ensuring stable control of the DC-link voltage and balance between the upper and lower DC-link voltages, the deterioration of the compensation currents caused by the voltage balance control signal is diminished.

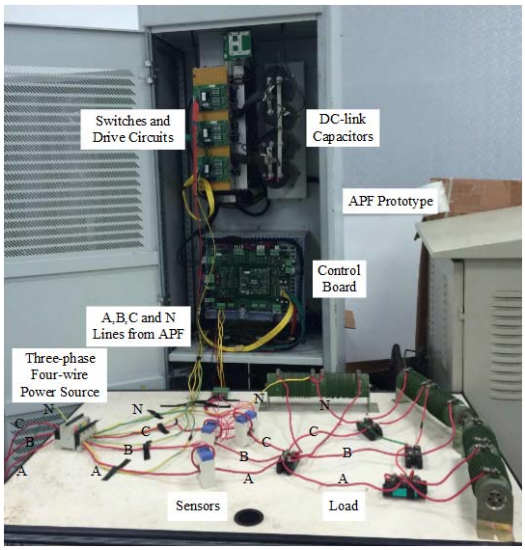
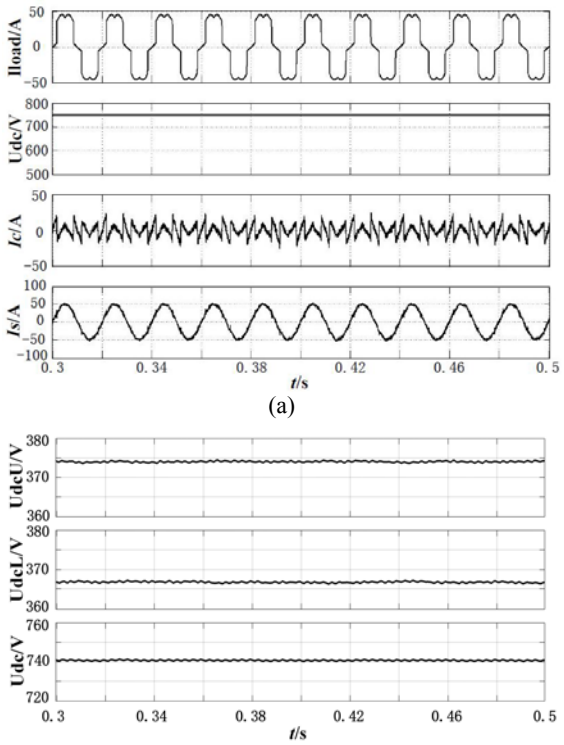


Fig. 4. The three-phase four-wire center-split shunt APF prototype and the experiment setup.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION OF THE ANALYSIS OF THE DC-LINK VOLTAGE BALANCE

In order to verify the analysis and the proposed strategy of the DC-link voltage balance, simulations and experiments in three-phase four-wire shunt APFs are carried out. The simulation studies are carried out in MATLAB. In order to verify the simulation results, a three phase four-wire center-split shunt APF prototype is also implemented in laboratory, as presented in Fig. 4. A load is connected to the three-phase four-wire power source. The load is composed of a three-phase rectifier and a resistance. Then it connects to a single-phase rectifier and a resistance in each phase, respectively, which acts as an unbalance load when the later resistances have unequal values. The APF accesses into the system in parallel, and the neutral lines of the power source, the APF and the load are connected together. The simulation and experimental system parameters are listed in Table I. In addition, a P controller is applied in the DC-link voltage control, and a PI-Repetitive compound control algorithm is applied to the compensation current control [23]. In this section, the discussion on the influence of the DC-link voltage balance control on the APF compensation performance is verified.

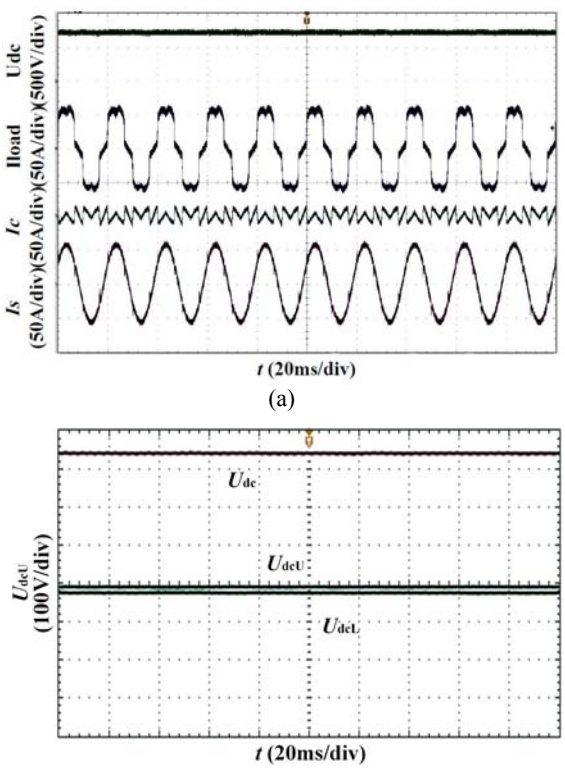
When the APF control system is operated without the DC-link voltage balance control, the simulation and experimental results are presented in Fig. 5 and Fig. 6, respectively. As can be seen from these figures, the load currents contain a large number of harmonics and the Total Harmonic Distortion (THD) of the load current in simulations and experiments are 22.59% and 23.61%, respectively. With the help of the APF, the harmonics of the load current are greatly compensated, and the THD of the source current after compensation drops to 4.61% and 4.94% in simulation and



(a)

(b)

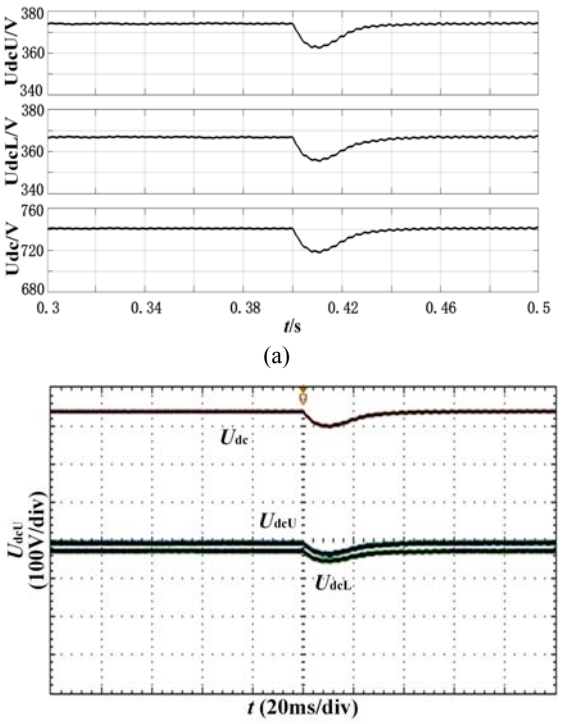
Fig. 5. Simulation results without DC-link voltage balance control. (a) Load, compensation and source currents. (b) DC-link voltages.



(a)

(b)

Fig. 6. Experiment results without DC-link voltage balance control. (a) Load, compensation and source currents, (b) DC-link voltages.



(a)

(b)

Fig. 7. Simulation and experiment results of DC-link voltage when load changes. (a) Simulation, (b) Experiment.

experiment, which satisfies international standards.

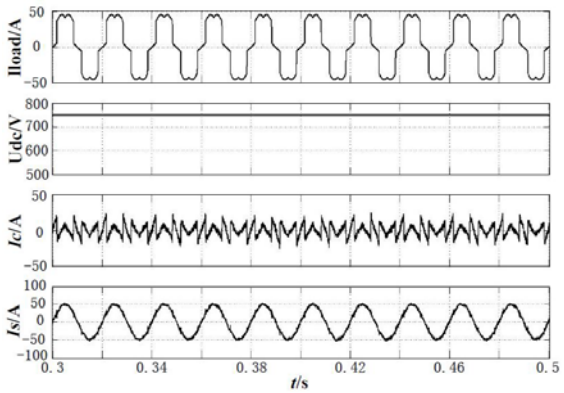
However, although the DC-link voltage is maintained at a preset 740V, the upper and lowers DC-link voltages are about 374V and 366V, respectively. Thus, they are not equal and their difference is larger than 10V with a voltage oscillation. This voltage difference brings a potential over-voltage problem to the DC-link capacitors, and a random voltage value in the upper and lower DC-link capacitor will also bring a risk and instability to both the capacitor and the control system.

Moreover, when the load varies, a large voltage fluctuation occurs, and it needs a long resume time to regain the voltage.

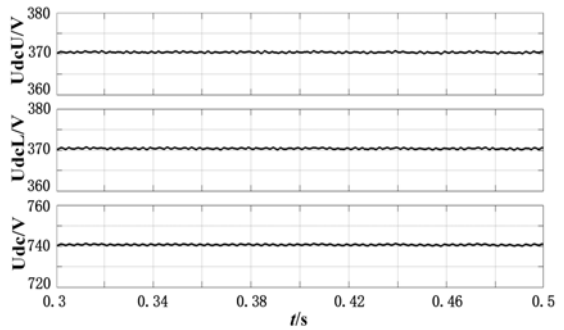
The simulation and experiment results are shown in Fig. 7, and the resume time is about 0.04s. In this situation, the APF dynamic property is deteriorated, and it brings potential harm to the capacitor and the APF itself.

Then, when the APF control system is operated with the DC-link voltage balance controller with K_p=1, the harmonics of the load current are greatly compensated, and the THD of the source currents after compensation drops to 4.41% and 4.74% in the simulation and the experiment, respectively. In addition, the upper and lower DC-link voltages are well controlled at half of the preset DC-link voltage value, $U_{dcU} = U_{dcL} = 0.5U_{dc} =$ 370V. The simulation and experiment results are presented in Fig. 8 and Fig. 9, respectively. Therefore, the voltage difference is eliminated and the affect from the voltage difference on compensation performance is diminished. Thus, the compensation performance is improved.

Moreover, when the load suddenly changes, the DC-link

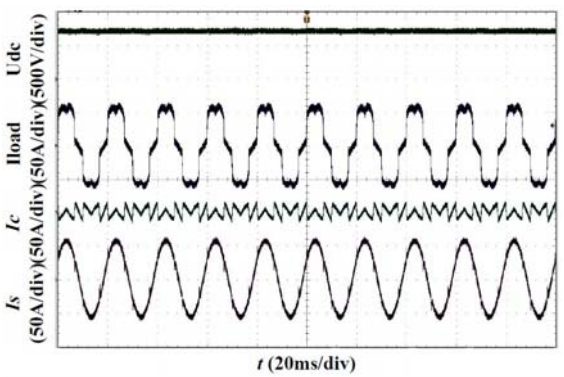


(a)



(b)

Fig. 8. Simulation results with DC-link voltage balance control. (a) Load, compensation and source currents. (b) DC-link voltages.



(a)

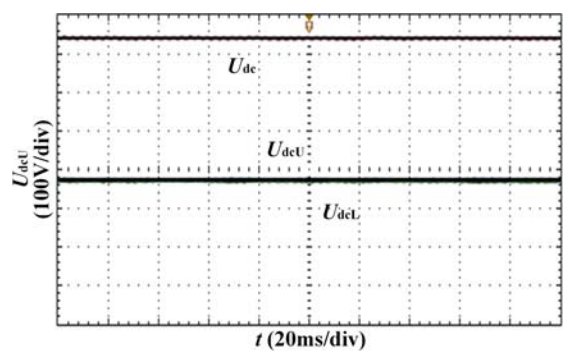


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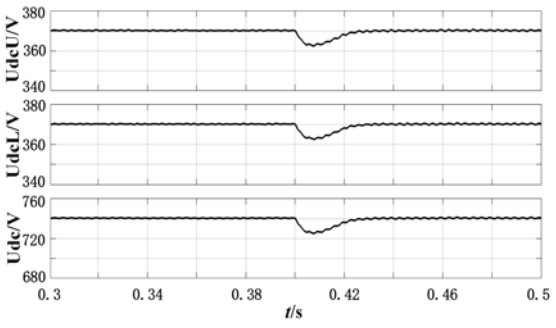
Fig. 9. Experiment results with DC-link voltage balance control. (a) Load, compensation and source currents, (b) DC-link voltages.



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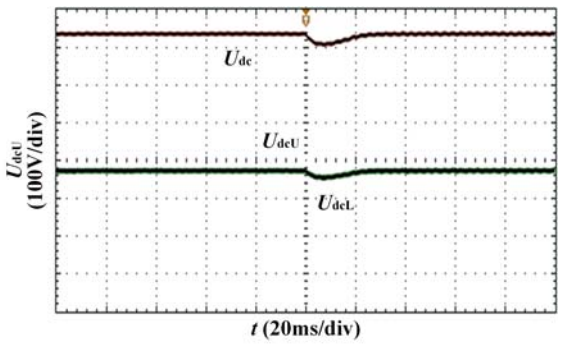

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Fig. 10. Simulation and experiment results of DC-link voltages when load changes. (a) Simulation, (b) Experiment.

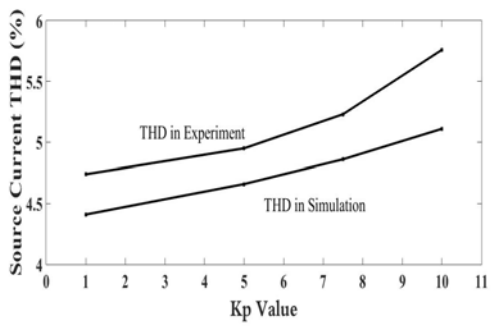


Fig. 11. Source current THD after compensation when K_p varies.

voltages rapidly resume to the setting value, and the voltage fluctuation is smaller than it is in the situation without the DC-link voltage balance control. The simulation and experiment results are shown in Fig. 10. Furthermore, when the voltage controller K_p varies from 1 to 5, 7.5 and 10, the resume time for the DC-link voltage becomes shorter and the voltage fluctuation becomes smaller with increases of K_p. Nevertheless, when K_p increases from 1 to 5, 7.5 and 10, the THD of the source current after compensation increases to 4.66%, 4.86%, 5.11% in the simulation, and 4.95%, 5.23%, 5.76% in the experiment. A diagram of the THD variation when K_p changes is presented in Fig. 11. The results show that, although the DC-link voltage balance control maintains the upper and lower DC-link voltages at a satisfactory condition and diminishes the effect from the voltage difference on compensation performance, the DC-link voltage balance controller itself is another factor that can deteriorate the compensation

TABLE II
THE VOLTAGE BALANCE SIGNAL IN DQ0 COORDINATES WITH VARIED CONTROLLER PARAMETER

Voltage Balance Control Signal ΔI_0	Orders	*Kp* = 1	*Kp* = 5	*Kp* = 10
	6th	0.30A	0.32A	0.33A
	12th	0.03A	0.04A	0.05A
	18th	0.01A	0.02A	0.03A
	24th	0.01A	0.01A	0.01A

TABLE III
THE FINAL REFERENCE CURRENT IN ABC COORDINATES WITH VARIED VOLTAGE BALANCE CONTROLLER

Current Order	Without Δi_0	*Kp* = 1	*Kp* = 5	*Kp* = 10
5th	8.47A	8.48A	8.49A	8.51A
6th	0.03A	0.03A	0.04A	0.05A
7th	4.21A	4.22A	4.24A	4.24A
11th	3.30A	3.31A	3.31A	3.34A
12th	0.03A	0.05A	0.08A	0.09A
13th	2.29A	2.32A	2.32A	2.34A
17rd	1.98A	1.55A	1.55A	1.55A
18th	0.02A	0.05A	0.06A	0.07A
19th	1.51A	1.54A	1.55A	1.56A
23rd	1.30A	1.35A	1.36A	1.38A
24th	0.01A	0.03A	0.05A	0.06A
25th	1.05A	1.07A	1.09A	1.11A

performance, and this influence is more significant with an increase of its parameter K_p.

For a detailed analysis, the values of the voltage balance control signal in the dq0 coordinates and the final reference compensation currents added to the DC-link voltage balance control signal in the abc coordinates with different voltage balance controller parameters, are listed in Table II and Table III, respectively. From Table II, it can be seen that the values in the d-axis are mainly in $6k^{th}$ (k=1,2,3,…), and values in the other orders are almost zero. Although the addition of a value with variations of the controller is small, the values in the $6k^{th}$ in the d-axis in dq0 coordinates affect the values in the abc coordinates, raising the values in the abc coordinate, which are shown in Table III, and these values become larger with an increase of K_p. Thus, the final reference compensation current value varies after adding the DC-link voltage balance control signal ΔI_0. Then the accuracy of the final reference currents in the dq0 coordinates are affected. In this situation, the final reference current deviates from the accurate harmonic current, and the situation become more serious with an increase of K_p.

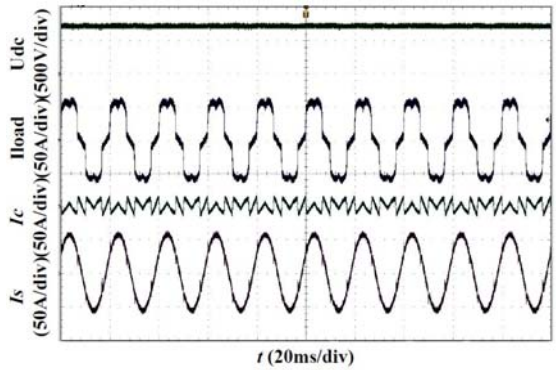
To sum up the simulation and experiment results above, without the DC-link voltage balance control, the upper and lower DC-link voltages are maintained at random voltage values, and a voltage difference between them occurs. When the DC-link voltage balance controller is applied, the upper and lower DC-link voltages are maintained at preset voltage values, which are equal to half of DC-link voltage. In addition, a larger K_p brings a better dynamic characteristic in the voltage balance control. Nevertheless, the DC-link voltage balance control signal Δi_0, which is an extra value in the final reference currents both in the dq0 coordinates and the abc coordinates, deviates the final reference compensation currents from the accurate harmonic currents, reducing the precision of the final reference value. Meanwhile, a larger K_p also leads to a larger Δi_0 by adding in the final reference compensation currents. However, the APF steady-state compensation performance may be worse with an increase of K_p.

V. SIMULATION AND EXPERIMENTAL VERIFICATION OF THE PROPOSED DC-LINK VOLTAGE BALANCE CONTROL STRATEGY

According to the analysis and experiment above, in order to realize the upper and lower DC-link voltage balance and to avoid the influence from the voltages balance controller on the APF compensation performance, a new DC-link voltage balance control strategy is proposed and applied. The experiment results are shown in Fig. 12.

Once the proposed DC-link voltage balance control strategy is applied, the upper and lower DC-link voltages become equal and their values are stable at the preset half of the DC-link voltage, $U_{dcU} = U_{dcL} = 0.5U_{dc} = 370$V. Thus, the total DC-link voltage will be maintained at 740V. In addition, the APF achieves an ideal compensation performance and the THD of the source current after compensation is 4.18% and 4.54% in the simulation and experiment, which is better than the performance with the conventional DC-link voltage balance control. Furthermore, when the load suddenly changes, the upper and lower DC-link voltages achieve an ideal dynamic characteristic, which is similar to the performance with the DC-link voltage balance control. In addition, the final reference compensation current values in the proposed strategy are equal to the values in the situation without the DC-link voltage balance control, and their values are listed in Table IV. Thus, the proposed DC-link voltage balance control strategy not only maintains the upper and lower DC-link voltage balanced, ensuring the dynamic and steady-state characteristic of the DC-link voltage, but it also eliminates the extra component added to the final reference compensation currents, avoiding the adverse effects from the DC-link voltage balance control on the final reference compensation currents. In this way, the balance of the upper and lower DC-link voltages can be obtained and precise control of the compensation current and ideal performance can be achieved.

In addition, when the system is connected to an unbalanced load, the experiment results are shown in Fig. 13. It can be seen from these figures that the source currents in the a, b, c phases



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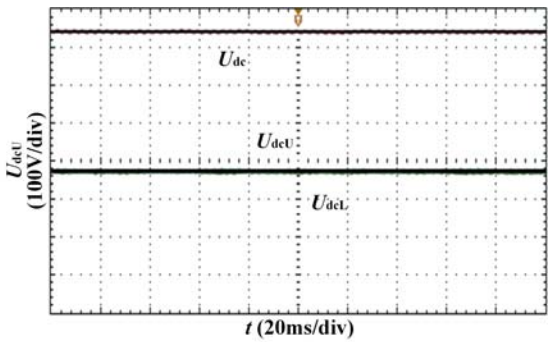

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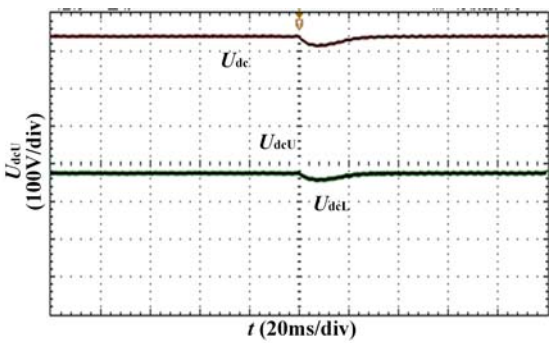
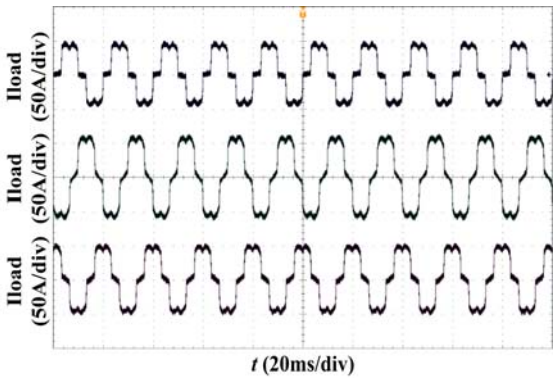


(c)

Fig. 12. Experiment results when the proposed voltage control strategy is applied. (a) Load, compensation and source currents. (b) DC-link voltage in steady-state. (c) DC-link voltage when load changes.

TABLE IV
THE FINAL REFERENCE CURRENT IN ABC COORDINATES IN CONVENTIONAL AND PROPOSED STRATEGIES

Orders	Strategy without Δi_0	Proposed Strategy
5th	8.47A	8.47A
7th	4.21A	4.21A
11th	3.30A	3.30A
13th	2.29A	2.29A
17th	1.98A	1.98A
19th	1.51A	1.51A
23th	1.30A	1.30A
25th	1.05A	1.05A



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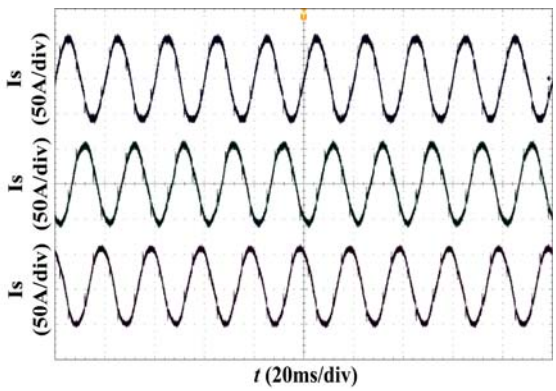
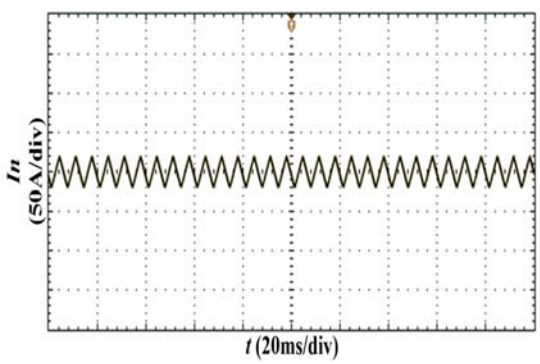
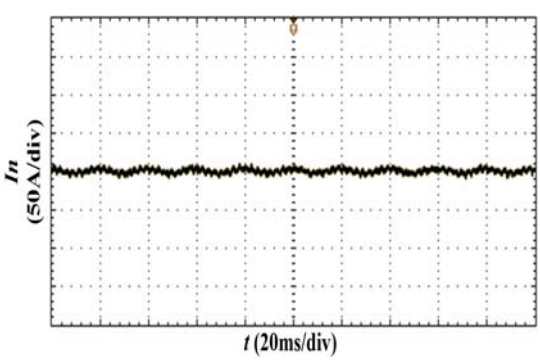


(b)

Fig. 13. Experiment results of three-phase source currents in unbalance load situation. (a) Before compensation. (b) After compensation.



(a)



(b)

Fig. 14. Experiment results of neutral line current in unbalance load situation. (a) Before compensation. (b) After compensation.

before compensation are 34.7A, 44.6A, 36.8A, respectively. With the help of an APF with the proposed strategy, the load harmonics are greatly compensated, and the source currents in a, b, c phases become almost sinusoidal. Furthermore, the source currents are 44.1A, 45.8A, 44.8A in the a, b, c phases, respectively. Therefore, it can be seen that the three-phase unbalanced phenomenon is well eliminated.

In addition, the neutral line current is large due to the unbalanced load, as shown in Fig. 14 (a), and its value is 11.2A. After compensation by an APF, the neutral current drops to about 1.8A, as shown in Fig. 14 (b). Thus, the neutral current is well compensated, reducing the influence of the neutral current effect on the system.

VI. CONCLUSION

The balance of the DC-link upper and lower capacitor voltages, which is a unique problem in three-leg inverters with the split-capacitor topology of three-phase four-wire APFs, has still not been concerned and discussed. In this paper, the influence of the balance of two DC-link voltages on the compensation performance and the influence of the voltage balance controller on the compensation performance are analyzed. To achieve the balance of two DC-link capacitor voltages and to avoid adverse effects from the voltage balance controller on the APF compensation performance, a new DC-link voltage balance control strategy for three-phase four-wire split-capacitor APFs is proposed. Representative simulation and experimental results are presented to verify the analysis and the proposed DC-link voltage control strategy. Therefore, the proposed nonlinear DC-link voltage balance control strategy has been shown to be an optimal solution in practical situations.

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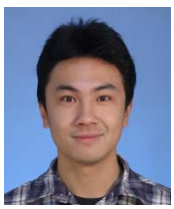

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