JPE 16-5-33

http://dx.doi.org/10.6113/JPE.2016.16.5.1950
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

IGBT Open-Circuit Fault Diagnosis for 3-Phase 4-Wire 3-Level Active Power Filters based on Voltage Error Correlation

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Abstract

A novel open-circuit fault diagnosis method for 3-phase 4-wire 3-level active power filters based on voltage error correlation is proposed in this paper. This method is based on observing the output pole voltage error of the active power filter through two kinds of algorithms. One algorithm is a voltage error analytical algorithm, which derives four output voltage error analytic expressions through the pulse state, current value and dc bus voltage, respectively, assuming that all of the IGBTs of a certain phase come to an OC fault. The other algorithm is a current circuit equation algorithm, which calculates the real-time output voltage error through basic circuit theory. A correlation is introduced to measure the similarity of the output voltage errors between the two algorithms, and OC faults are located by the maximum of the correlations. A FPGA has been chosen to implement the proposed method due to its fast prototyping. Simulation and experimental results are presented to show the performance of the proposed OC fault diagnosis method.

Keywords: Active Power Filter, Correlation, Fault Diagnosis, IGBT OC Fault, NPC 3-Level

I. INTRODUCTION

The active power filter (APF) has been widely used for harmonic compensation in industrial areas. The principle of active filtering was established decades ago in [1]. The APF can be treated as a special controlled converter, which shares the same topologies as the H bridge, 2-level, NPC 3-level, etc. Since IGBTs and other semiconductors play a crucial role in these converters, their failures can greatly interrupt or even damage a system, which can result in security problems and economic losses.

According to [2], nearly 40% of the failures in power devices are semiconductor and soldering failures. Therefore, reliability is always a focus in [3]. For the IGBT itself, short-circuit (SC) and open-circuit (OC) faults are the two most common faults, where SC faults are usually destructive and result in a direct shut down of the system. Advanced IGBT drivers are usually designed with SC protection, where a system controller can detect the protection signal and turn off all of the pulses within several μs. When compared to SC faults, OC faults have a higher rate and are more likely to go undetected.

During the past 4 decades, multilevel converters have been under research and development in terms of successful industrial applications, as mentioned in [4], [5]. Multilevel converters increase the number of the output voltage values, leading to low harmonics of the output voltage. A comparison of the common topologies for 3-level converters versus 2-level converters is discussed in [6], which shows the great advantages of multilevel converters. For APFs, the multilevel topology is also widely used to increase the capacity and to obtain a better compensation performance. However, multilevel topology result in an increased number of IGBTs, which increases the probability of IGBT failure.

Research has been carried out on both the OC fault diagnosis and fault tolerance of power converters. For OC fault diagnosis, this research is mainly focused on converters [7]-[11], motor drive systems [12]-[17] and DC/DC converters [18], when compared to the much more reduced work on active power filters. In addition, many methods have been proposed for 2-level converters [13]-[17]. However there have only been

Manuscript received Feb. 16, 2016; accepted May 25, 2016
Recommended for publication by Associate Editor Kyo-Beum Lee.
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a few for 3-level converters [7]-[12].

Current-based and voltage-based methods are common OC fault diagnosis strategies. In terms of the current-based proposals in the literature, the current Park's Vector method has been proposed as a fault diagnostic tool for 2-level converters [19], [20]. However, it requires very complex pattern recognition algorithms, which are not suitable for integration into drive controllers. Despite this fact, many fault diagnostic methods are based on this first strategy. The average current Park's Vector method was introduced in [21]. Further works based on the analysis of the current space vector trajectory diameter were proposed in [22], [23]. The major drawbacks of these proposals are their load dependence and sensitivity to transients, which result in unsatisfactory performance for low load conditions and false alarms during transients. To overcome these weaknesses and to enhance the robustness, a normalized average currents method was proposed in [24] and the absolute values of the normalized average currents are considered in [25]. A combined method based on both the derivative of the current Park's vector phase and the current polarity was proposed in [26]. It possesses an excellent immunity to false alarms.

On the other hand, voltage-based methods have a faster response than current-based methods [27], [28]. However, they usually need additional detection hardware, which increases the drive costs and complexity. A direct comparison between the measured voltages and the reference values was proposed in [29] and a time delay was introduced to prevent false alarms. A FPGA based fault location approach was introduced in [30], with detection times shorter than 10 μs. Alternatively, a low-cost proposal based on indirect voltage measurement was obtained using high-speed photocouplers in [31]. However, well-defined time delays dependent on the nature of the power converter are still required.

In summary, current-based methods are independent of system parameters and no additional sensors are needed. Voltage-based methods rely on extra hardware, but they possess a fast detection time. Furthermore, some well-defined time-delay values must be correctly defined to avoid false alarms.

In addition, some other methods, such as wave-let fuzzy algorithm [32], wavelet-neural network [33] and rule-based expert systems [34] can be chosen for OC fault diagnosis. For these methods, 3-phase currents, inverter pole voltage, phase voltage, switch voltages, DC link current or user input are all potential quantities which can be chosen as detection parameters. For expert systems, user input can use a combination of the above parameters.

Most of the fault diagnosis proposals in the literature are designed for rectifiers, motor drive systems or DC/DC converters. As in APF systems, the load situation becomes more complicated and changeable, and the requirements for the fault diagnosis method are increased.

Generally, APF OC fault diagnosis is more difficult than rectifiers and motor drive systems due to the following reasons:

- Sine current is the control purpose for rectifiers and motor drive systems. However, the current in APFs only follows the detected compensation current order, which is usually not sine-shaped, unless it is only the reactive power compensation case.
- Unbalanced current exists in unbalanced load conditions for APF.
- A higher switch frequency is usually required in APFs.

As a result, the previous current Park's Vector method and the average Park's Vector method could fail for APFs.

Limited work has been done on APF OC fault diagnosis and tolerance. An OC fault diagnosis method based on classical voltage measurements and combinatory logic was proposed in [35]. A similar method was given in [36], with current sensor fault consideration. [35] and [36] both proposed 2-level APFs with additional sensors.

An APF OC fault diagnosis and tolerance method based on a NPC 3-level was proposed in [37]. This method is based on a direct comparison between estimated filter line voltages and the expected voltages without additional sensors. However, the calculation precision cannot be guaranteed and no experimental results are given in [37].

In [38], an advanced strategy was proposed for APF OC fault diagnosis through an analysis of converter voltage errors and conditions under which large errors occur. The voltage error calculation precision is improved by consideration of near-zero current situations, which has an influence on the voltage error values. Additionally, the diagnostic time is reduced in some situations and no additional sensor is required. The same method was used in NPC 3-level rectifier OC fault diagnosis in [39]. Both [38] and [39] are based on the *dSpace* platform.

In [37]-[39], the voltage error was estimated by using circuit equations, where di/dt must be involved. In a discrete digital control system, di/dt is calculated by using the last period value $i(k\text{-}1)(k=1,2,3\ldots)$ and T_S, which means that a T_S time delay constantly exists. As a result, the estimated voltage will never be exactly the same as the real voltage. The error can be reduced by a higher sampling frequency, but it cannot be eliminated. This has a direct influence on the OC fault diagnosis, which was not considered in [37]-[39].

In this paper, a novel OC fault diagnosis method for 3-phase 4-wire 3-level active power filters based on voltage error correlation is proposed. For ground neutral systems, the APF should have a compensation ability for the neutral wire current and a 4-wire compensation system is needed [40]. Therefore, the OC fault diagnosis becomes more complicated. No published work has discussed 3-level 4-wire APF OC fault diagnosis.

The given method is based on [38]. However, its reliability

is greatly improved. The zero current situation is considered and no additional sensors are required. Instead of judging an OC fault solely by the amplitude of the calculated pole voltage error, which can be affected by the sampling frequency and the sampling accuracy, a more reliable algorithm is proposed. A Butterworth filter strategy is introduced to eliminate the noise of the pole voltages, obtained through the two given methods, and the correlation is compared during a supply period. A FPGA is chosen to implement the given method and the OC faults are located within 40.1ms.

The main advantages of the proposed pole voltage error correlation-based approach are as follows:

- High accuracy. Unlike previous OC fault diagnosis solutions, which depend on only one type of detection parameter, such as 3-phase currents [19], 3-phase voltages [29] or reference voltages available from the control system [27], the proposed correlation-based method takes advantage of a combination of all of the available parameters, such as currents, voltages and pulse states to calculate the output pole voltage error. Furthermore, a Butterworth second-order filter is involved to eliminate the noise of the calculated pole voltage error, solving the tuning problems and reducing the chance of false alarm, which are not considered in [38][39]. In addition, instead of judging an OC fault by only one moment's amplitude of the calculated pole voltage error as in [38][39], a whole supply period's voltage values are considered to be the diagnosis references, which greatly enhances the accuracy of the proposed method.
- Load independence. The proposed algorithm is independent of different power conditions, such as the rectifier load, inductive load or capacitive load. It has good performance under unbalanced load current situations.
- No additional sensors are required. The proposed method could be classified as a voltage-based fault diagnosis method, but without any additional voltage measurements.
- Effectiveness and reliability. The zero-current situation is considered, which allows the fault diagnosis to be achieved effectively. Thanks to the parallel architecture of the FPGA, the tasks can be implemented quickly, and the result of the fault IGBT's correlation is distinct from other healthy IGBTs, leading to clear judging of OC faults.

However, there are some drawbacks to the proposed method. The algorithm must be implemented on a very fast digital target, such as a FPGA or a CPLD, which increases the hardware costs. Although no additional sensors are demanded, ADCs with a very high frequency bandwidth are required. This algorithm needs a large amount of calculation, which increases the burden on the controller. In addition, the response time of the proposed algorithm is between 20.1ms~40.1ms, which is longer than the conventional voltage-based method.

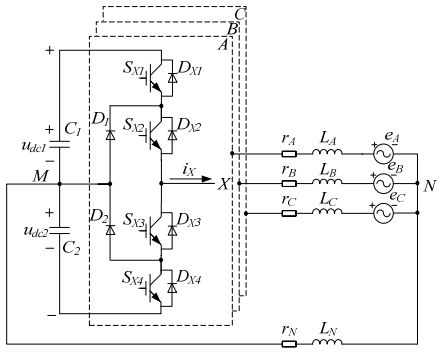


Fig. 1. Schematic of the 3-line 4-wire APF.

The given algorithm is explained in Section II. In addition, experimental results and FPGA implementation will be presented in Section III. Some conclusions are presented in Section IV.

II. Open-Circuit Fault Diagnosis Algorithm

A. System under Healthy Conditions

The 3-phase 4-wire 3-level NPC APF topology is represented in Fig.1. For each leg (*A* or *B* or *C*), there are 4 IGBTs and 6 Diodes, which are defined as S_{X1}, S_{X2}, S_{X3}, S_{X4}, D_{X1}, D_{X2}, D_{X3}, D_{X4}, D_1 and D_2. In this paper, $X \in (A, B, C)$. The output current i_X of leg X is shown in Fig. 1, with a reference direction.

V_{XM} is defined as the output pole voltage between point X and point M under healthy conditions. For the NPC 3-level topology, the pulse state $S_X=\{1,0,-1\}$ is introduced to each leg. When $S_X=1$, S_{X1} and S_{X2} turn on, and point X is connected to the dc bus "+" through S_{X1} and $S_{X2}(i_X>0)$ or D_{X1} and $D_{X2}(i_X<0)$. When $S_X=0$, S_{X2} and S_{X3} turn on, and X point is connected to point M through D_1 and $S_{X2}(i_X>0)$ or S_{X3} and $D_2(i_X<0)$. When $S_X=-1$, S_{X3} and S_{X4} turn on, and point X is connected to the dc bus "-" through D_{X4} and $D_{X3}(i_X>0)$ or S_{X3} and $S_{X4}(i_X<0)$.

The pole voltage V_{XM} in healthy conditions is given by:

$$V_{XM}=\begin{cases} u_{dc1} & S_X=1 \\ 0 & S_X=0 \\ -u_{dc2} & S_X=-1 \end{cases}, (X \in A,B,C). \quad (1)$$

B. Voltage Error Analytical Algorithm

V'_{XM} is defined as the output pole voltage between point X and point M under fault conditions. The value of V'_{XM} differs when an OC fault of S_{X1}, S_{X2}, S_{X3} or S_{X4} occurs, which will be discussed later.

When S_{X1} comes to open fault, if the pulse state $S_X=0$ or -1, $V'_{XM}=V_{XM}$. S_{X1} is kept off. If $S_X=1$ and $i_X<0$, current flows to

TABLE I
THE VALUES OF V'_{XM} AND V_{XM} IN OC FAULT CONDITIONS

$S_{X1/2/3/4}$	i_X Condition	S_X	V_{XM}	V'_{XM}
S_{X1}	$i_X>0$	1	u_{dc1}	0
S_{X2}	$i_X>0$	1	u_{dc1}	$-u_{dc2}$
	$i_X>0$	0	0	$-u_{dc2}$
S_{X3}	$i_X<0$	0	0	u_{dc1}
	$i_X<0$	-1	$-u_{dc2}$	u_{dc1}
S_{X4}	$i_X<0$	-1	$-u_{dc2}$	0

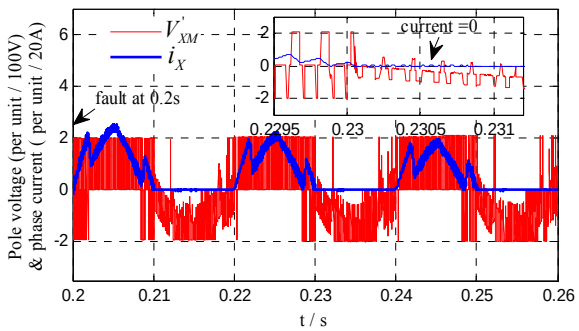


Fig. 2. The value of V'_{XM} in i_X=0 or i_X≈0 conditions.

the dc bus "+" through D_{X1} and D_{X2}, and V'_{XM} is not affected. If S_X=1 and i_X>0, point X is cut off from the dc bus "+" and finds a new current path of M->D_1->S_{X2}->X. In this case, V'_{XM}=0.

When S_{X2} comes to an OC fault, if the pulse state S_X=-1, V'_{XM}=V_{XM}. S_{X2} is kept off. If S_X=0 and i_X<0, current flows to point M through S_{X3} and D_2, and V'_{XM} is not affected. If S_X=0 and i_X>0, point X is cut off from point M, and current flows following the path of "-"->D_{X4}->D_{X3}->X. In this case, V'_{XM}=-u_{dc2}. If S_X=1 and i_X<0, current flows to point M through D_{X1} and D_{X2}, and V'_{XM}=u_{dc1}, which is equal to V_{XM} under healthy conditions. If S_X=1 and i_X>0, current flows following the path of "-"->D_{X4}->D_{X3}->X, and V'_{XM}=-u_{dc2}.

Similarly, the situations of S_{X3} and S_{X4} OC faults can be analyzed. Thus, the output pole voltage differs in terms of fault conditions, as shown in Table I.

From what has been discussed above, no matter which IGBT comes to an OC fault, the current can find a new path and point X can connect to point M, dc bus "+" or dc bus "-". However, in real situations, if the current i_X falls below the holding current, the IGBT is turned off. This means than when i_X=0 or i_X≈0 happens, as shown in Fig. 2, V'_{XM} is not simply equal to u_{dc1}, 0 or -u_{dc2}. V'_{XM} in the i_X=0 or i_X≈0 conditions will be derived later.

The equivalent circuit in the i_A=0 or i_A≈0 condition is shown in Fig. 3.

Fig. 3 can be described through the following equations:

$$V'_{AM}=i_A\cdot r_A+L_A\cdot\frac{di_A}{dt}+e_A-e_B-L_B\cdot\frac{di_B}{dt}-i_B\cdot r_B+V_{BM} \quad (2)$$

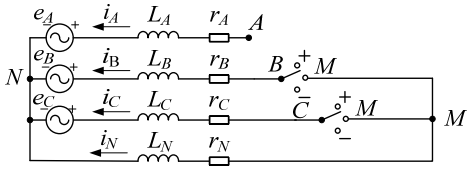


Fig. 3. The equivalent circuit in i_A=0 or i_A≈0 conditions.

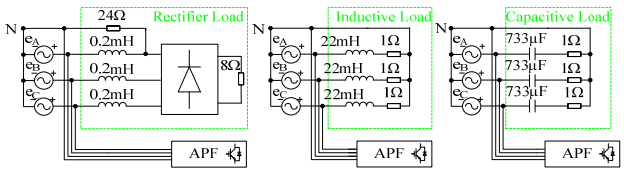


Fig.4. Various loads of simulation.

or $$V'_{AM}=i_A\cdot r_A+L_A\cdot\frac{di_A}{dt}+e_A-e_C-L_C\cdot\frac{di_C}{dt}-i_C\cdot r_C+V_{CM} \quad (3)$$

or $$V'_{AM}=i_A\cdot r_A+L_A\cdot\frac{di_A}{dt}+e_A-L_N\cdot\frac{di_N}{dt}-i_N\cdot r_N. \quad (4)$$

Approximately, r_X=r_N=0, $i_X\cdot r_X$=$i_N\cdot r_N$=0. As i_A≈0, $L_A\cdot\frac{di_A}{dt}$≈0, i_B+i_C+i_N≈0. Assuming that L_A=L_B=L_C=L_N, then $L_B\cdot\frac{di_B}{dt}$+$L_C\cdot\frac{di_C}{dt}$+$L_N\cdot\frac{di_N}{dt}$≈0. According to (2), (3) and (4), the output pole voltage V'_{AM} is given by:

$$V'_{AM}\approx e_A-\frac{2}{3}(e_B+e_C)+\frac{1}{3}(V_{BM}+V_{CM}). \quad (5)$$

Similarly:

$$V'_{BM}\approx e_B-\frac{2}{3}(e_A+e_C)+\frac{1}{3}(V_{AM}+V_{CM}), \quad (6)$$

$$V'_{CM}\approx e_C-\frac{2}{3}(e_A+e_B)+\frac{1}{3}(V_{AM}+V_{BM}). \quad (7)$$

To sum up, V^*_{XM} is defined as the real output pole voltage between point X and point M under fault conditions, which is given by:

$$V^*_{XM}=\begin{cases} V'_{XM} & |i_X|>\varepsilon \\ e_X-\frac{2}{3}\sum\limits_{\substack{i\neq X\\ i\in\{A,B,C\}}}e_i+\frac{1}{3}\sum\limits_{\substack{i\neq X,\\ i\in\{A,B,C\}}}V_{iM} & |i_X|\le\varepsilon \end{cases}. \quad (8)$$

Where ε is a small value and ε>0.

Then:

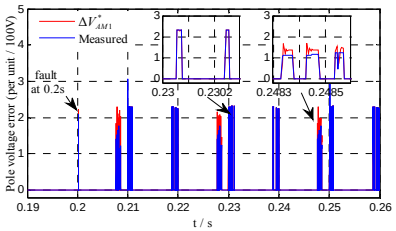
$$\Delta V^*_{XM}=V_{XM}-V^*_{XM}=\begin{cases} V_{XM}-V'_{XM} & |i_X|>\varepsilon \\ V_{XM}-e_X+\frac{2}{3}\sum\limits_{\substack{i\neq X\\ i\in\{A,B,C\}}}e_i-\frac{1}{3}\sum\limits_{\substack{i\neq X,\\ i\in\{A,B,C\}}}V_{iM} & |i_X|\le\varepsilon \end{cases}. \quad (9)$$

When an OC fault occurs, the output pole voltage differs from that under healthy conditions. The output pole voltage error ΔV^*_{XM} can be calculated by (9). This method is called voltage error analytical algorithm. Matlab/Simulink is used to verify the performance of this algorithm under different power conditions. A rectifier load, an inductive load and a capacitive load are considered as 3 typical load conditions, which are shown in Fig. 4. The simulation parameters are shown in Table II.

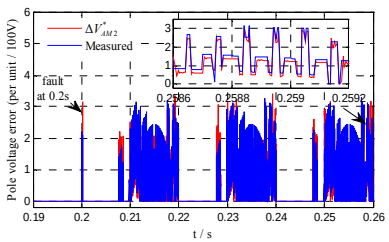
Simulation results of a S_{A1}, S_{A2} OC fault are shown in Fig. 5, Fig. 6 and Fig. 7, where Fig. 5 represents a rectifier load,

TABLE II
SIMULATION PARAMETERS

Parameter	Value
e_{AB},e_{BC},e_{CA}	190V(RMS)
L_X, L_N	1mH
u_{dc}=u_{dc1}+u_{dc2}	450V
C_1,C_2	13600μF(6800μF*2)
Switching frequency	10kHz
Sampling frequency	80kHz



(a)



(b)

Fig. 5. Comparison between measured output pole voltage error and ΔV_{XM}^{*} by voltage error analytical algorithm when S_{A1} OC fault (a) and S_{A2} OC fault (b) with rectifier load.

Fig. 6 represents an inductive load, and Fig. 7 represents a capacitive load. Comparisons between ΔV_{XM}^{*} and the actual measured output pole voltage error are illustrated in small windows for all 3 different power conditions. The calculated ΔV_{XM}^{*} and the actual voltage error match each other well, which shows the accuracy of voltage error analytical algorithm. In Fig. 5, Fig. 6 and Fig. 7, ΔV_{XMi}^{*} (i=1,2,3 or 4) stands for ΔV_{XM}^{*} in a S_{Xi} OC fault.

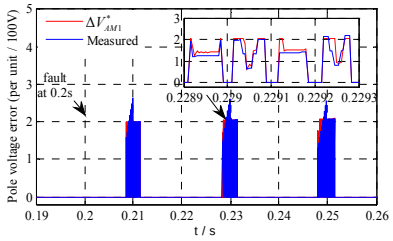
It can be seen from Fig. 5, Fig. 6 and Fig. 7 that the given voltage error analytical algorithm is not affected by the type of load, and can accurately calculate the output pole voltage error under a variety of load conditions.

The voltage error analytical algorithm is easy to implement without additional sensors, since e_X, i_X, u_{dc1} and u_{dc2} are required for APF control systems and the pulse state S_X is ready to use (e.g. in FPGA or CPLD).

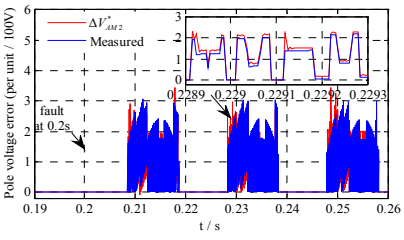
However, (9) will not come to alive until an OC fault moment arrives. That is to say (9) is incorrect under healthy conditions. Thus, ΔV_{XM}^{*}=0 is defined before an OC fault moment.

C. Current Circuit Equation Algorithm

The authors of [38] proposed a method for estimating the

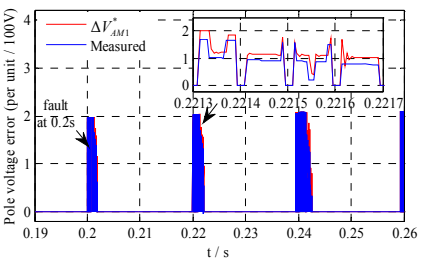


(a)

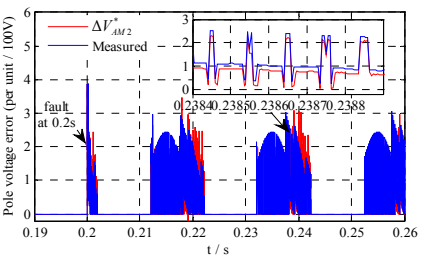


(b)

Fig. 6. Comparison between measured output pole voltage error and ΔV_{XM}^{*} by voltage error analytical algorithm when S_{A1} OC fault (a) and S_{A2} OC fault (b) with inductive load.



(a)



(b)

Fig. 7. Comparison between measured output pole voltage error and ΔV_{XM}^{*} by voltage error analytical algorithm when S_{A1} OC fault (a) and S_{A2} OC fault (b) with capacitive load.

output pole voltage by a circuit equation. To avoid common mode voltage, line-to-line voltage is used to perform an indirect analysis of the pole voltage error. As in a 3-phase 4-wire system, point M is connected to point N, no common mode voltage is involved and the output pole voltage can be derived similarly by a circuit equation.

$\Delta V_{XM}^{Circuit}$ (orΔV_{XM}^{C}) is defined as the output pole voltage between point X and point M, which is obtained by a current circuit equation algorithm. An equivalent circuit is shown in Fig. 8.

The equation is given by:

$$V_{XM}^{C}=i_X\cdot r_X+L_X\cdot\frac{di_X}{dt}+e_X-L_N\cdot\frac{di_N}{dt}-i_N\cdot r_N. \quad (10)$$

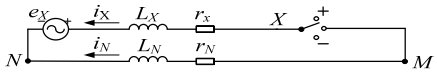


Fig. 8. Equivalent circuit of phase *X*.

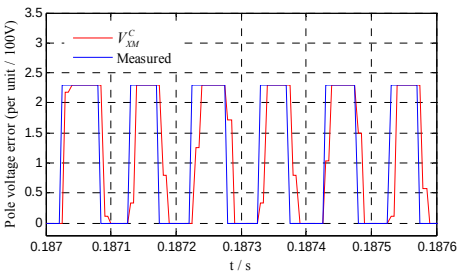


Fig. 9. Comparison between V^C_{XM} and measured output pole voltage.

In a discrete digital control system, the current rate is given by:

$$\frac{di_X}{dt}=\frac{i_X(k)-i_X(k-1)}{T_S}. \tag{11}$$

Where k=1,2,3⋯; T_S is the sampling time.

Thus, the output pole voltage is given by:

$$\Delta V^C_{XM}=V_{XM}-V^C_{XM} \tag{12}$$

As discussed previously, (9) is only correct when an OC fault occurs. By comparison, (12) is correct in both healthy and fault conditions, which is its major advantage. However, for actual discrete digital systems, the calculation accuracy of ΔV^C_{XM} is severely influenced by the sampling frequency. As in (11), $i_X(k\text{-}1)$ is used to calculate the current rate di_X/dt, where a T_S period delay exists. The calculation error cannot be eliminated even if T_S is reduced to the μs level. Fig. 9 illustrates a comparison between V^C_{XM} and the measured pole voltage error, with a sampling frequency of $f_S=1/T_S$=80kHz and a switching frequency of f_{switch}=10kHz.

Therefore, ΔV^C_{XM} by (12) contains narrow pluses near f_{switch}, which has a major influence on the OC fault location. [38] locates an OC fault according to the amplitude of V^C_{XM}. However, how the limitation of f_S affects the result of the fault location is not discussed.

D. Noise Elimination Strategy

Two methods, a voltage error analytical algorithm and a current circuit equation algorithm have been introduced above to calculate the output pole voltage.

In ideal situations, there is

$$V^*_{XM}=V^C_{XM}. \tag{13}$$

However, ΔV^C_{XM} is full of noise around the sampling frequency, which interferes with effective OC fault information. To clearly illustrate this problem, simulation waveforms of V^*_{AM1} and V^C_{AM} (a S_{A1} OC fault, for example) with a rectifier load are shown in Fig. 10, while $f_S=1/T_S$=80kHz and f_{switch}=10kHz.

As shown in Fig. 10, (13) fails under both the healthy and fault conditions. In order to use V^*_{XM} and V^C_{XM} as an OC

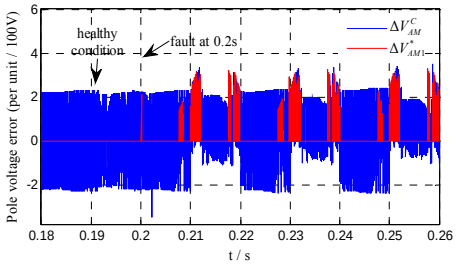


Fig. 10. Waveforms of V^C_{AM} and V^*_{AM1} of S_{A1} OC fault with rectifier load.

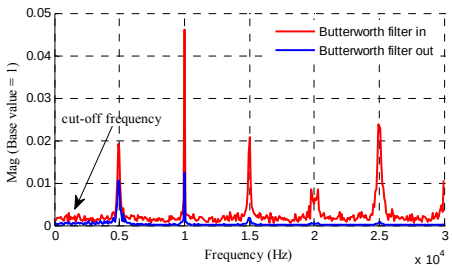


Fig. 11. Frequency spectrum of V^C_{AM} before and after designed second-order Butterworth filter.

fault diagnostic reference, a second-order Butterworth filter noise elimination strategy is proposed. Butterworth demonstrated a low pass filter whose frequency response (gain) is:

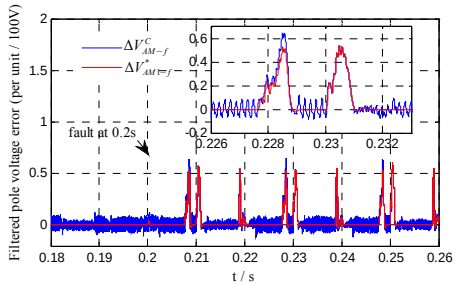
$$G(\omega)=|H(j\omega)|=\frac{1}{\sqrt{1+(\omega/\omega_{cut\text{-}off})^2}}, \tag{14}$$

where $\omega_{cut\text{-}off}=2\pi f_{cut\text{-}off}$ is the angular frequency in radians per second. If $\omega/\omega_{cut\text{-}off}$=1, the amplitude response of this filter in the passband is $1/\sqrt{2}$ ≈0.707(-3dB). If $\omega/\omega_{cut\text{-}off}$>1, the response slopes off linearly toward negative infinity at -40dB per decade.

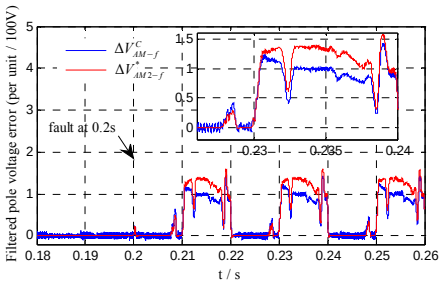
In this paper, $f_{cut\text{-}off}$ is set to 2kHz, which is less than f_{switch}. V^C_{AM}, under healthy conditions (i.e. t<0.2s in Fig. 10), is brought into the designed second-order Butterworth filter and the frequency spectrum of the filter input and output are shown in Fig. 11, where the high frequency component gain is significantly attenuated as a result.

Then, V^C_{AM} and V^*_{AM1} of a S_{A1} OC fault with a rectifier load, shown in Fig. 10, are both brought into Butterworth filters and turn into what is shown in Fig. 12(a), where $V^C_{XM\text{-}f}$ and $V^*_{XM\text{-}f}$ are defined as the output of the Butterworth filters, and $V^*_{XM\text{-}f}=\{V^*_{XMi\text{-}f},\ i=1,2,3 \text{ or } 4\}$. Similarly, simulation results of S_{A2}, S_{A3} and S_{A4} OC faults with a rectifier load are shown in Fig. 12(b)-(d), respectively. Here, the simulation parameters are the same as those shown in Fig. 4 and Table II.

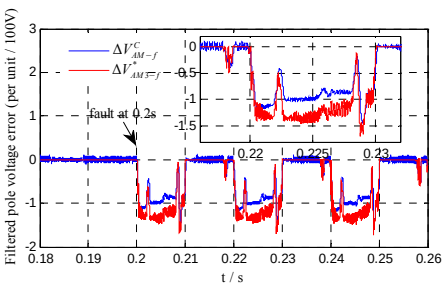
For inductive and capacitive load conditions, the Butterworth filter also achieves a very good performance in V^C_{AM} and V^*_{AM} noise elimination, which is shown in Fig. 13(a)-(d) and Fig. 14(a)-(d).



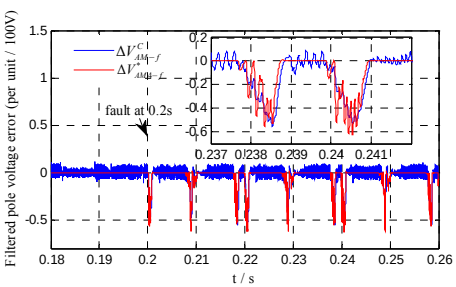
(a)



(b)

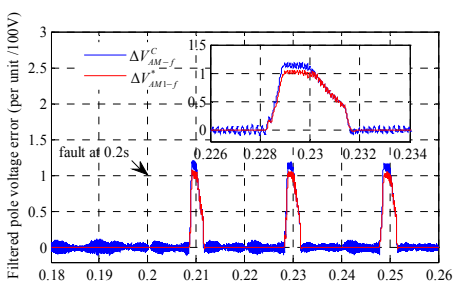


(c)

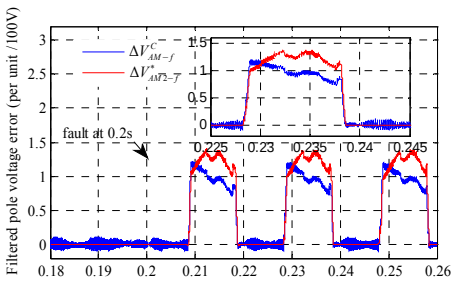


(d)

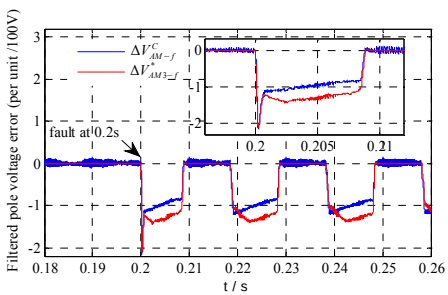
Fig. 12. Filtered pole voltage error of Leg *A* by 2 proposed algorithms when: (a) S_{A1} OC fault, (b) S_{A2} OC fault, (c) S_{A3} OC fault and (d) S_{A4} OC fault with rectifier load.



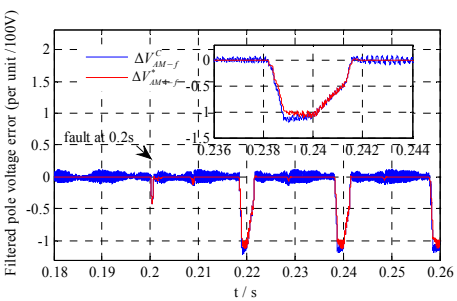
(a)



(b)

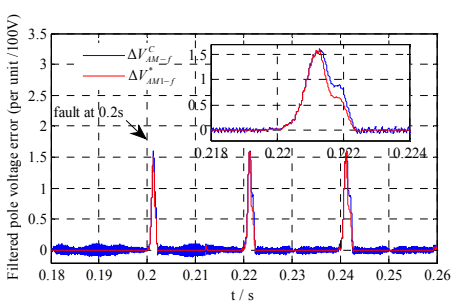


(c)

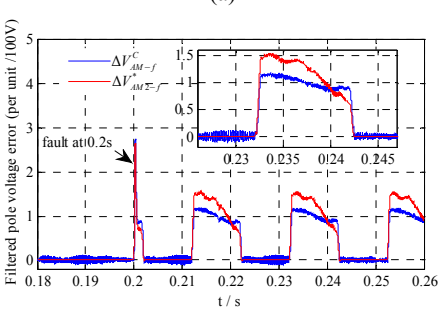


(d)

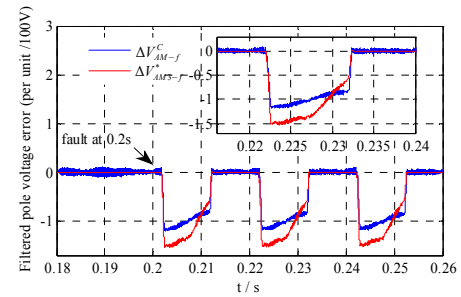
Fig. 13. Filtered pole voltage error of Leg *A* by 2 proposed algorithms when: (a) S_{A1} OC fault, (b) S_{A2} OC fault, (c) S_{A3} OC fault and (d) S_{A4} OC fault with inductive load.



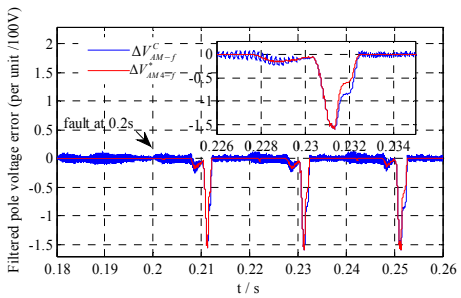
(a)



(b)



(c)



(d)

Fig. 14. Filtered pole voltage error of Leg *A* by 2 proposed algorithms when: (a) S_{A1} OC fault, (b) S_{A2} OC fault, (c) S_{A3} OC fault and (d) S_{A4} OC fault with capacitive load.

As shown in Fig. 12, Fig. 13 and Fig. 14, $V^{C}_{XM\text{-}f}$ and $V^{*}_{XM\text{-}f}$ match each other perfectly under various loads conditions. The calculation of the error voltage is independent of load changes. For inductive, capacitive and rectifier loads, this method has a high accuracy and adaptability. It is worth emphasizing that, during the filtering process, part of the effective fault information will be filtered too, resulting in an amplitude reduction of useful information. However, this does not affect the distinction between the fault waveforms.

As shown in Fig. 12, Fig. 13 and Fig. 14, $V^{*}_{XM\text{-}f}$ under all of the IGBT OC faults are so different from each other that $V^{*}_{XM\text{-}f}$ can be treated as a fault feature. When a certain IGBT comes to a fault, $V^{C}_{XM\text{-}f}$ can be compared with $V^{*}_{XM1\text{-}f}$, $V^{*}_{XM2\text{-}f}$, $V^{*}_{XM3\text{-}f}$ and $V^{*}_{XM4\text{-}f}$, respectively, and the fault can be located by its similarity.

E. OC Fault Diagnosis based on Voltage Error Correlation

Let v_1 and v_2 be random variables having finite means. Let $E(v_1)$ and $E(v_2)$ be expectations of v_1 and v_2, respectively. The covariance of v_1 and v_2, which is denoted by $Cov(v_1, v_2)$, is defined as:

$$Cov(v_1, v_2)=E[(v_1-E(v_1))\cdot(v_2-E(v_2))]. \tag{15}$$

Then the correlation of v_1 and v_2, which is denoted by $\mu(v_1, v_2)$, is defined as follows:

$$\mu(v_1,v_2)=\frac{Cov(v_1,v_2)}{\sqrt{E\{[v_1-E(v_1)]^2\}}\cdot\sqrt{E\{[v_1-E(v_1)]^2\}}}. \tag{16}$$

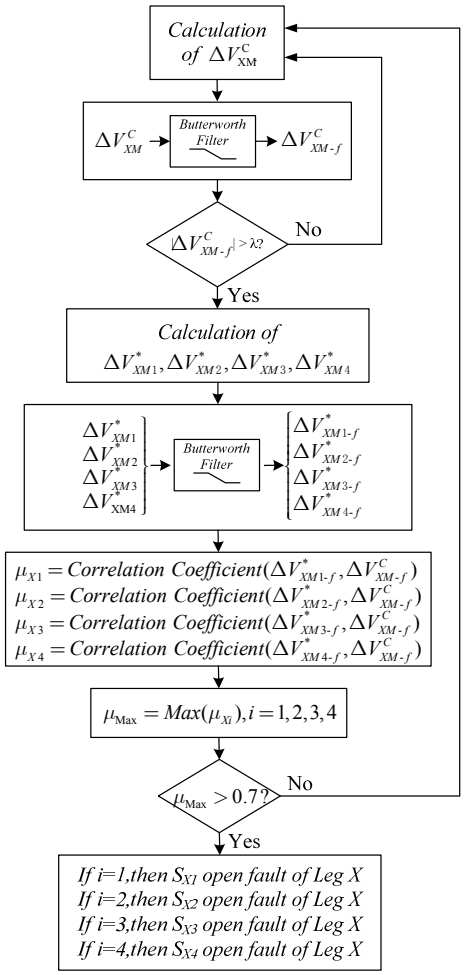


Fig. 15. Proposed OC fault diagnosis algorithm.

(15) and (16) can be used to measure the association between two random variables v_1 and v_2, where (15) is normalized to "1" through (16).

The proposed OC fault diagnosis is implemented as follows: First, a pole voltage error V^{C}_{XM} of three phases is calculated through the current circuit equation algorithm and then filtered, where $V^{C}_{XM\text{-}f}$ is obtained. Second, if $V^{C}_{XM\text{-}f}$ of a certain phase is greater than λ(e.g., λ=0.5), then *X* phase is judged with an OC open fault. Third, once an OC open fault is confirmed, (9) comes to alive and V^{*}_{XM1}, V^{*}_{XM2}, V^{*}_{XM3} and V^{*}_{XM4} are calculated through the voltage error analytical algorithm. Then V^{*}_{XM1}, V^{*}_{XM2}, V^{*}_{XM3} and V^{*}_{XM4} are filtered, and $V^{*}_{XM1\text{-}f}$, $V^{*}_{XM2\text{-}f}$, $V^{*}_{XM3\text{-}f}$ and $V^{*}_{XM4\text{-}f}$ are obtained. Fourth, assuming that $\mu_{Xi}=\mu(V^{C}_{XM\text{-}f}, V^{*}_{XMi\text{-}f})$($X\in A,B$ or C; i=1,2,3 or 4), μ_{X1}, μ_{X2}, μ_{X3} and μ_{X4} are calculated by (16). Finally, assuming that μ_{Xi} is the maximum of μ_{X1}, μ_{X2}, μ_{X3} and μ_{X4} then S_{Xi} is an OC fault IGBT as the final diagnosis result. Furthermore, to prevent the occurrence of a misdiagnosis, μ_{Xi} of the fault IGBT must be greater than a certain value (e.g., 0.7), or the diagnosis result will be abandoned. The proposed algorithm is shown in Fig. 15.

TABLE III
SIMULATION RESULT WITH RECTIFIER LOAD

phase A	μ_{A1}	μ_{A2}	μ_{A3}	μ_{A4}
S_{A1} open fault	0.8211▲	0.3897	0.0775	-0.0798
S_{A2} open fault	0.5040	0.9882▲	0.8987	0.4170
S_{A3} open fault	0.4313	0.9035	0.9898▲	0.5069
S_{A4} open fault	0.0083	0.1629	0.5092	0.8681▲
phase B	μ_{B1}	μ_{B2}	μ_{B3}	μ_{B4}
S_{B1} open fault	0.9055▲	0.4879	0.1597	0.0348
S_{B2} open fault	0.5248	0.9886▲	0.9055	0.4530
S_{B3} open fault	0.3884	0.9030	0.9894▲	0.5201
S_{B4} open fault	0.0318	0.1623	0.5377	0.9178▲
phase C	μ_{C1}	μ_{C2}	μ_{C3}	μ_{C4}
S_{C1} open fault	0.9037▲	0.5687	0.1924	0.0594
S_{C2} open fault	0.5113	0.9896▲	0.9062	0.4728
S_{C3} open fault	0.4550	0.9038	0.9899▲	0.5042
S_{C4} open fault	0.0710	0.2095	0.6114	0.9232▲

▲ Maximum μ_X of S_{Xi} open fault, and fault IGBT located here.

TABLE IV
SIMULATION RESULT WITH INDUCTIVE LOAD

phase A	μ_{A1}	μ_{A2}	μ_{A3}	μ_{A4}
S_{A1} open fault	0.9822▲	0.4885	0.4623	0.2865
S_{A2} open fault	0.6461	0.9424▲	0.8135	0.4113
S_{A3} open fault	0.4204	0.7981	0.9448▲	0.6447
S_{A4} open fault	0.2484	0.4377	0.5564	0.9834▲
phase B	μ_{B1}	μ_{B2}	μ_{B3}	μ_{B4}
S_{B1} open fault	0.9834▲	0.4908	0.4605	0.2539
S_{B2} open fault	0.6511	0.9407▲	0.8117	0.4151
S_{B3} open fault	0.4221	0.7970	0.9438▲	0.6487
S_{B4} open fault	0.2542	0.4463	0.5581	0.9824▲
phase C	μ_{C1}	μ_{C2}	μ_{C3}	μ_{C4}
S_{C1} open fault	0.9825▲	0.4849	0.4571	0.2508
S_{C2} open fault	0.6447	0.9406▲	0.8136	0.4144
S_{C3} open fault	0.4193	0.7965	0.9460▲	0.6501
S_{C4} open fault	0.2519	0.4412	0.5632	0.9836▲

▲ Maximum μ_X of S_{Xi} open fault, and fault IGBT located here.

TABLE V
SIMULATION RESULT WITH CAPACITIVE LOAD

phase A	μ_{A1}	μ_{A2}	μ_{A3}	μ_{A4}
S_{A1} open fault	0.9705▲	0.5833	0.4250	0.2308
S_{A2} open fault	0.5659	0.9426▲	0.8700	0.4476
S_{A3} open fault	0.4348	0.8574	0.9455▲	0.5475
S_{A4} open fault	0.2308	0.4154	0.5853	0.9658▲
phase B	μ_{B1}	μ_{B2}	μ_{B3}	μ_{B4}
S_{B1} open fault	0.9714▲	0.5835	0.4246	0.2300
S_{B2} open fault	0.5680	0.9438▲	0.8690	0.4457
S_{B3} open fault	0.4356	0.8594	0.9445▲	0.5419
S_{B4} open fault	0.2289	0.4145	0.5865	0.9651▲
phase C	μ_{C1}	μ_{C2}	μ_{C3}	μ_{C4}
S_{C1} open fault	0.9709▲	0.5843	0.4243	0.2293
S_{C2} open fault	0.5614	0.9441▲	0.8700	0.4431
S_{C3} open fault	0.4341	0.8573	0.9457▲	0.5450
S_{C4} open fault	0.2262	0.4097	0.5951	0.9665▲

▲ Maximum μ_X of S_{Xi} open fault, and fault IGBT located here.

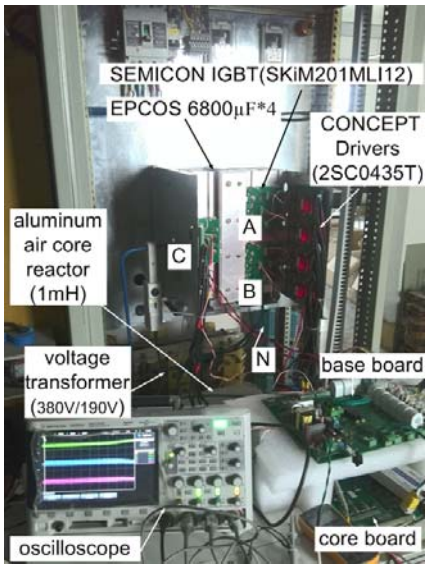


Fig. 16. Experimental prototype.

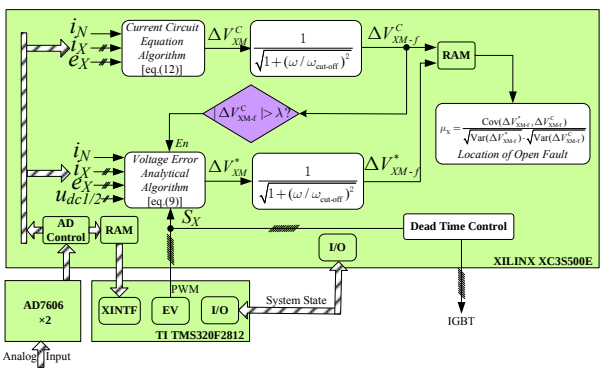


Fig. 17. FPGA implementation of proposed OC fault diagnosis algorithm.

Simulation results for all twelve of the IGBTs with a rectifier load, an inductive load, and a capacitive load are shown in Table III, IV and V, with the simulation parameters in Fig. 4 and Table II. For various load conditions, the diagnostic accuracy is up to 100%. These results demonstrate the good performance of the proposed algorithm.

III. EXPERIMENTAL RESULTS

A 3-phase 4-wire 3-level NPC prototype is developed to validate the proposed OC fault diagnosis algorithm, as shown in Fig. 16. A rectifier load, an inductive load and a capacitive load, as shown in Fig. 4, are all considered to verify the adaptability of the proposed method. The experimental parameters are the same as simulation parameters shown in Table II.

In the process of OC fault diagnosis, the pulse state is involved in calculation, which requires a high sampling frequency and a fast computing controller. Therefore, a control unit based on a FPGA+DSP is developed, in which the FPGA is mainly working on proposed algorithm and the

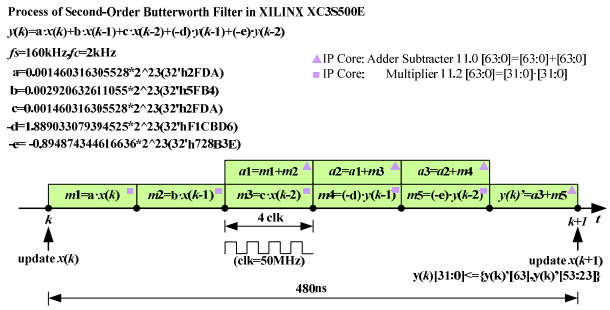
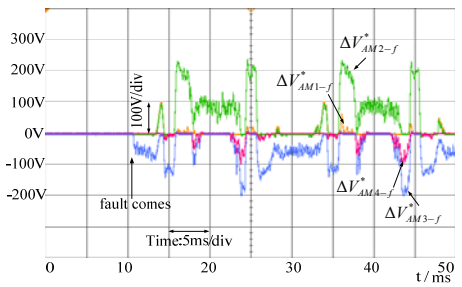
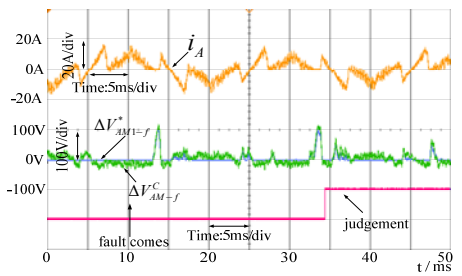


Fig. 18. Process of second-order Butterworth filter in FPGA.



(a)



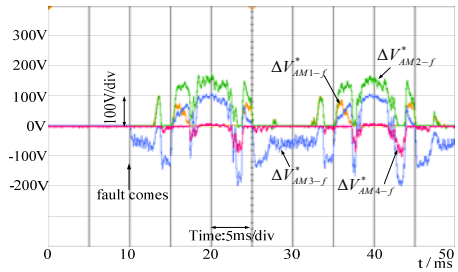
(b)

Fig. 19. Waveforms of S_{A1} OC faults: (a) $V^*_{AM1\text{-}f}$, $V^*_{AM2\text{-}f}$, $V^*_{AM3\text{-}f}$ and $V^*_{AM4\text{-}f}$; (b) i_A, $V^C_{AM\text{-}f}$, $V^*_{AM1\text{-}f}$ and judging signal with rectifier load.

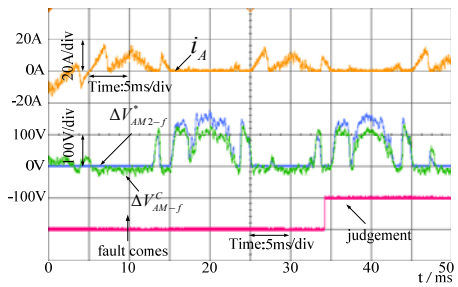
DSP is for the APF double closed-loop control. The diagnosis part is shown in Fig. 17.

The sampling frequency of an AD7606 (16 bits) is set to f_s=80kHz(8 times the f_{switch}). Thus, V^C_{XM} and V^*_{XM} are updated every 12.5μs (i.e. 80kHz). According to Shannon's sampling theorem, for a given sample rate f_s, perfect reconstruction is guaranteed to be possible for a band-limit $B_s < f_s/2$. Therefore, the discrete second-order Butterworth filter is designed with a sample time of 160kHz. The process of this filter is shown in Fig. 18. At least 480ns is needed for one variable filtering, which is far less than 6.25μs (i.e. 160kHz).

To save the FPGA's resources and to shorten the calculation time, only a period of 20ms is utilized for $V^C_{XM\text{-}f}$ and $V^*_{XMi\text{-}f}$ data saving, which begins at the moment of $V^C_{XM\text{-}f} > \lambda$(i.e. 0.5). In addition, only 128 data of $V^C_{XM\text{-}f}$ and $V^*_{XMi\text{-}f}$ are saved into RAM to wait for correlation judgment. Here 128 data are obtained with a sampling time of 156.25μs during 20ms.



(a)



(b)

Fig. 20. Waveforms of S_{A2} OC faults: (a) $V^*_{AM1\text{-}f}$, $V^*_{AM2\text{-}f}$, $V^*_{AM3\text{-}f}$ and $V^*_{AM4\text{-}f}$; (b) i_A, $V^C_{AM\text{-}f}$, $V^*_{AM2\text{-}f}$ and judging signal with rectifier load.

TABLE VI
EXPERIMENTAL RESULT WITH RECTIFIER LOAD

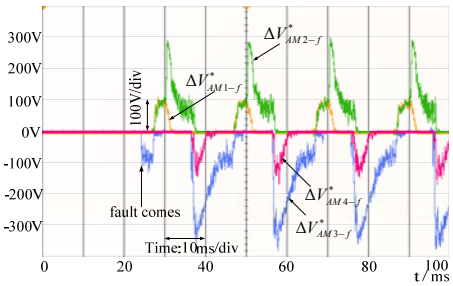
phase *A*	μ_{A1}	μ_{A2}	μ_{A3}	μ_{A4}
S_{A1} open fault	0.8151▲	0.5473	0.6104	0.2174
S_{A2} open fault	0.5083	0.9655▲	0.8924	0.3169
S_{A3} open fault	0.3539	0.9018	0.9650▲	0.4979
S_{A4} open fault	0.2327	0.6392	0.5492	0.7734▲
phase *B*	μ_{B1}	μ_{B2}	μ_{B3}	μ_{B4}
S_{B1} open fault	0.7539▲	0.6523	0.6330	0.1817
S_{B2} open fault	0.4995	0.9733▲	0.9112	0.3643
S_{B3} open fault	0.3874	0.9233	0.9767▲	0.4609
S_{B4} open fault	0.1395	0.4867	0.4328	0.8517▲
phase *C*	μ_{C1}	μ_{C2}	μ_{C3}	μ_{C4}
S_{C1} open fault	0.8614▲	0.4967	0.4725	0.1427
S_{C2} open fault	0.4685	0.9765▲	0.9005	0.2872
S_{C3} open fault	0.3426	0.9159	0.9752▲	0.4573
S_{C4} open fault	0.1836	0.6137	0.5152	0.7314▲

▲ Maximum μ_X of S_{Xi} open fault, and fault IGBT located here.

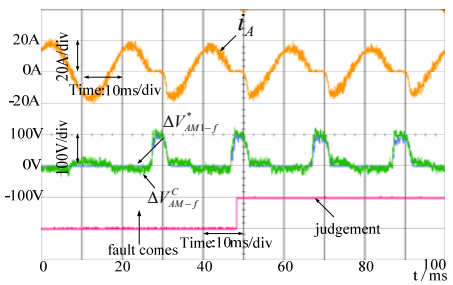
Experimental results with a rectifier load are shown in Fig. 19 and Fig. 20. Fig. 19 displays waveforms of S_{A1} OC faults, and Fig. 20 displays waveforms of S_{A2} OC faults. Table VI shows μ_X and the judgments for all twelve IGBT OC faults with the rectifier load condition.

Experimental results with an inductive load are shown in Fig. 21 and Fig. 22. Fig. 21 displays waveforms of S_{A1} OC faults, and Fig. 22 displays waveforms of S_{A2} OC faults. Table VII shows μ_X and the judgments for all twelve IGBT OC faults with the inductive load condition.

Experimental results with an inductive load are shown in Fig. 23 and Fig. 24. Fig. 23 displays waveforms of S_{A1} OC

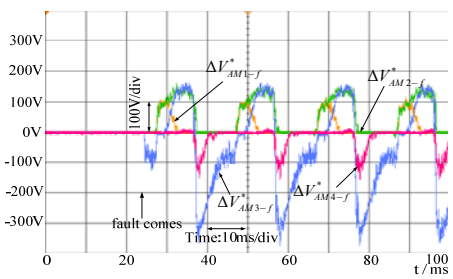


(a)

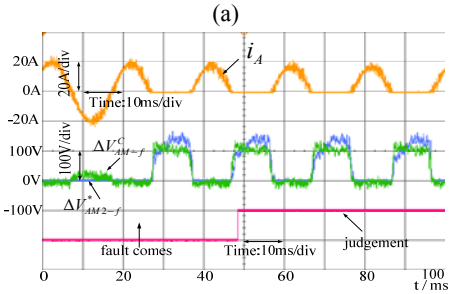


(b)

Fig. 21. Waveforms of S_{A1} OC faults: (a) $V^*_{AM1\text{-}f}$, $V^*_{AM2\text{-}f}$, $V^*_{AM3\text{-}f}$ and $V^*_{AM4\text{-}f}$; (b) i_A, $V^C_{AM\text{-}f}$, $V^*_{AM1\text{-}f}$ and judging signal with inductive load.

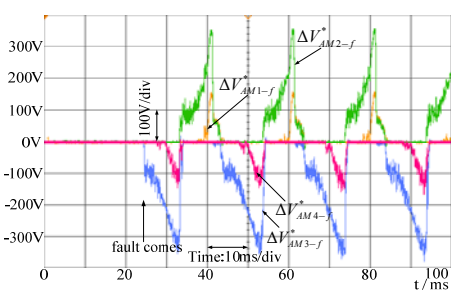


(a)



(b)

Fig. 22. Waveforms of S_{A2} OC faults: (a) $V^*_{AM1\text{-}f}$, $V^*_{AM2\text{-}f}$, $V^*_{AM3\text{-}f}$ and $V^*_{AM4\text{-}f}$; (b) i_A, $V^C_{AM\text{-}f}$, $V^*_{AM2\text{-}f}$ and judging signal with inductive load.



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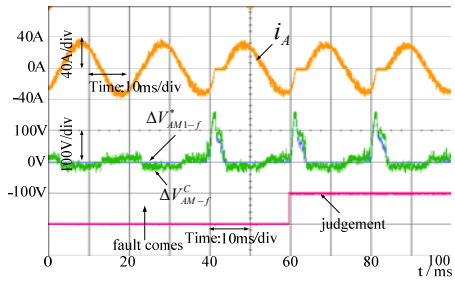
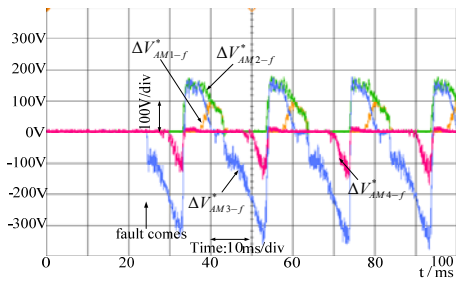
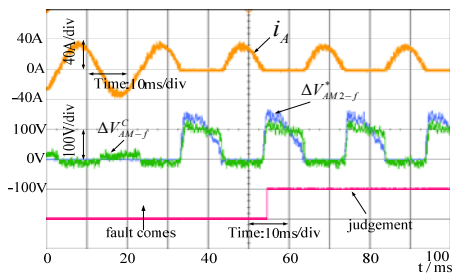


(b)

Fig. 23. Waveforms of S_{A1} OC faults: (a) $V^*_{AM1\text{-}f}$, $V^*_{AM2\text{-}f}$, $V^*_{AM3\text{-}f}$ and $V^*_{AM4\text{-}f}$; (b) i_A, $V^C_{AM\text{-}f}$, $V^*_{AM1\text{-}f}$ and judging signal with capacitive load.



(a)



(b)

Fig. 24. Waveforms of S_{A2} OC faults: (a) $V^*_{AM1\text{-}f}$, $V^*_{AM2\text{-}f}$, $V^*_{AM3\text{-}f}$ and $V^*_{AM4\text{-}f}$; (b) i_A, $V^C_{AM\text{-}f}$, $V^*_{AM2\text{-}f}$ and judging signal with capacitive load.

TABLE VII
EXPERIMENTAL RESULT WITH INDUCTIVE LOAD

phase *A*	μ_{A1}	μ_{A2}	μ_{A3}	μ_{A4}
S_{A1} open fault	0.9584▲	0.5971	0.5848	0.3450
S_{A2} open fault	0.6459	0.9423▲	0.8253	0.4319
S_{A3} open fault	0.4333	0.8186	0.9250▲	0.6339
S_{A4} open fault	0.3486	0.5714	0.5926	0.9468▲
phase *B*	μ_{B1}	μ_{B2}	μ_{B3}	μ_{B4}
S_{B1} open fault	0.9605▲	0.5622	0.5588	0.3086
S_{B2} open fault	0.6327	0.9361▲	0.8241	0.4208
S_{B3} open fault	0.4112	0.8278	0.9413▲	0.6365
S_{B4} open fault	0.3222	0.5819	0.6291	0.9521▲
phase *C*	μ_{C1}	μ_{C2}	μ_{C3}	μ_{C4}
S_{C1} open fault	0.9489▲	0.5619	0.5888	0.3421
S_{C2} open fault	0.6295	0.9396▲	0.8328	0.4376
S_{C3} open fault	0.4224	0.8216	0.9369▲	0.6492
S_{C4} open fault	0.3173	0.5786	0.6118	0.9513▲

▲ Maximum μ_X of S_{Xi} open fault, and fault IGBT located here.

TABLE VIII
EXPERIMENTAL RESULT WITH CAPACITIVE LOAD

phase *A*	μ_{A1}	μ_{A2}	μ_{A3}	μ_{A4}
S_{A1} open fault	0.9580▲	0.5787	0.5706	0.3213
S_{A2} open fault	0.6420	0.9440▲	0.8322	0.4396
S_{A3} open fault	0.4268	0.8146	0.9286▲	0.6372
S_{A4} open fault	0.3482	0.5824	0.5998	0.9448▲
phase *B*	μ_{B1}	μ_{B2}	μ_{B3}	μ_{B4}
S_{B1} open fault	0.9590▲	0.5628	0.5637	0.3062
S_{B2} open fault	0.6325	0.9362▲	0.8283	0.4315
S_{B3} open fault	0.4112	0.8278	0.9413▲	0.6365
S_{B4} open fault	0.3222	0.5819	0.6291	0.9521▲
phase *C*	μ_{C1}	μ_{C2}	μ_{C3}	μ_{C4}
S_{C1} open fault	0.9489▲	0.5619	0.5888	0.3421
S_{C2} open fault	0.6295	0.9396▲	0.8328	0.4376
S_{C3} open fault	0.4224	0.8216	0.9369▲	0.6492
S_{C4} open fault	0.3173	0.5786	0.6118	0.9513▲

▲ Maximum μ_X of S_{Xi} open fault, and fault IGBT located here.

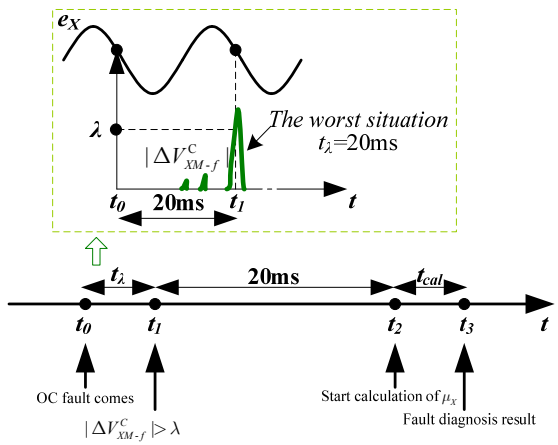


Fig. 25. Response time of the given OC fault algorithm.

faults, and Fig. 24 displays waveforms of S_{A2} OC faults. Table VIII shows μ_X and the judgments for all twelve IGBT OC faults with the capacitive load condition.

In Table VI, VII and VIII, experimental results of the proposed algorithm are shown under various loads. All twelve IGBTs OC fault are successfully located with different power conditions, which shows the good performance of the proposed method.

The whole diagnosis response time costs t_λ+20ms+t_{cal}, as shown in Fig. 25. Here, 20ms refers to a whole supply period, during which the processes of relevant variable sampling, computing and storage are repeatedly done. t_{cal} stands for the correlation calculation, which is mainly determined by the max clock frequency in the FPGA. For the 50MHz clock frequency condition, t_{cal} has been tested at less than 100μs. t_λ is defined as the time between the coming moment of an OC fault and the moment $|\Delta V^C_{XM}|>\lambda$ arrives. t_λ is not a fixed value that is dependent on load changes and fault's coming moment. Therefore, it is really hard to precisely calculate the value of t_λ. However, it can be sure that $|\Delta V^C_{XM}|>\lambda$ will occur in the next 20ms of the OC coming moment and that t_λ is definitely less than a supply period (20ms). t_λ can be 0ms, which means that $|\Delta V^C_{XM}|>\lambda$ occurs right after the coming moment of an OC fault. On the other hand, the worst situation for t_λ is illustrated in Fig. 25, where t_λ=20ms. In conclusion, the diagnosis response time for the proposed algorithm is between 20.1 ms~40.1ms.

IV. CONCLUSIONS

A novel open-circuit fault diagnosis method for 3-phase 4-wire 3-level active power filters based on voltage error correlation is proposed in this paper. The method is based on converter output pole voltage error observing. A comparison between the actual pole voltage error and the analytic expecting voltage error under fault conditions is implemented though a FPGA and a correlation is introduced to locate the OC fault IGBT. A Butterworth filter is considered to eliminate the noise caused by the discrete system accuracy limitation. The zero current condition is considered and no additional sensors are needed. In addition, high location accuracy is guaranteed through this method.

The proposed method is independent of various loads conditions, such as a rectifier load, an inductive load and a capacitive load. It has good performance under unbalanced load current situations and both effectiveness and reliability can be achieved.

There are some drawbacks to the given method. The proposed method must be implemented on a very fast digital target, such as a FPGA or a CPLD, which increases the hardware costs. In addition, ADCs with a very high frequency bandwidth are required.

The simulation and experimental results demonstrate the good performance of the algorithm. An OC fault can be located within 40.1ms. This response time is acceptable, since it is accompanied by a higher reliability and accuracy.

REFERENCES

[1] A. Ametanid, "Harmonic reduction in thyristor converters by harmonic current injection," *IEEE Trans. Power App. Syst.*, Vol. 95, No. 2, pp. 441-449, Mar./Apr. 1976.

[2] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, Vol. 25, No. 11, pp. 2734-2752, Nov. 2010.

[3] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 3, pp. 1441-1451, May/Jun. 2011.

[4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I.

Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.

[5] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardeau "Survey on fault operation on multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2207-2218, Jul. 2010.

[6] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, utility applications," *IEEE Trans. Ind. Appl.*, Vol. 41, No. 3, pp. 855-865, May/Jun. 2005.

[7] U. -M. Choi, H. -G. Jeong, K. -B. Lee, and F. Blaabjerg, "Method for detecting an open-switch fault in a grid-connected NPC inverter system," *IEEE Trans. Power Electron.*, Vol. 27, No. 6, pp. 2726-2739, Jun. 2012.

[8] W.-S. Im, J.-M. Kim, D.-C. Lee, and K.-B. Lee, "Diagnosis and fault-tolerant control of three-phase AC-DC PWM converter systems," *IEEE Trans. Ind. Appl.*, Vol. 49, pp. 1539-1547, Jul./Aug. 2013.

[9] U. -M. Choi, K. -B. Lee, and F. Blaabjerg, "Diagnosis and Tolerant Strategy of an Open-Switch Fault for T-Type Three-Level Inverter Systems," *IEEE Trans. Ind. Appl.*, Vol. 50, No. 1, pp. 495-508, Jan./Feb. 2014.

[10] U. -M. Choi, F. Blaabjerg, J. -S. Lee, and K. -B. Lee, "Open-circuit fault diagnosis for a grid-connected NPC inverter with unity power factor," in *Proc. IEEE APEC*, pp. 213-220, 2015

[11] U. -M. Choi, J. -S. Lee, F. Blaabjerg, and K. -B. Lee, "Open-circuit fault diagnosis and fault-tolerant control for a grid-connected NPC inverter," *IEEE Early Access Articles*, 2015.

[12] J. -S. Lee, and K. -B. Lee, "Open-Circuit Fault-Tolerant Control for Outer Switches of Three-Level Rectifiers in Wind Turbine Systems," *IEEE Trans. Power Electron.*, Vol. 31, No. 5, May 2016.

[13] J. O. Estima and A. J. M. Cardoso, "A new algorithm for real-time multiple open-circuit fault diagnosis in voltage-fed PWM motor drives by the reference current errors," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 8, pp. 3496-3505, Aug. 2013.

[14] N. M. A. Freire, J. O. Estima, and A. J. M. Cardoso, "Open-circuit fault diagnosis in PMSG drives for wind turbine applications," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 9, pp. 3957-3967, Sep. 2013.

[15] A. M. S. Mendes, M. B. Abadi, and S. M. A. Cruz, "Fault diagnostic algorithm for three-level neutral point clamped AC motor drives, based on the average current Park's vector," *IET Power Electron.*, Vol. 7, No. 5, pp. 1127-1137, May 2014.

[16] N. M. A. Freire, J. O. Estima, and A. J. M. Cardoso, "A voltage-based approach without extra hardware for open-circuit fault diagnosis in closed-loop PWM AC regenerative drives," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 9, pp. 4960-4970, Sep. 2014.

[17] S.-M. Jung, J.-S. Park, H.-W. Kim, K.-Y. Cho, and M.-J. Youn, "An MRAS-based diagnosis of open-circuit fault in PWM voltage-source inverters for PM synchronous motor drive systems," *IEEE Trans. Power Electron.*, Vol. 28, No. 5, pp. 2514-2526, May 2013.

[18] X. Pei, S. Nie, Y. Chen, and Y. Kang, "Open-circuit fault diagnosis and fault-tolerant strategies for full-bridge DC-DC converters," *IEEE Trans. Power Electron.*, Vol. 27, No. 5, pp. 2550-2565, May 2012.

[19] J. O. Estima, N. M. A. Freire, and A. J. M. Cardoso, "Recent advances in fault diagnosis by Park's vector approach," in *Proc. IEEE WEMDCD*, pp. 279-288, 2013.

[20] A. M. S. Mendes, A. J. M. Cardoso, and E. S. Saraiva, "Voltage source inverter fault diagnosis in variable speed ac drives, by Park's vector approach," in *Proc. 7th Int. Conf. Power Electron. Variable Speed Drives* (456), pp. 538-543, 1998.

[21] J. A. A. Caseiro, A.M. S.Mendes, and A. J.M. Cardoso, "Open-circuit fault diagnosis and fault-tolerant control for a grid-connected NPC inverter tolerance using the average current park's vector approach," in *Proc. IEEE IEMDC, Miami, FL, USA, 2009*, pp. 695-701, 2009.

[22] R. Peuget, S. Courtine, and J. P. Rognon, "Fault detection and isolation on a PWM inverter by knowledge-based model," *IEEE Trans. Ind. Appl.*,Vol. 34, No. 6, pp. 1318-1326, Nov./Dec. 1998.

[23] M. Trabelsi, M. Boussak, and M. Gossa, "Multiple IGBTs open circuit faults diagnosis in voltage source inverter fed induction motor using modified slope method," in *Proc. XIX Int. Conf. Electr. Mach.*, pp. 1-6, 2010

[24] W. Sleszynski, J. Nieznanski, and A. Cichowski, "Open-transistor fault diagnostics in voltage-source inverters by analyzing the load currents," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 11, pp. 4681-4688, Nov. 2009.

[25] J. O. Estima and A. J. M. Cardoso, "A new approach for real-time multiple open-circuit fault diagnosis in voltage source inverters," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 6, pp. 2487-2494, Nov./Dec. 2011.

[26] N. M. A. Freire, J. O. Estima, and A. J. M. Cardoso, "Multiple open-circuit fault diagnosis in voltage-fed PWM motor drives using the current Park's vector phase and the currents polarity," in *Proc. 8th IEEE Int. Symp. Diagnost. Elect. Mach.*, Power Electron. Drives, pp. 397-404, 2011.

[27] N. M. A. Freire, J. O. Estima, and A. J. M. Cardoso, "A voltage-based approach without extra hardware for open-circuit fault diagnosis in closed-loop PWM AC regenerative drives," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 9, pp. 4960-4970, Sep. 2014.

[28] M. Shahbazi, P. Poure, S. Saadate, and M. R. Zolghadri, "FPGA-based fast detection with reduced sensor count for a fault-tolerant three-phase converter," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 3, pp. 1343-1350, Aug. 2013.

[29] R. Ribeiro, C. Jacobina, E. da Silva, and A. Lima, "Fault detection of open-switch damage in voltage-fed PWM motor drive systems," *IEEE Trans. Power Electron.*, Vol. 18, No. 2, pp. 587-593, Mar. 2003.

[30] S. Karimi, A. Gaillard, P. Poure, and S. Saadate, "FPGA-based real-time power converter failure diagnosis for wind energy conversion systems," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 12, pp. 4299-4308, Dec. 2008

[31] Q.-T. An, L.-Z. Sun, K. Zhao, and L. Sun, "Switching function model-based fast-diagnostic method of open-switch faults in inverters without sensors," *IEEE Trans. Power Electron.*, Vol. 26, No. 1, pp. 119-126, Jan. 2011.

[32] M. R. Mamat, M. Rizon, and M. S. Khanniche, "Fault detection of 3-phase VSI using wavelet-fuzzy algorithm," *Amer. J. Appl. Sci.*, Vol.3, No. 1, pp. 1642-1648, Mar. 2006.

[33] F. Charfi, F. Sellami, and K. Al-Haddad, "Fault diagnosis in power system using wavelet transforms and neural networks," in *Proc. IEEE Int. Symp. Ind. Electron.*, pp. 1143-1148, 2006.

[34] K. Debebe, V. Rajagopalan, and T. S. Sankar, "Expert systems for fault diagnosis of VSI fed ac drives," in *Conf. Rec. IEEE IAS Annu. Meeting*, pp. 368-373, 1991.

[35] H. E. Brouji, P. Poure, and S. Saadate, "A fast and reliable fault diagnosis method for fault tolerant shunt three-phase active filter," in *IEEE Int. Symp. on Ind. Electron. (ISIE)*, pp. 1688-1693, 2006.
[36] S. Karimi, P. Poure, S. Saadate, and E. Gholipour, "Current sensors and power switches fault detection and compensation for shunt active power filters," in *Ind. Electron. ISIE*, pp. 3157-3161, 2007.
[37] P. F. Lopes and A. M. S. Mendes, "Fault tolerance in active power filters, based on multilevel NPC topology," in *Proc. 38th IEEE IECON, Montréal, QC, Canada*, pp. 410-415, 2012.
[38] L. M. A. Caseiro, A. M. S. Mendes, and P. M. A. F. Lopes, "Open-circuit fault diagnosis in neutral-point-clamped active power filters based on instant voltage error with no additional sensors," in *Proc. IEEE APEC*, pp. 2217-2222, 2015.
[39] L. M. A. Caseiro, A. M. S. Mendes, "Real-time IGBT open-circuit fault diagnosis in three-level neutral-point-clamped voltage-source rectifiers based on instant voltage error," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 3, pp. 1669-1678, Mar. 2015.
[40] O. Vodyakho and C. C. Mi, "Three-level inverter-based shunt active power filter in three-phase three-wire and four-wire systems," *IEEE Trans. Power Electron.*, Vol. 24, No. 5, pp. 1350-1363, May. 2009.

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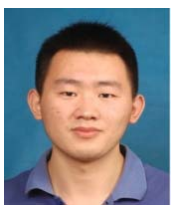

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