

A Simplified Synchronous Reference Frame for Indirect Current Controlled Three-level Inverter-based Shunt Active Power Filters

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Abstract

This paper presents a new simplified harmonics extraction algorithm based on the synchronous reference frame (SRF) for an indirect current controlled (ICC) three-level neutral point diode clamped (NPC) inverter-based shunt active power filter (SAPF). The shunt APF is widely accepted as one of the most effective current harmonics mitigation tools due to its superior adaptability in dynamic state conditions. In its controller, the SRF algorithm which is derived based on the direct-quadrature (DQ) theory has played a significant role as a harmonics extraction algorithm due to its simple implementation features. However, it suffers from significant delays due to its dependency on a numerical filter and unnecessary computation workloads. Moreover, the algorithm is mostly implemented for the direct current controlled (DCC) based SAPF which operates based on a non-sinusoidal reference current. This degrades the mitigation performances since the DCC based operation does not possess exact information on the actual source current which suffers from switching ripples problems. Therefore, three major improvements are introduced which include the development of a mathematical based fundamental component identifier to replace the numerical filter, the removal of redundant features, and the generation of a sinusoidal reference current. The proposed algorithm is developed and evaluated in MATLAB / Simulink. A laboratory prototype utilizing a TMS320F28335 digital signal processor (DSP) is also implemented to validate effectiveness of the proposed algorithm. Both simulation and experimental results are presented. They show significant improvements in terms of total harmonic distortion (THD) and dynamic response when compared to a conventional SRF algorithm.

Key words: Active power filter, Current harmonics, DQ theory, Dynamic response, Multilevel inverter, Power quality

I. INTRODUCTION

Harmonics mitigations and reactive power compensations have received a tremendous amount of attention in power systems due in large part to the rapid growth of nonlinear loads such as power converters, variable speed drives and switched mode power supplies. The current harmonics and reactive power burden caused by these nonlinear loads degrade overall system efficiency and worsen power factor (PF) performances. Therefore, it is necessary to mitigate the harmonics levels of power systems.

The shunt active power filter (SAPF) [1], [2] is designed specifically for this purpose. In addition, it also provides reactive power compensation, which is meant for power factor correction. Previously, most SAPFs utilized a standard two-level inverter configuration in their design. However, multilevel inverters have recently proven to possess more advantages than conventional two-level inverters due to their superior ability in producing an output voltage with multiple levels [3], [4]. Generally, when an inverter produces higher voltage levels, it provides lower harmonics contents and power losses. However, in the context of APFs, the multilevel inverters employed are mostly limited to three-level inverters [5]-[7] due to complexity of controller design which involves a higher number of switching states and more severe voltage imbalances to the capacitors as the number of level increases. In a three-level neutral point diode clamped (NPC) inverter, the

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voltage across the split capacitors has to be maintained at half of the overall DC-Bus voltage.

The performance of a SAPF in power quality mitigation is strictly dependent on how quickly and how accurately its control strategies work. Specifically, the controller consists of three main algorithms, known as current harmonics extraction algorithm, current control (switching) algorithm, and voltage control algorithm. Among these algorithms, the current harmonics extraction algorithm is deemed to be the most important [7]-[9]. Being the very first algorithm to operate in the controller, accurate and efficient current harmonics extractions result in proper and fast reference current generation which further controls the SAPF to generate a desired injection current for harmonics mitigation.

Various studies on this particular algorithm have been reported in the literature such as Synchronous Reference Frame (SRF) [10]-[20], DQ Theory with Fourier (DQF) [21], Instantaneous Power (PQ) Theory [7], [9], [22], [23], Fast Fourier Transform (FFT) [24], Synchronous Detection (SD) [25], [26], wavelet-based approach [27], Artificial Neural Network (ANN) [28], [29] and many others. Among all of the existing algorithms, the SRF algorithm shows significant advantages over the others such as a simple design, increased speed and fewer calculations, which makes it more likely to be implemented practically.

In the context of the SRF based harmonics extraction algorithm, the ability to provide accurate and efficient fundamental component detection is the main factor that determines its performance. However, the latest trend in the SRF algorithm is relying on numerical filters especially a low pass filter (LPF) [11], [12], [14]-[20] to detect the desired fundamental component for reference current generation. The dependency on a sluggish numerical LPF which suffers from a serious time delay has significantly limited the detection performance. Moreover, the performance of numerical filters strictly depends on their tuned cutoff frequency, where the tuning is normally realized through a tedious approach. Furthermore, a good compromise between the cutoff frequency and the order of a filter is difficult to attain. However, this is required to ensure optimum performance.

In addition, the conventional SRF algorithm is still considered to possess unnecessary features which do not represent the basic requirements of current harmonics extraction, thereby increasing the computation burden of the algorithm.

Another weakness of the conventional SRF algorithm is related to the characteristic of its generated reference current. To date, the conventional SRF algorithm is still producing a non-sinusoidal reference current through a derivation of the extracted harmonic current, and forcing the switching signals meant for controlling the switching activities of the SAPF to be generated based on the direct current controlled (DCC) scheme [30]-[32].

Based on previous studies [1], [32], [33], the switching of the SAPF is reported to produce switching ripples in the source current, which undoubtedly degrades the THD performance of the mitigated source current. However, the DCC scheme, which operates based on a comparison of the measured injection current with its non-sinusoidal reference current counterpart [30]-[32], does not possess accurate information on the shape of the actual source current. Therefore, even if the source current is polluted by switching ripples, the DCC scheme is unable to mitigate the ripples due to its lack of exact information. As a result, the mitigated source current of the higher THD value is produced.

Although the indirect current controlled (ICC) scheme which operates based on a comparison of the actual source current with its sinusoidal reference current counterpart [7], [30]-[33] has been revealed to overcome the weakness of the DCC scheme, there is still no work on the SRF algorithm which has been conducted together with the ICC scheme. In fact, the working principle of the conventional SRF algorithm itself limits its application to the DCC scheme.

Compared to the DCC scheme, the ICC scheme that possess exact information on the characteristic of the actual source current is free from switching ripples problems [7], [32], [33] and thus providing superior harmonics mitigation performance. Moreover, the ICC scheme has a simpler control structure which involves a lower number of calculations [31], [34] and can be implemented with a lower number of sensors [30], [34]. As a result, it effectively reduces the system requirements for practical implementation.

On top of that, there are three key parameters that determine the performance of the SAPF. These parameters are known as the THD value, PF and dynamic response. Basically, the previous literature [10]-[12], [14], [19], [20] reported that the SAPF which is operated by utilizing the SRF algorithm successfully performed within the THD limit of 5 % set by IEEE Standard 519-2014 [35] with the PF being close to unity, thus proving the effectiveness of the SRF algorithm under steady state conditions. However, under dynamic state conditions where the fundamental component of a distorted signal fluctuates dynamically, the conventional SRF algorithm suffers from significant delays in tracking the required fundamental component. The achieved response time is within 0.05 s which corresponds to 2.5 cycles of a 50 Hz signal [15], [16]. However, further improvements can still be applied especially in reducing the computation burden and unnecessary delay resulting from an inefficient harmonics extraction algorithm which will surely improve the performance of the SAPF.

Therefore, this paper presents a simplified version of the SRF algorithm known as the simplified SRF (SSRF) algorithm that is suited for the operation of an ICC based SAPF in which the reference current is derived from the

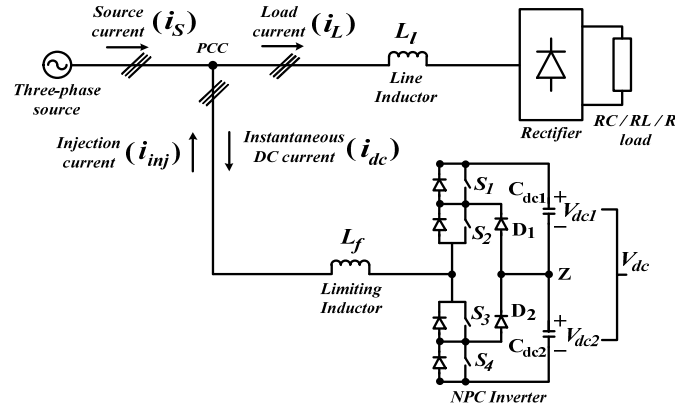


Fig. 1. The proposed SAPF connected at PCC.

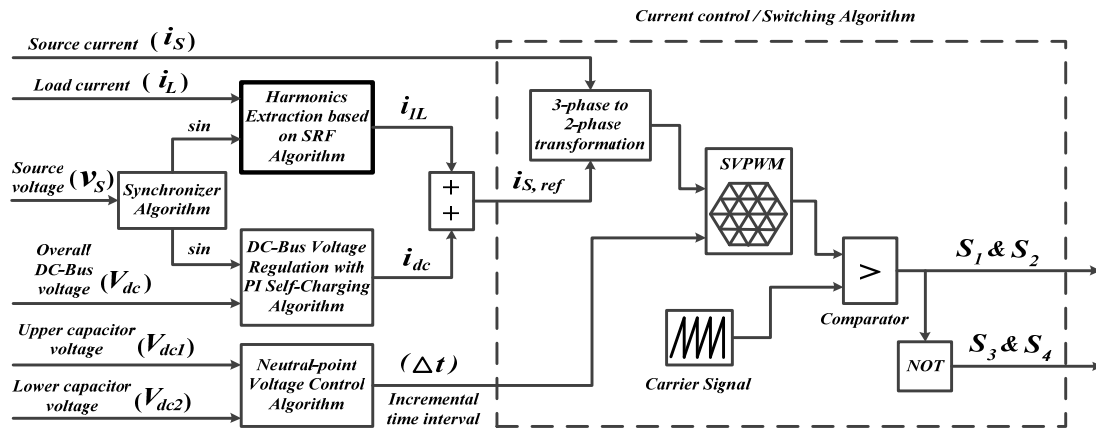


Fig. 2. The proposed SAPF's controller showing the harmonics extraction algorithm and all the other associated algorithms.

fundamental active current instead of the harmonic current.

The following points highlight the main areas of improvement in the proposed algorithm.

- 1) Fundamental component detection technique.
- 2) Algorithm complexity.
- 3) Characteristic of the output current.

The design concept and effectiveness of the proposed algorithm are verified using MATLAB / Simulink. For a performance comparison, the conventional SRF algorithm is developed, and both of the algorithms are tested under steady and dynamic state conditions. Moreover, a laboratory prototype is developed with the proposed algorithm downloaded to a digital signal processor (DSP) for further validation.

The remainder of this paper is organized as follows. In Section II, the proposed SAPF with control strategies is explained. Section III presents the details of the proposed current harmonics extraction algorithm with clear illustrations. In Section IV and Section V, simulation and experimental results are presented and discussed showing the effectiveness of the proposed algorithm with a comparison to the conventional algorithm. The paper ends with a brief conclusion in Section VI by summarizing the significant contributions of this work.

II. PROPOSED SAPF WITH CONTROL STRATEGIES

Fig. 1 shows the proposed three-phase three-level NPC inverter-based SAPF connected at the point of common coupling (PCC) between a three-phase source and a nonlinear load. The nonlinear load consists of a full bridge rectifier which is considered to be one of the worst sources of harmonics [17], [36] in electrical systems. Meanwhile, the SAPF's control strategies, as shown in Fig. 2, include a harmonics extraction algorithm, synchronizer algorithm, DC-Bus voltage regulation algorithm, neutral point voltage control algorithm, and current control (switching) algorithm.

In this paper, the main focus is on the harmonics extraction algorithm. The synchronizer algorithm is used to provide a sinusoidal referencing signal to the harmonics extraction algorithm and the DC-Bus voltage regulation algorithm governed by the self-charging technique [37]-[39]. Meanwhile, the split capacitors voltage balancing is achieved via the neutral point voltage control algorithm [40]-[42] which adjusts the incremental time interval Δt according to the detected instantaneous split capacitor voltages (V_{dc1} and V_{dc2}). Finally, the switching control is realized through the 25 kHz Space Vector PWM (SVPWM) [5], [40], [43]-[45] switching algorithm.

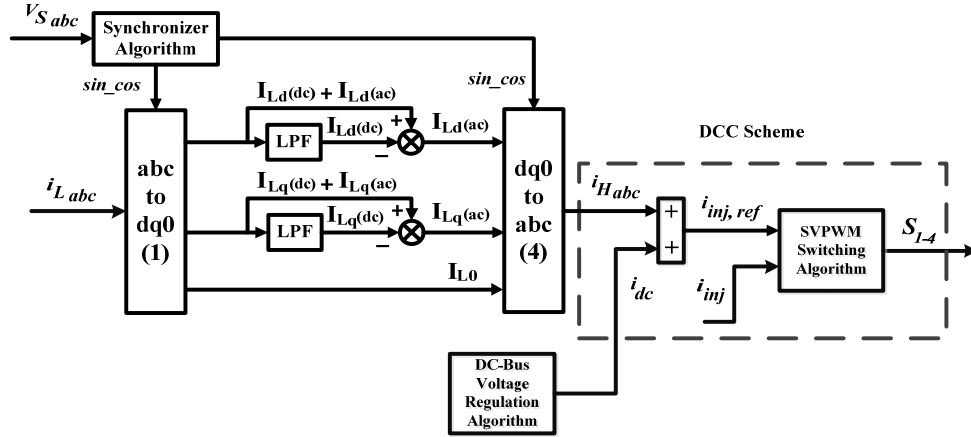


Fig. 3. The conventional SRF algorithm operating with DCC scheme.

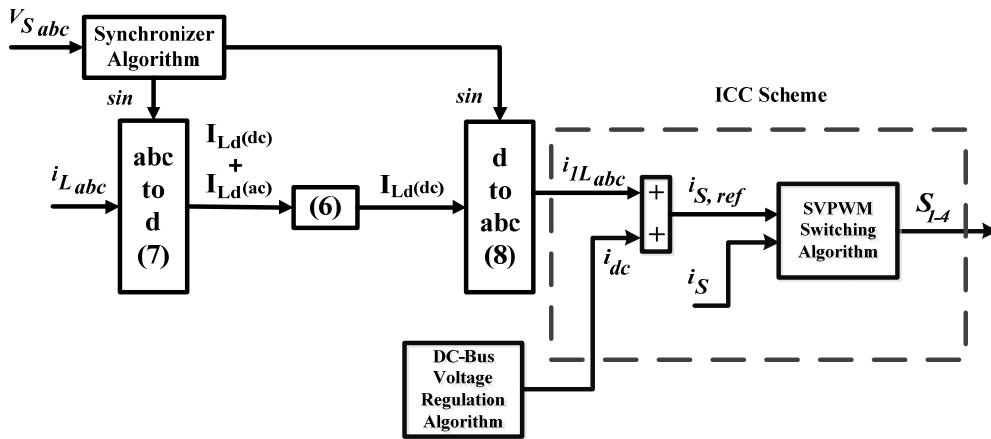


Fig. 4. The proposed simplified SRF (SSRF) algorithm operating with ICC scheme.

III. SIMPLIFIED SYNCHRONOUS REFERENCE FRAME (SSRF) ALGORITHM

In order to obtain a better understanding of the proposed harmonics extraction algorithm, and at the same time, to provide a proper comparison, the details of an existing algorithm known as the Synchronous Reference Frame (SRF) is first presented serving as a benchmark for improvement. Next, by referring to the SRF algorithm, the proposed algorithm known as the simplified Synchronous Reference Frame (SSRF) algorithm is elaborated. This is done to highlight the improvements made.

A. Synchronous Reference Frame (SRF) Algorithm

The overall process flow of harmonics extraction based on SRF is shown in Fig. 3. Basically, the extraction process is realized through a series of mathematical calculations of the three-phase load current which is conducted in the direct-quadrature-zero ($dq0$) frame. The measured load current in the three-phase abc frame is transformed into its corresponding $dq0$ frame by means of the Park-transformation, which is given as:

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

where ωt is the synchronization angle which represents the angular position of the dq synchronous reference frame.

Under the influence of nonlinear loads, the actual I_{Ld} and I_{Lq} components are polluted by harmonics resulting in the formation of a new current relationship given as:

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \end{bmatrix} = \begin{bmatrix} I_{Ld(dc)} + I_{Ld(ac)} \\ I_{Lq(dc)} + I_{Lq(ac)} \end{bmatrix} \quad (2)$$

where $I_{Ld(dc)}$ and $I_{Ld(ac)}$ represent the fundamental (dc) and distorted (ac) components of the load current in the d frame respectively. A similar relation holds for the load current in the q frame $I_{Lq(dc)}$ and $I_{Lq(ac)}$.

In the dq frame, the fundamental component of the load current appears as a dc signal, while the harmonics generated

by nonlinear loads, which are represented by the ac components, appear as ripples. For the purpose of harmonics extraction, both the $I_{Ld(ac)}$ and $I_{Lq(ac)}$ components are required for reference current generation. Generally, the ac components are obtained by detecting and removing the detected dc component from the actual load current in the dq frame. This approach can be represented as follows:

$$\begin{bmatrix} I_{Ld(ac)} \\ I_{Lq(ac)} \end{bmatrix} = \begin{bmatrix} I_{Ld} - I_{Ld(dc)} \\ I_{Lq} - I_{Lq(dc)} \end{bmatrix}. \quad (3)$$

Previously, the fundamental component $I_{Ld(dc)}$ detection is mostly accomplished by using a Butterworth-type tuned numerical LPF [11], [12], [17]-[19], [46].

However, the tuning of cutoff frequency and the selection of the filter's order are rather difficult tasks. Generally, a LPF with a lower cutoff frequency produces a smoother filtered signal (less ripples) but at the expense of a slow dynamic response. Meanwhile, a lower order LPF provides a fast dynamic response but some unwanted components remain (as ripples) in the filtered signal. On the other hand, a LPF with a higher cutoff frequency provides a fast dynamic response but poor filtering features (higher ripples). Meanwhile, a higher order LPF provides a better filtering features (less ripples) but it suffers from a longer time delay [10], [46]. Therefore, a good trade-off between the cutoff frequency and the order of the filter is crucial for optimum performance. However, this is a tough decision to make.

From the literature, in order to achieve a balance between the dynamic response and the filtering performance, the best cutoff frequency is reported to be in the range of 5 Hz to 25 Hz [10], [11], [17]. Meanwhile the order of the filter is restricted to second order [10]-[12], [17]-[19], [46] since higher order filters impose a great computational burden on the controller. However, a good compromise between the cutoff frequency and the filter's order does not provide a promising solution in achieving fast and smooth filtering performance.

Once the ac components ($I_{Ld(ac)}$ and $I_{Lq(ac)}$) are extracted, the inverse Park-transformation, as shown in equation (4), is performed to transform the ac components back into an actual three-phase harmonic current i_{Habc} , which is then used to derive the required reference injection current $i_{inj,ref}$.

$$\begin{bmatrix} i_{Ha} \\ i_{Hb} \\ i_{Hc} \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) & 1 \\ \sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \times \begin{bmatrix} I_{Ld(ac)} \\ I_{Lq(ac)} \\ I_{L0} \end{bmatrix}. \quad (4)$$

The reference injection current is derived by using equation (5), which is given as:

$$i_{inj,ref} = i_{Habc} + i_{dc} \quad (5)$$

where i_{dc} represents the instantaneous DC current, which results from the DC-Bus voltage regulation algorithm.

The non-sinusoidal $i_{inj,ref}$ forces the subsequent switching signals S_{1-4} to be generated based on the DCC scheme which operates by requiring a measurement of the actual injection current i_{inj} .

B. Proposed Improvements and Simplifications

Although the conventional SRF algorithm has been accepted as a simple and effective algorithm in current harmonics extraction, it still possesses weaknesses and unnecessary features which might degrade the performance of current harmonics extraction. Therefore, further improvements are implemented, resulting in the formation of the SSRF algorithm, as shown in Fig. 4. Three major improvements are proposed and highlighted as follows:

- 1) A mathematical based fundamental component identifier is proposed to replace the LPF in detecting the required fundamental dc component.
- 2) A reduction of the algorithm complexity through the removal of cosine and zero-sequence components.
- 3) A sinusoidal fundamental active current is generated as the output current instead of a non-sinusoidal harmonic current.

The first proposed improvement aims to overcome the drawbacks of the tuned numerical LPF, which include a tedious tuning workload and a significant delay in the dc component detection. Therefore, a mathematical based fundamental component identifier is proposed to replace the LPF. The proposed mathematical based fundamental component identifier is given as:

$$I_{L(dc)} = I_{L(average)} = \frac{1}{T} \int_0^T I_L dt \quad (6)$$

where $I_{L(average)}$ and T represents the average value and the period of the signal I_L .

The mathematical based fundamental component identifier eliminates the need for filtering. Thus, it removes the tuning workload as well as the possibility of inaccurate and inefficient dc component detection due to improper tuning.

Meanwhile, the second proposed improvement is aimed at reducing the algorithm complexity through the removal of the cosine component (q frame) and the zero-sequence component (0 frame) from the calculation.

The cosine component is removed according to the symmetrical theory in which the odd function is symmetric with respect to the origin. In order to suit the working principle of the ICC scheme, the proposed SSRF algorithm is designed to produce a sinusoidal reference current. The produced reference current is an odd function, which consists of only a sine component. As a result, it is unnecessary to include an even function such as a cosine component into the calculation process. In other words, a transformation using the sine component (d frame) alone is good enough to represent the odd function characteristic of the resulting sinusoidal reference current.

Further simplification can be achieved by removing the zero-sequence component from the calculation. The simplification is implemented based on the fact that the zero-sequence current does not exist in balanced three-phase systems [9], [47], [48]. The SAPF is mainly designed to operate in a balanced three-phase system in which the source voltage is assumed to be purely sinusoidal [6], [37], [39]. Thus, the zero-sequence component can be excluded from the calculation.

After removing the redundant cosine component and zero-sequence component from the calculation, the Park-transformation given in equation (1) is simplified as equation (7).

$$\begin{aligned} & [I_{Ld}] \\ &= \frac{2}{3} \left[\sin(\omega t) \quad \sin\left(\omega t - \frac{2\pi}{3}\right) \quad \sin\left(\omega t + \frac{2\pi}{3}\right) \right] \\ & \quad \times \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \end{aligned} \quad (7)$$

As a result of the applied simplification, the operation of the proposed SSRF algorithm has been changed. Previously, to achieve reference current generation, equation (3) is needed to extract the required ac components from the dq frame after detecting the dc component. However, in the proposed SSRF algorithm, the detected dc component is directly utilized to generate the reference current. Therefore, it eliminates the use of equation (3). Only the dc component of the d frame is involved in reference current generation. Therefore, the inverse Park-transformation given in equation (4) is simplified as equation (8) to transform the detected dc component back to an actual three-phase fundamental active current i_{1Labc} for further derivation.

$$\begin{bmatrix} i_{1La} \\ i_{1Lb} \\ i_{1Lc} \end{bmatrix} = \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} [I_{Ld(dc)}] \quad (8)$$

The third proposed improvement is aimed at further reducing the higher THD value of the source current resulting from the DCC based operation. Therefore, the operation of the conventional SRF algorithm is modified to suit the requirements of the ICC scheme. In order to realize this modification, the characteristic of the generated reference current needs to be changed.

Instead of deriving the reference current from i_{Habc} , the operation of the proposed SSRF algorithm makes it possible to derive the reference current from i_{1Labc} . As a result, a sinusoidal reference source current $i_{s,ref}$ can now be derived through equation (9).

$$i_{s,ref} = i_{1Labc} + i_{dc} \quad (9)$$

The sinusoidal $i_{s,ref}$ enables the subsequent switching signals S_{1-4} to be generated based on the measurement of i_s instead of i_{inj} . In other words, it changes the DCC based

TABLE I
PROPOSED PARAMETERS FOR SAPF

Parameter	Value
Voltage source	400 Vrms, 50 Hz
DC-Bus capacitor	3300 μ F (each)
DC-Bus reference voltage	880 V
Limiting inductor	5 mH
Switching frequency	25 kHz

operation to the ICC based operation. In contrast to the DCC based operation, the ICC based operation which possess exact information on the switching ripples, existing in the source current, eliminates any unnecessary problems caused by the switching activities of the SAPF [30]-[33].

IV. SIMULATION RESULTS

The proposed three-phase three-level NPC inverter-based SAPF utilizing the simplified SRF (SSRF) algorithm as the proposed harmonics extraction algorithm is tested and evaluated in MATLAB / Simulink. Initially, a study on the selection of the SAPF's output filter is carried out. After the selection of the best filter, further simulation work is conducted under both steady and dynamic state conditions involving three types of nonlinear loads. The first nonlinear load is constructed using a three-phase uncontrolled bridge rectifier feeding a 20 Ω resistor and a 2200 μ F capacitor connected in parallel (capacitive). The second nonlinear load is developed using a similar rectifier feeding a series connected 50 Ω resistor and a 50 mH inductor (inductive). The third nonlinear load is developed using a similar rectifier feeding a series connected 20 Ω resistor (resistive). Furthermore, the conventional SRF algorithm is tested for comparison purposes. The details of the proposed parameters used in the simulation work are summarized in Table I.

Under steady state condition, two key parameters are used for analyzing the performance of each harmonics extraction algorithm, which includes the percentage of ripple current and the THD value. The percentage of ripple current %RC is a newly proposed parameter and is defined as the ratio of the peak-to-peak fundamental component of the d frame load current $I_{Ld(dc,pp)}$ to the desired fundamental component of the d frame load current $I_{Ld(dc,desired)}$ as given below.

$$\%RC = \frac{I_{Ld(dc,pp)}}{I_{Ld(dc,desired)}} \times 100 \quad (10)$$

Meanwhile, under dynamic state condition, the performance parameters involved are undershoot, overshoot and response time. For this analysis, two dynamic state conditions are created by changing the nonlinear loads from capacitive to inductive and from inductive to resistive, respectively.

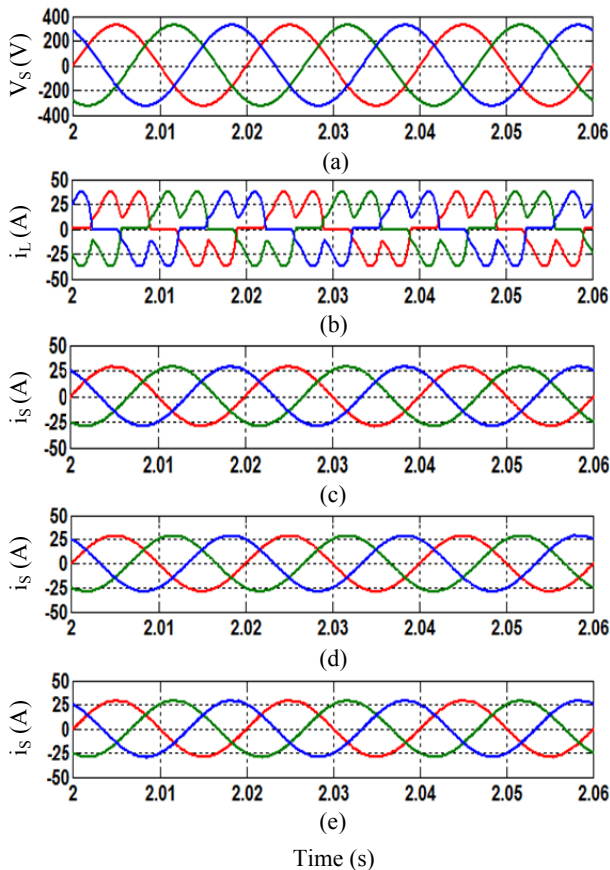


Fig. 5. Three-phase simulation waveforms for capacitive load which include (a) source voltage v_s , (b) load current i_L , and source current i_s resulted from SAPF utilizing SSRF algorithm with (c) L, (d) LC and (e) LCL output filters.

A. Selection of SAPF's Output Filter

As a result of high switching ripples generated during the mitigation process of APF, an output filter is usually applied as an interface between the APF and the utility grid to minimize the resulting switching ripples to ensure that high quality power is injected back into the grid at the PCC. Therefore, other than ensuring proper switching operation of the APF, it is also important to carefully select and design the output filter so that the designated APF can be operated at its best. For that purpose, complete understanding of the characteristics of the applied output filter must be acquired.

Various output filters have been reported in the literature such as L [49]-[54], LC [55] and LCL [56], [57] filters. They have been shown to be effective in APF applications. Among the available output filters, L filters are most commonly applied especially in SAPF applications due to their simple implementation features. In industrial applications, SAPFs utilizing L filters are widely used to mitigate the current harmonics present in the utility grid [49], [50]. Other SAPF applications which utilize L filters can also be found, even in aircraft [51], [52] and railway applications [53], [54].

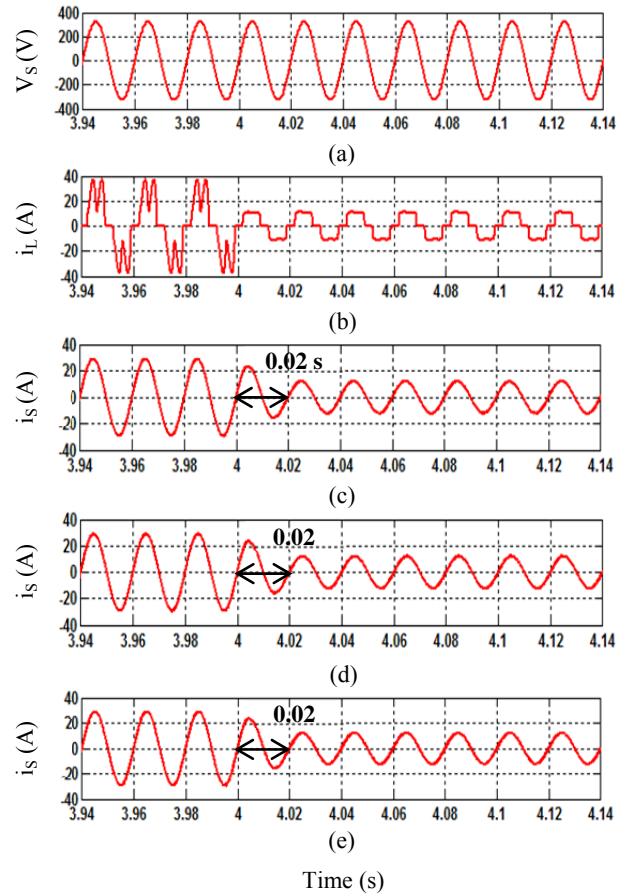


Fig. 6. Phase A simulation waveforms for dynamic state condition of capacitive to inductive which include (a) source voltage v_s , (b) load current i_L , and source current i_s resulted from SAPF utilizing SSRF algorithm with (c) L, (d) LC and (e) LCL output filters.

TABLE II
PARAMETERS OF OUTPUT FILTERS FOR SAPF

Type of Filter	Parameter	Value
L filter	Inductance	5 mH
LC filter	Inductance	5 mH
	Capacitance	30 μ F
LCL filter	Grid side Inductance	0.012 mH
	Capacitance	20 μ F
	Damping Resistor	0.1 Ω
	SAPF side Inductance	3 mH

Nevertheless, the selection and design of an output filter for SAPF requires special care since its performance differs depending on its designated application. Hence, the characteristics and performances of the selected output filter must be thoroughly studied so that the best output filter can be designed to suit its designated application.

Owing to that reason, an initial study is conducted in this research to investigate the influences of different SAPF's

TABLE III
THDs OF MITIGATED SOURCE CURRENT (CAPACITIVE LOAD) FOR DIFFERENT SAPF'S OUTPUT FILTERS

Harmonics Extraction Algorithm	Total Harmonic Distortion, THD (%)								
	Phase A			Phase B			Phase C		
	L	LC	LCL	L	LC	LCL	L	LC	LCL
Before Connecting SAPF									
N/A	43.03			43.03			43.03		
After Connecting SAPF									
SSRF	1.10	1.13	1.15	1.09	1.12	1.15	1.08	1.12	1.14

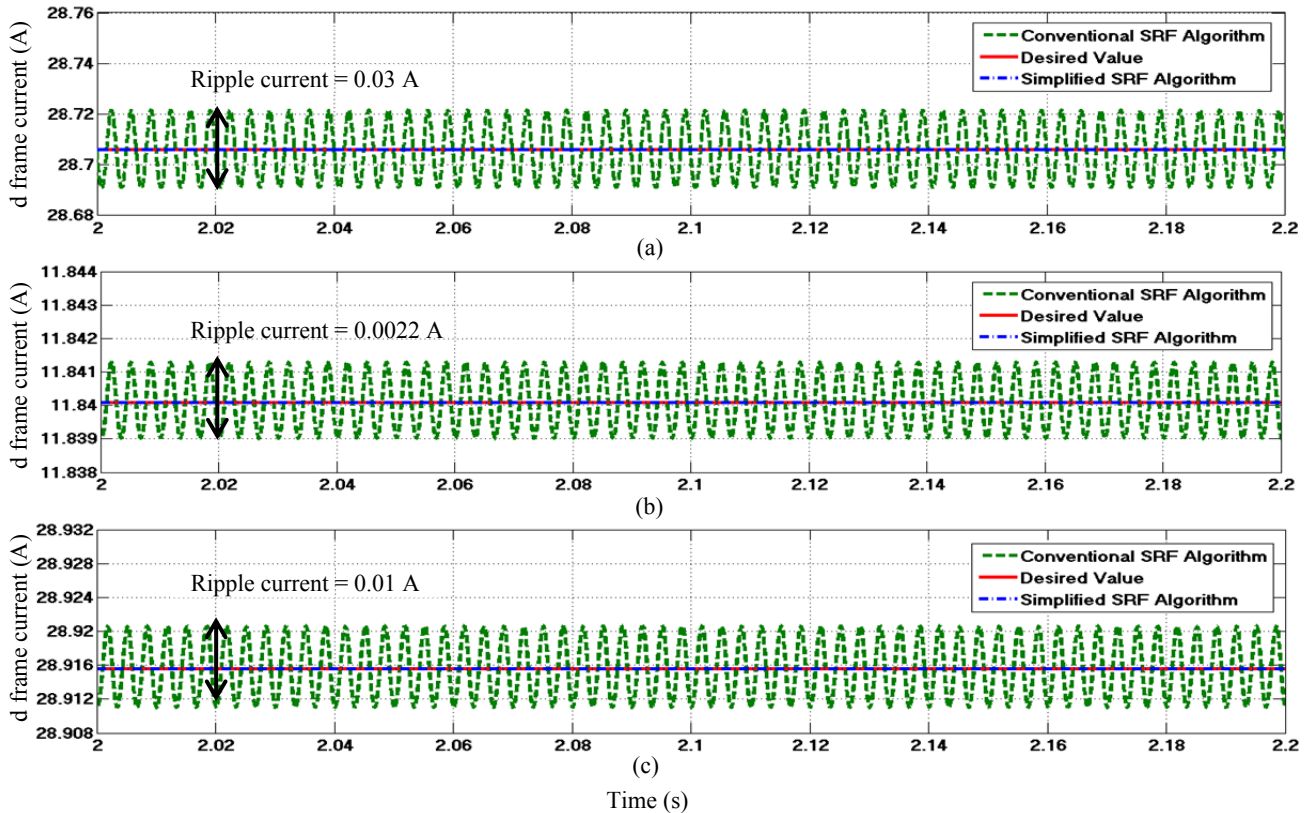


Fig. 7. Fundamental component of load current in d frame $I_{ld(dc)}$, detected by each harmonics extraction algorithm for (a) capacitive, (b) inductive and (c) resistive loads.

output filters in terms of harmonics extraction performances of the proposed SSRF algorithm, based on the mitigation performances of SAPF. Three types of output filters are considered in this study including L, LC and LCL filters. Table II summarizes the parameters for all of the considered output filters.

The study is conducted under both steady (capacitive load) and dynamic state (capacitive to inductive) conditions. Under steady state condition, performance of the proposed SSRF algorithm is determined based on the THD value. Meanwhile, under dynamic state condition, its performance is determined based on the response time.

Fig. 5 shows three-phase simulation waveforms of the source voltage v_s , load current i_L , and source current i_s resulted from the SAPF utilizing the proposed SSRF algorithm

with different output filters for a capacitive load. Meanwhile, the resulted THD values of the source current i_s mitigated by the SAPF are summarized in Table III. On the other hand, the dynamic responses demonstrated by the SAPF are shown in Fig. 6.

The findings show that the used of different output filters influence the mitigation performance of the SAPF in term of THD performances. All of the output filters provide outstanding ripples filtering performance by achieving low THD values for the mitigated source current i_s . However, the SAPF with a L filter provides the best filtering performance by achieving the lowest THD value. In addition, it is clear that the dynamic performances of the SAPF are not affected by the choice of the output filters.

Therefore, by taking into consideration the performance

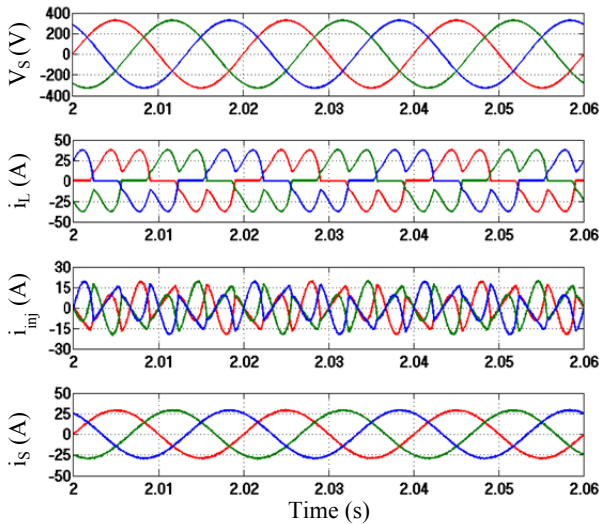


Fig. 8. Three-phase simulation waveforms of source voltage v_s , load current i_L , injection current i_{inj} , and source current i_s resulted from the Simplified SRF algorithm for capacitive load.

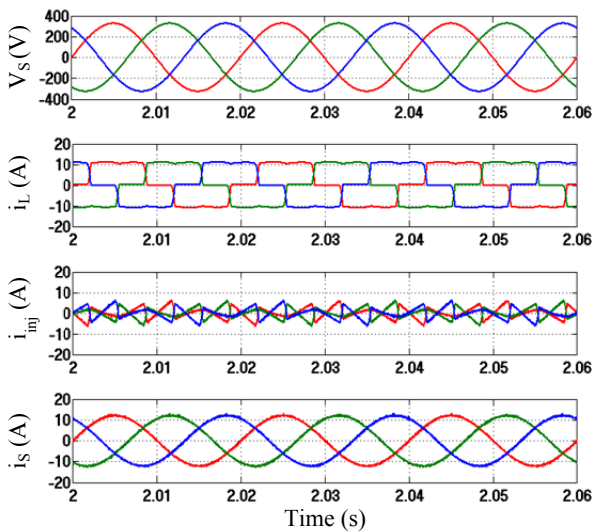


Fig. 9. Three-phase simulation waveforms of source voltage v_s , load current i_L , injection current i_{inj} , and source current i_s resulted from the Simplified SRF algorithm for inductive load.

and the required design efforts of each selected output filter, the L filter which provides the best performances and requires the least design efforts, is selected and applied throughout this research work.

B. Steady State Condition

The performance of each harmonics extraction algorithm in detecting the desired fundamental component of the load current in the d frame $I_{Ld(dc)}$ for capacitive, inductive and resistive loads are shown in Fig. 7.

Both of the algorithms detect the fundamental component well but they differ in term percentage of ripple current. The proposed SSRF algorithm provides accurate fundamental

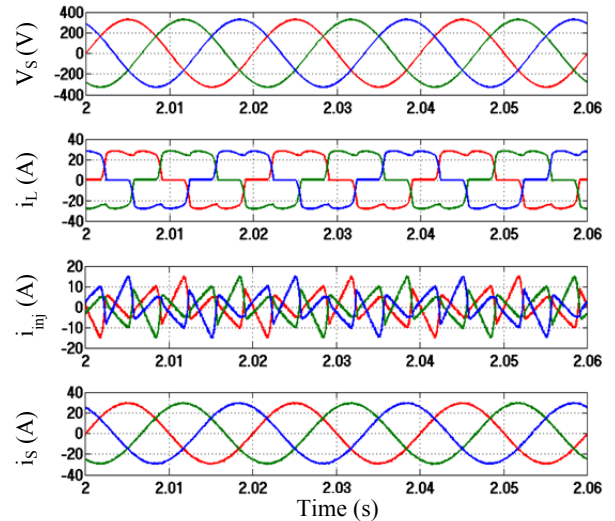


Fig. 10. Three-phase simulation waveforms of source voltage v_s , load current i_L , injection current i_{inj} , and source current i_s resulted from the Simplified SRF algorithm for resistive load.

component detection without any ripple for all nonlinear loads. In contrast, the conventional SRF algorithm produces fundamental component with ripple currents of 0.03 A (% $RC = 0.104\%$), 0.0022 A (% $RC = 0.019\%$), and 0.01 A (% $RC = 0.034\%$) for the capacitive, inductive and resistive loads respectively. The findings prove that the proposed mathematical based fundamental component identifier is able to detect the desired fundamental component of the load current with a higher accuracy as compared to the tuned numerical LPF.

On the other hand, Figs. 8, 9 and 10 show three-phase waveforms of the source voltage v_s , load current i_L , injection current i_{inj} , and source current i_s resulting from the proposed SSRF algorithm for capacitive, inductive and resistive loads, respectively. Meanwhile, the THD values of the source current i_s mitigated by the SAPF utilizing each of the harmonics extraction algorithms are summarized in Table IV.

Both of the algorithms successfully control the SAPF to remove the generated current harmonics resulting in THD values of below 5% which complies with the limit set by IEEE Standard 519-2014 [35]. However, the proposed SSRF algorithm shows superior performance in reducing the switching ripples in the source current i_s by achieving a lower THD value for all of the nonlinear loads as compared to the conventional SRF algorithm. Furthermore, the mitigated source current i_s seems to work in phase with the source voltage v_s for all nonlinear loads, which leads to an almost unity power factor.

C. Dynamic State Condition

The dynamic behaviour of each of the harmonics extraction algorithms in detecting the desired fundamental component of load current in the d frame $I_{Ld(dc)}$ for dynamic state

conditions of capacitive to inductive and inductive to resistive are shown in Fig. 11. For both dynamic state conditions, the proposed SSRF algorithm shows the best performance with a response time of 0.02 s, and no undershoot or overshoot. Meanwhile, the conventional SRF algorithm performs poorly with a response time of 0.12 s, and a high undershoot and overshoot of 0.6 A. These findings prove that in terms of fundamental component detection, the proposed algorithm shows superior dynamic performance by achieving a response time that is 6 times faster than that of the conventional algorithm.

On the other hand, Figs. 12 and 13 show the dynamic behaviour of each of the harmonics extraction algorithms in current harmonics mitigation for dynamic state conditions of capacitive to inductive and inductive to resistive, respectively. For both dynamic state conditions, the proposed SSRF shows the best performance with a response time of 0.02 s. Meanwhile, the conventional SRF algorithm performs poorly with a response time of 0.04 s. Therefore, in term of current harmonics mitigation, SAPF with the proposed algorithm shows superior dynamic performance by achieving a response time that is 2 times faster than that of the conventional algorithm.

In order to further verify effectiveness of the proposed SAPF, performance evaluations in terms of DC-Bus voltage regulation and neutral point voltage deviation control are also conducted. Figs. 14 and 15 show the simulation results obtained for the overall DC-Bus voltage V_{dc} , the split capacitor voltages (V_{dc1} and V_{dc2}), and the neutral point voltage deviation ($V_{dc1} - V_{dc2}$) for dynamic state conditions of capacitive to inductive and inductive to resistive, respectively.

The results show that all of the DC-Bus voltages (V_{dc} , V_{dc1} and V_{dc2}) of the proposed SAPF are properly controlled at desired value with a response time of 0.3 s for both of the dynamic state conditions. Moreover, the voltages across both of the split capacitors (V_{dc1} and V_{dc2}) are successfully maintained as half of the overall DC-Bus voltage V_{dc} with a minimal neutral point voltage deviation. These findings prove the effectiveness of the DC-Bus voltage regulation algorithm and neutral point voltage control algorithm applied in the proposed SAPF.

From all of the simulation results obtained in both steady and dynamic state conditions, it is clear that the proposed SSRF algorithm shows the best performance with high accuracy, low THD, no overshoot, no undershoot and fast response time. On the other hand, the conventional SRF algorithm, which has widely been reported in the literature, performs well under steady state conditions. However, under dynamic state conditions, it is unable to track and response fast enough to rapid change of nonlinear loads.

V. EXPERIMENTAL VALIDATION

A laboratory prototype is developed to validate practically performance of the proposed SSRF algorithm. The experimental setup for the proposed three-phase three-level NPC inverter-based SAPF system is constructed as shown in Fig. 16. For experimental testing, the supply voltage source is set at 100 Vrms, which is supplied from a programmable AC source. Meanwhile, the desired overall reference voltage of the DC-Bus is set at 220 V.

Furthermore, a TMS320F28335 digital signal processor (DSP) board is configured and programmed to perform all control algorithms of the SAPF and to generate the desired switching signals for the NPC inverter. Similar to the simulation work, the laboratory prototype is also tested under both steady and dynamic state conditions. Under steady state conditions, the proposed algorithm is evaluated in terms of its THD performance. Meanwhile, under dynamic state conditions, the proposed algorithm is evaluated in terms of its dynamic response towards rapid changes of nonlinear loads.

Figs. 17, 18 and 19 show experimental results (Phase A) of the SAPF utilizing the proposed SSRF algorithm which covers the source voltage v_s , load current i_L , injection current i_{inj} , and source current i_s , for capacitive, inductive and resistive loads, respectively. Meanwhile, the THD values of source current i_s mitigated by the SAPF utilizing each of the harmonics extraction algorithms obtained from the experimental work are summarized in Table V. On the other hand, Figs. 20 and 21 show the dynamic behaviour of the SAPF utilizing each of the harmonics extraction algorithms in current harmonics mitigation for dynamic state conditions of

TABLE IV
THDS OF MITIGATED SOURCE CURRENT RESULTED FROM EACH HARMONICS EXTRACTION ALGORITHM FOR CAPACITIVE, INDUCTIVE AND RESISTIVE NONLINEAR LOADS (SIMULATION RESULTS).

Harmonics Extraction Algorithm	Total Harmonic Distortion, THD (%)								
	Phase A			Phase B			Phase C		
	Capacitive	Inductive	Resistive	Capacitive	Inductive	Resistive	Capacitive	Inductive	Resistive
Before Connecting SAPF									
N/A	43.03	27.43	26.64	43.03	27.43	26.64	43.03	27.43	26.64
After Connecting SAPF									
Conventional SRF	1.27	1.63	1.28	1.26	1.65	1.32	1.28	1.64	1.30
SSRF	1.10	1.44	1.08	1.09	1.45	1.03	1.08	1.44	1.06

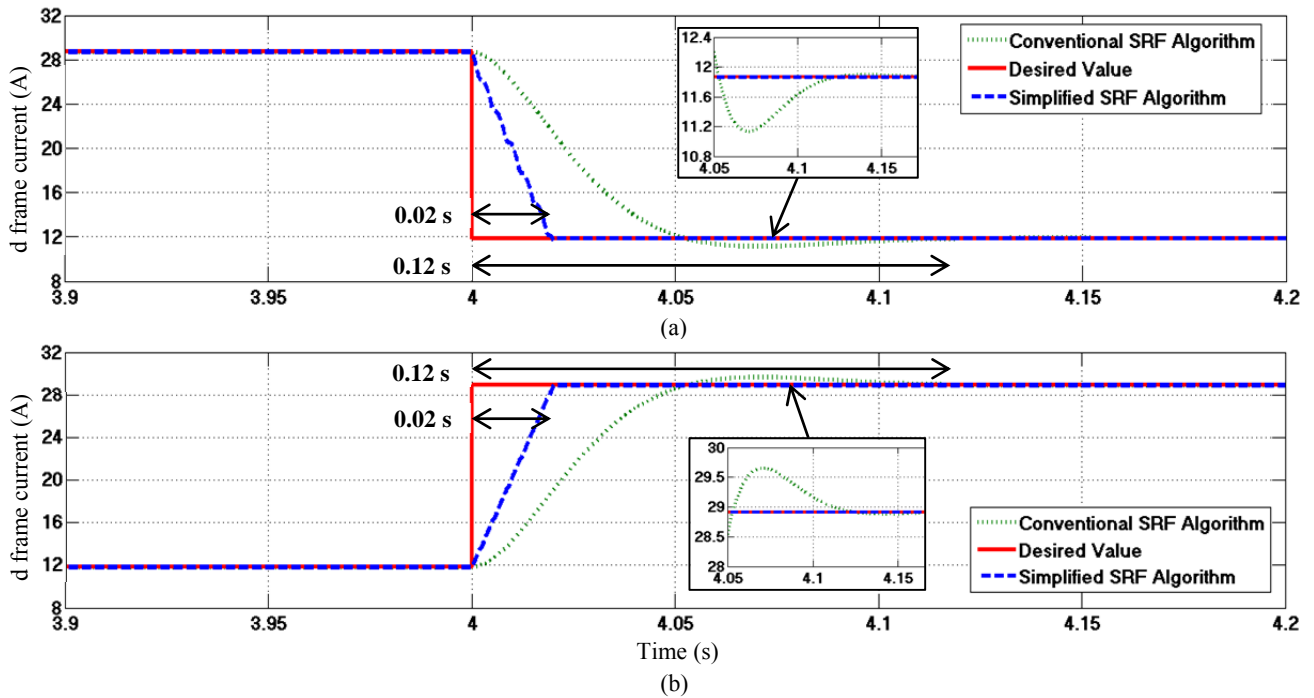


Fig. 11. Fundamental component of load current in d frame $I_{Ld(dc)}$, detected by each harmonics extraction algorithm for dynamic state conditions of (a) capacitive to inductive, and (b) inductive to resistive.

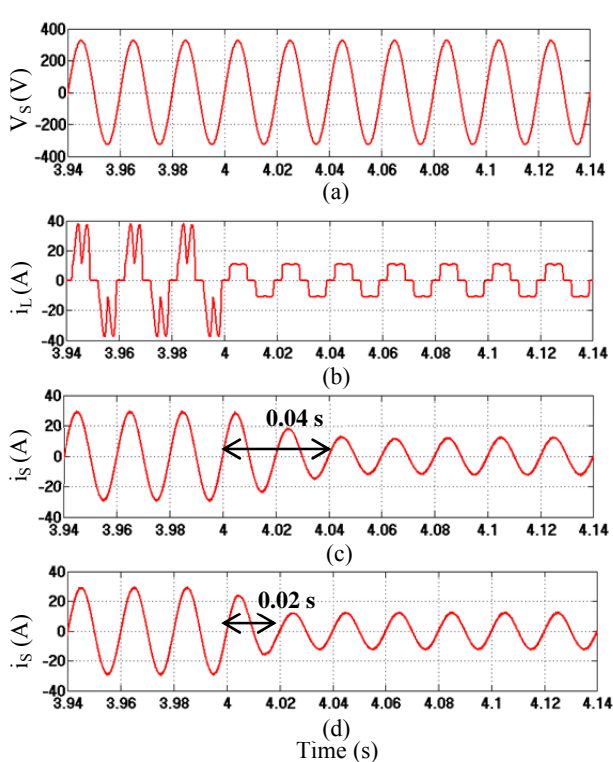


Fig. 12. Phase A simulation waveforms for dynamic state condition of capacitive to inductive which include (a) source voltage v_s , (b) load current i_L , (c) source current i_s resulted from conventional SRF algorithm, and (d) source current i_s resulted from simplified SRF algorithm.

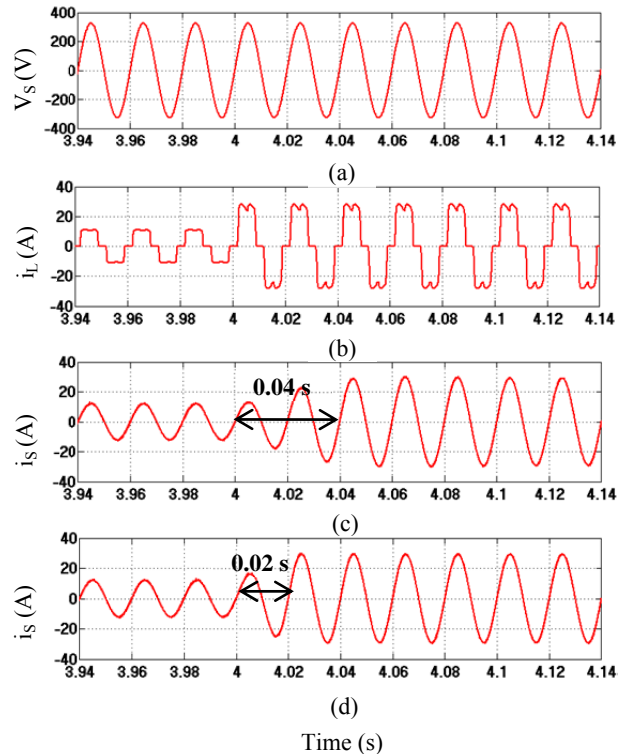


Fig. 13. Phase A simulation waveforms for dynamic state condition of inductive to resistive which include (a) source voltage v_s , (b) load current i_L , (c) source current i_s resulted from conventional SRF algorithm, and (d) source current i_s resulted from simplified SRF algorithm.

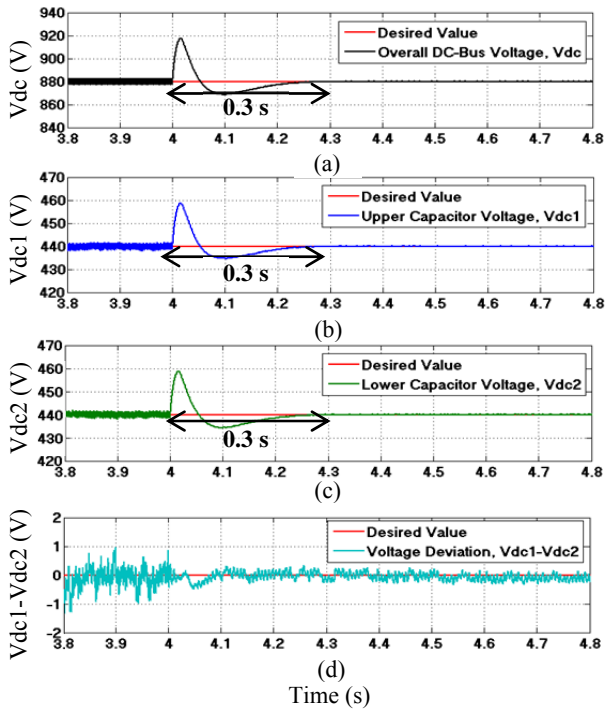


Fig. 14. Simulation waveforms of (a) overall DC-Bus voltage V_{dc} , (b) upper capacitor voltage V_{dc1} , (c) lower capacitor voltage V_{dc2} , and (d) neutral point voltage deviation ($V_{dc1} - V_{dc2}$), for dynamic state condition of capacitive to inductive.

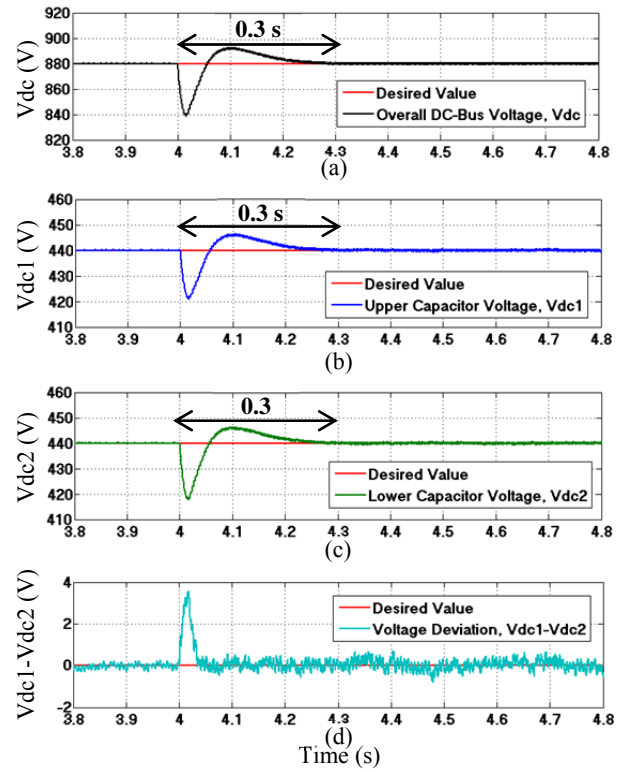


Fig. 15. Simulation waveforms of (a) overall DC-Bus voltage V_{dc} , (b) upper capacitor voltage V_{dc1} , (c) lower capacitor voltage V_{dc2} , and (d) neutral point voltage deviation ($V_{dc1} - V_{dc2}$), for dynamic state condition of inductive to resistive.

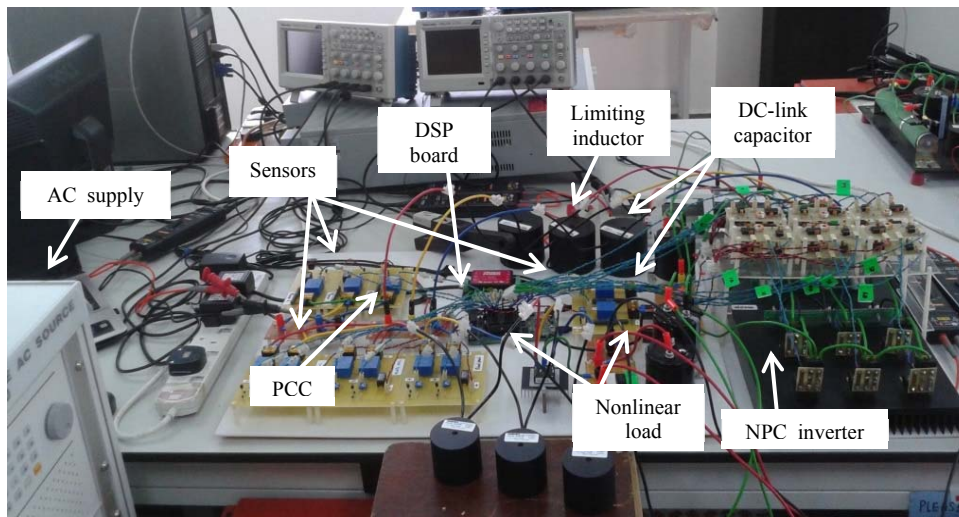


Fig. 16. Experimental setup for the proposed SAPF.

capacitive to inductive and inductive to resistive, respectively.

Both of the algorithms successfully control the SAPF to remove the generated current harmonics, resulting in a THD value of below 5%. However, the THD value recorded for the proposed SSRF algorithm is in a better range, within 2.50% to 3.33%, as compared to the conventional SRF algorithm which performs within the range of 3.69% to 4.33%. Most

importantly, by using the proposed SSRF algorithm, the response time of around two cycles (0.04 s to 0.045 s) in current harmonics mitigation, which was previously achieved by using the conventional SRF algorithm is now significantly reduced to around one cycle (0.02 s to 0.025 s).

Fig. 22 shows experimental results obtained for the overall DC-Bus voltage V_{dc} , and the split capacitor voltages (V_{dc1}

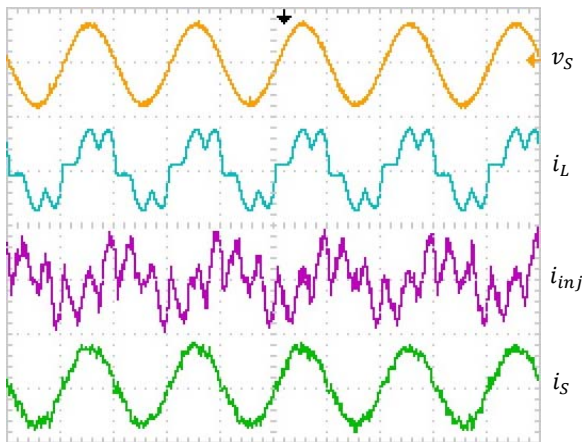


Fig. 17. Experimental result (Phase A) of source voltage v_s (100 V/div), load current i_L (10 A/div), injection current i_{inj} (5 A/div), and source current i_s (10 A/div) resulted from the simplified SRF algorithm for capacitive load.

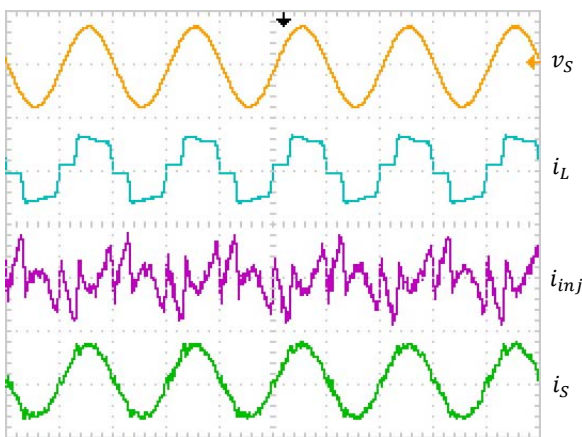


Fig. 18. Experimental result (Phase A) of source voltage v_s (100 V/div), load current i_L (5 A/div), injection current i_{inj} (2 A/div), and source current i_s (5 A/div) resulted from the simplified SRF algorithm for inductive load.

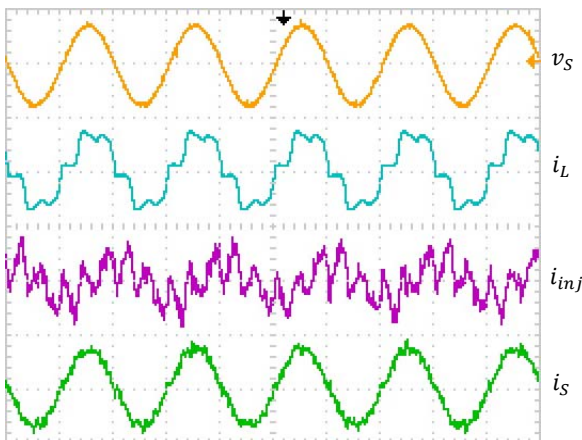
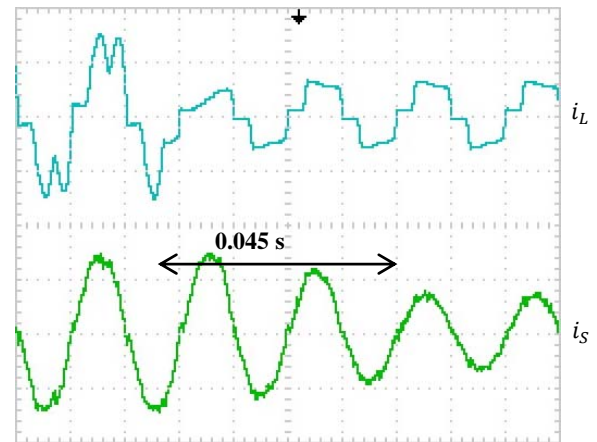
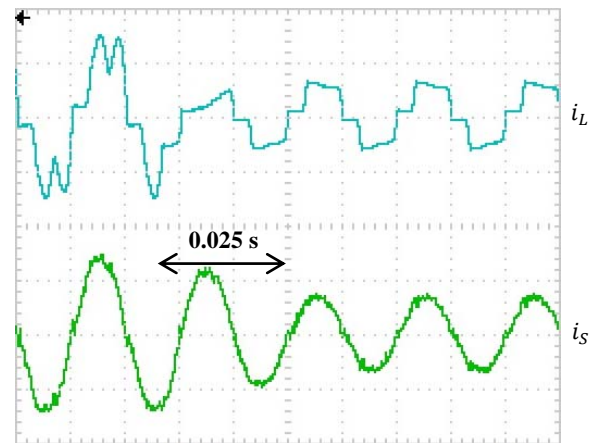


Fig. 19. Experimental result (Phase A) of source voltage v_s (100 V/div), load current i_L (10 A/div), injection current i_{inj} (5 A/div), and source current i_s (10 A/div) resulted from the simplified SRF algorithm for resistive load.



(a)



(b)

Fig. 20. Experimental result (Phase A) for dynamic state condition of capacitive to inductive for load current i_L (5 A/div), and source current i_s (5 A/div) resulted from (a) conventional SRF algorithm, and (b) simplified SRF algorithm.

and V_{dc2}), for dynamic state conditions of capacitive to inductive and inductive to resistive. The findings show that all of the DC-Bus voltages (V_{dc} , V_{dc1} and V_{dc2}) of the proposed SAPF are properly controlled at desired value with a response time of 0.4 s for both of the dynamic state conditions. Moreover, the voltages across both of the split capacitors (V_{dc1} and V_{dc2}) are successfully maintained as half of the overall DC-Bus voltage V_{dc} with minimal deviation.

From all of the simulation and experimental results obtained in both steady and dynamic state conditions, the improvements achieved by the proposed SSRF algorithm have revealed the significant roles of applying a mathematical based fundamental component identifier, simplifying the algorithm complexity, and modifying the characteristic of the generated reference current to suit the ICC based operation. The implementation of the proposed algorithm has significantly improved the performances of the proposed SAPF. In addition, the successful control of all of the DC-Bus voltages at their respective desired values together with the

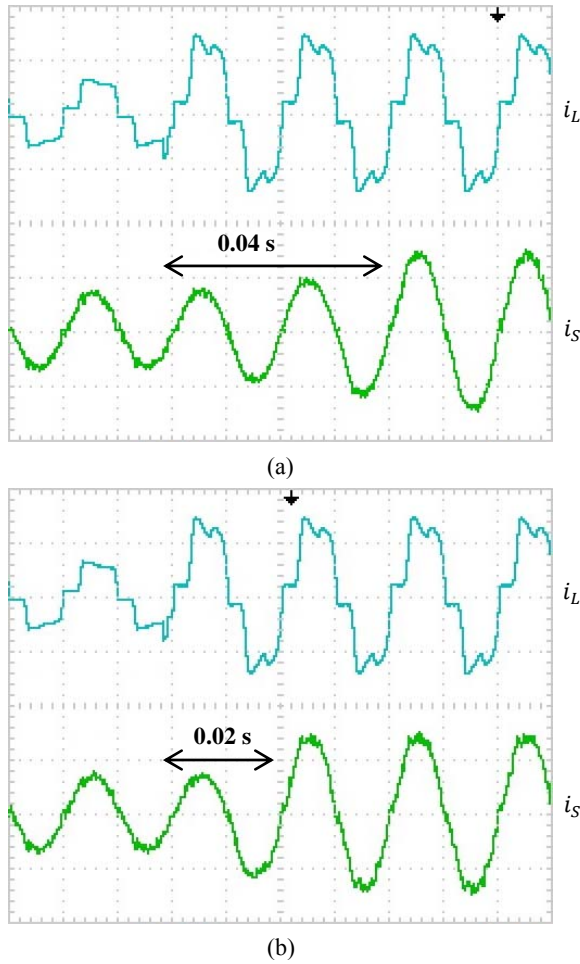


Fig. 21. Experimental result (Phase A) for dynamic state condition of inductive to resistive for load current i_L (5 A/div), and source current i_S (5 A/div) resulted from (a) conventional SRF algorithm, and (b) simplified SRF algorithm.

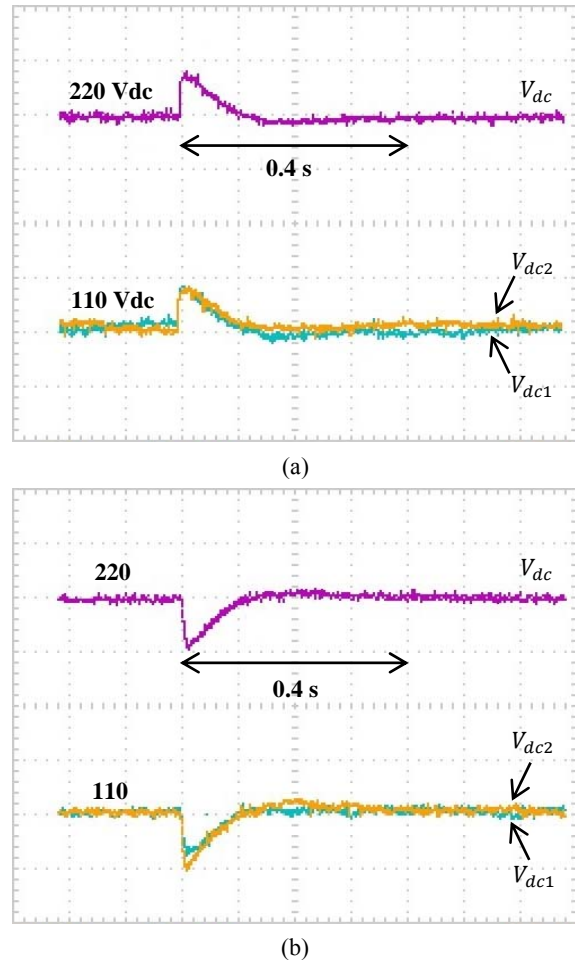


Fig. 22. Experimental result of overall DC-Bus voltage V_{dc} (40 V/div), and split capacitor voltages V_{dc1} and V_{dc2} (20 V/div) for dynamic state conditions of (a) capacitive to inductive, and (b) inductive to resistive.

TABLE V

THDs OF MITIGATED SOURCE CURRENT RESULTED FROM EACH HARMONICS EXTRACTION ALGORITHM FOR CAPACITIVE, INDUCTIVE AND RESISTIVE NONLINEAR LOADS (EXPERIMENTAL RESULTS).

Harmonics Extraction Algorithm	Total Harmonic Distortion, THD (%)								
	Phase A			Phase B			Phase C		
	Capacitive	Inductive	Resistive	Capacitive	Inductive	Resistive	Capacitive	Inductive	Resistive
Before Connecting SAPF									
N/A	32.14	24.62	24.32	32.18	24.65	24.30	32.11	24.66	24.31
After Connecting SAPF									
Conventional SRF	4.33	3.98	3.69	4.31	3.93	3.76	4.31	3.86	3.70
SSRF	3.33	3.04	2.54	3.28	2.99	2.50	3.30	2.93	2.56

minimal neutral point voltage deviation has further verified the design concept and the effectiveness of the proposed SAPF in current harmonics mitigation.

VI. CONCLUSION

This paper has presented a new simplified SRF algorithm which is applicable in ICC based SAPFs. The following points

summarize the major contributions of this work.

- 1) The development of a mathematical based fundamental component identifier to replace a sluggish numerical LPF. This provides efficient fundamental component detection, and at the same time, eliminates the needs for a tedious tuning workload.
- 2) The reduction of algorithm complexity through the

removal of the cosine component and the zero-sequence component, which reduces the computational burden for practical implementations.

- 3) The fundamental active current is generated instead of a harmonic current, which grants the ability to generate a sinusoidal reference current. As a result, the SRF algorithm can now be implemented in ICC based SAPFs which was previously only applicable in DCC based SAPFs. Consequently, this technique indirectly improves the THD value of the mitigated source current through the elimination of switching ripples.

A comprehensive analysis in both steady and dynamic state conditions is conducted to evaluate performance of the proposed algorithm. Moreover, a comparative evaluation with the conventional algorithm is also conducted to verify the improvements achieved by the proposed algorithm. Under steady state conditions, the simulation work shows that the proposed algorithm is not only able to control the SAPF in mitigating the current harmonics with a lower THD value for all of the nonlinear loads, but is also able to eliminate the ripples remained in the detected fundamental component. On the other hand, significant improvements can be observed during dynamic state conditions where the proposed algorithm has successfully performed with a fast response time and no undershoot or no overshoot.

Furthermore, the hardware test results have confirmed the effectiveness of proposed algorithm in both steady and dynamic state conditions as conducted in the simulation work. A low THD value and a fast response time clearly show the advantages of the proposed simplified SRF algorithm over the conventional SRF algorithm especially in dealing with dynamic state conditions.

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