JPE 16-6-8

http://dx.doi.org/10.6113/JPE.2016.16.6.2067
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Modified Charge Balancing Scheme for Cascaded H-Bridge Multilevel Inverter

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Abstract

Cascaded H-bridge multilevel inverters are currently used because it enables the integration of various sources, such as batteries, ultracapacitors, photovoltaic array and fuel cells in a single system. Conventional modulation schemes for multilevel inverters have concentrated mainly on the generation of a low harmonic output voltage, which results in less effective utilization of connected sources. Less effective utilization leads to a difference in the charging/discharging of sources, causing unsteady voltages over a long period of operation and a reduction in the lifetime of the sources. Hence, a charge balance control scheme has to be incorporated along with the modulation scheme to overcome these issues. In this paper, a new approach for charge balancing in symmetric cascaded H-bridge multilevel inverter that enables almost 100% charge balancing of sources is presented. The proposed method achieves charge balancing without any additional stages or complex circuit or considerable computational requirement. The validity of the proposed method is verified through simulation and experiments.

Key words: Cascaded H-bridge, Charge balancing, Modulation scheme, Multilevel inverter

I. INTRODUCTION

In recent years, the demand for medium-power, high-voltage power units have been increasing in industries on account of its economic prospects. This scenario has resulted in considerable attention being given to multilevel inverter (MLI) topologies as an alternative. The MLIs utilize a number of power semiconductor switches and voltage sources to generate near sinusoidal output waveform with low voltage stress, harmonic distortion, common mode voltage and EMI issues [1]. Classical multilevel inverter topologies include cascaded H-bridge (CHB), diode-clamped (DC) and capacitor-clamped (CC) MLIs [2]-[4]. Over the past few years, variants of classical topologies and numerous new and hybrid MLI topologies have been introduced [5], [6]. Proficiency and maturity of technological developments in this area has led to a wide range of industrial applications, such as motor drives, power quality improvement, STATCOM, HVDC, electric vehicles, etc. [7], [8].

CHB-MLI topologies are also suitable for systems with isolated DC supplies, as well as those with different characteristics, such as batteries, ultracapacitors, photovoltaic array, fuel cells, etc. that enable the use of MLIs in renewable energy applications [9], [10].

In the case of CHB-MLI, the output voltage level has to be increased to achieve near sinusoidal output waveform and improve the harmonic profile. Increasing the level of output voltage requires utilization of a number of isolated DC voltage sources to attain different voltage levels. In a conventional modulation scheme, some sources are connected periodically to achieve certain output voltage levels. In such cases, charging or discharging currents and terminal voltages will differ for each source, resulting in unbalanced power drawn from DC sources. In effect, load sharing between the sources is uneven, resulting in a difference in state-of-charge (SOC) and voltage levels in DC sources over a long period of operation [11]. The last few decades have witnessed vital advancements in modulation and control strategies for MLIs; however, these developments have concentrated mainly on optimising parameters, such as switching frequency, harmonic distortion, switching loss, etc. [12], [13]. Hence, to ensure proper power management of the voltage sources, an effective charge balance control scheme has to be incorporated along with the modulation scheme [14], [15].

A charge balance control scheme for cascade multilevel converter was presented for hybrid electric vehicle

Manuscript received Apr. 17, 2016; accepted Jul. 9, 2016
Recommended for publication by Associate Editor Liqiang Yuan.
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application [16], [17], where a gate-signal swapping scheme was employed to swap duty-cycle among various levels that resulted in the equal charge and/or discharge of all batteries used. This duty-cycle swapping circuit to establish the gate pulse swapping is an additional realisation requirement. Another method for voltage balance control for CHB-MLI based on two auxiliary controllers has been proposed [18]. In this auxiliary controller method, output voltage reference signals are obtained from the DC voltage balance controller, which is realised by auxiliary voltage signal and shift signal controllers and achieves charge balancing. The drawback of this method is that the generation of auxiliary signals and output voltage reference signals involves matrix multiplication, which in turn involves increased implementation effort and computational requirement.

Another modulation control scheme involving a charge balancing technique has been introduced based on altered aggregated signal in a new reduced number of count MLI topology [19], [20]. The advantage of this method is its simplicity and the realisation is completely in the modulation stage without additional computational requirement. However, it has the drawback of increased level comparisons and expanded switching table, leading to added implementation effort. In this paper, a new modulation method is proposed, where the added implementation effort is addressed effectively by incorporating the gate-signal swapping method along with altered aggregated signal method, which in turn provides an improved scheme with simple implementation effort, less computational requirement, and minimum fundamental cycle requirement for charge balancing.

The paper is organized as follows. A brief discussion on CHB-MLI topology and modulation scheme is given in Section 2, and detailed explanations of charge balance control schemes are included in Section 3. The simulation and experimental results are presented in Section 4 and the effectiveness and improvement of the proposed method are discussed in Section 5. The conclusions are given in Section 6.

II. CHB-MLI Topology and Modulation Scheme

A. Topology

The CHB-MLI topology consists of a series connected H-bridges. This unique structure allows the generation of the desired output voltage from a number of isolated DC sources. The general structure of the CHB-MLI topology is shown in Fig. 1. In the figure, the switches are indicated as 'S_{np}', where 'n' denotes the corresponding H-bridge and 'p' indicates the switch positions (p=1, 2, 3, 4) in the H-bridges. The relation between output voltage level (N) and number of bridges (H) and maximum output voltage ($V_{ao,max}$) are given as

$$N = 2H + 1;\ V_{dcn} = V_{dc} \quad for \quad n = 1, 2, ...H \tag{1}$$

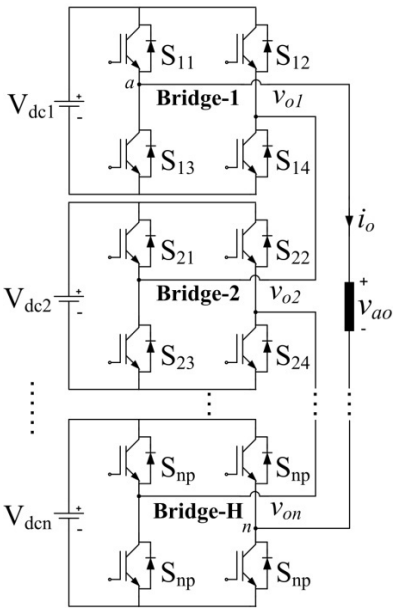


Fig. 1. General structure of CHB-MLI topology.

$$V_{ao,\max} = H \times V_{dc} \tag{2}$$

The switching functions 'T_{Snp}' is defined as

$$TSnp = \begin{cases} 1; Snp = Closed \\ 0; Snp = Open \end{cases} . \tag{3}$$

The expression for individual bridge voltages can be written as a function of the switching function as

$$\begin{aligned} v_{o1}(t) &= [(TS11 \times TS14)Vdc1 - (TS12 \times TS13)Vdc1] \\ v_{o2}(t) &= [(TS21 \times TS24)Vdc2 - (TS22 \times TS23)Vdc2] \\ v_{on}(t) &= [(TSn1 \times TSn4)Vdcn - (TSn2 \times TSn3)Vdcn] \end{aligned} . \tag{4}$$

The output voltage ($v_{ao}(t)$) of this topology is the sum of H-bridges output voltages ($v_{on}(t)$), expressed as

$$v_{ao}(t) = v_{o1}(t) + v_{o2}(t) + ... + v_{on}(t) = \sum_{k=1}^{H} v_{ok}(t) . \tag{5}$$

B. Modulation Scheme

The modulation technique controls the turn-on and turn-off of switches from one state to another, to synthesize the desired output voltage of low harmonic content. Multilevel inverters consist of a number of switches compared to two-level inverter topology, and thus, modulation results in increased complexity. A number of schemes have been developed and adopted, each with its own unique merits and demerits, depending upon the application and inverter topology [12], [13]. In the case of a multilevel inverter, the most discussed modulation schemes are multicarrier sine pulse width modulation (multicarrier-SPWM), selective harmonic elimination (SHE) and space vector PWM (SVPWM).

In this paper, multicarrier-Sine PWM was used to modulate MLIs [12], [18]. This modulation scheme involves the comparison of multiple carriers with a reference signal. Consider an output voltage with odd number of levels (N), and

then the number of positive level 'N_P' is given as

$$N_P = \frac{N-1}{2} \tag{6}$$

The number of carrier signals required in this scheme is '$2N_P$'. Next, consider the number of bridges, H=2. The output voltage levels (N) is '5' based on Eq. (1). Therefore, the modulation scheme of a five-level CHB-MLI involves comparison of four carrier signals (v_{car}) and a sinusoidal reference signal (v_{ref}). A sinusoidal reference signal of 50Hz is compared with four triangular carriers of 1 kHz frequency for generation of gate pulses, as shown in Fig. 2(a).

At every instant, these carrier signals (v_{car}) are compared with a sinusoidal reference signal (v_{ref}). When the reference signal is greater than the carrier signals in the positive half cycle (v^+_{car}), the comparison yields '1', otherwise '0'. Similarly, when the reference signal is greater than the carrier signals in the negative half cycle (v^-_{car}), the comparison yields '0', otherwise '-1', as given below:

$$f^+(t) = \begin{cases} 1, & for \quad v_{ref} \geq v^+_{car} \\ 0, & for \quad v_{ref} < v^+_{car} \end{cases} \tag{7}$$

$$f^-(t) = \begin{cases} 0, & for \quad v_{ref} \geq v^-_{car} \\ -1, & for \quad v_{ref} < v^-_{car} \end{cases} \tag{8}$$

The results obtained from the comparison are added to generate the aggregated signal ($f_{agg}(t)$).

$$f_{agg}(t) = \sum f^+(t) + \sum f^-(t) \tag{9}$$

This aggregates signal resembles the output voltage waveform shown in Fig. 2(a) from which the gating signals are derived using level comparisons, switching table and logic operations. The block diagram of this scheme is shown in Fig. 2(b). This scheme has been adopted to implement charge balancing schemes.

III. CHARGE BALANCING SCHEMES

In this paper, a CHB-MLI with two H-bridges (H=2) is considered. With H=2, the output voltage level is obtained as '5' from Eq. (1). This five-level CHB-MLI is connected to two isolated DC sources of equal values (V_{dc1} and V_{dc2}). However, the time duration of use of these two DC sources may differ because of the modulation requirement. Consider an operating condition, where source 1 (V_{dc1}) is used for the generation of levels 1 and 2 (V_{dc} and $2V_{dc}$) and source 2 (V_{dc2}) is used to generate level 2 ($2V_{dc}$). In this case, the DC source (V_{dc1}) is connected to the load for a longer time duration compared to the level 2 DC source (V_{dc2}), leading to uneven power drawn from the two sources. Therefore, DC source 1 (V_{dc1}) discharges sooner than DC source 2 (V_{dc2}). After a long operation, the aforementioned condition results in a difference in SOC and unsteady voltages that causes a reduction in the life cycle of the DC sources.

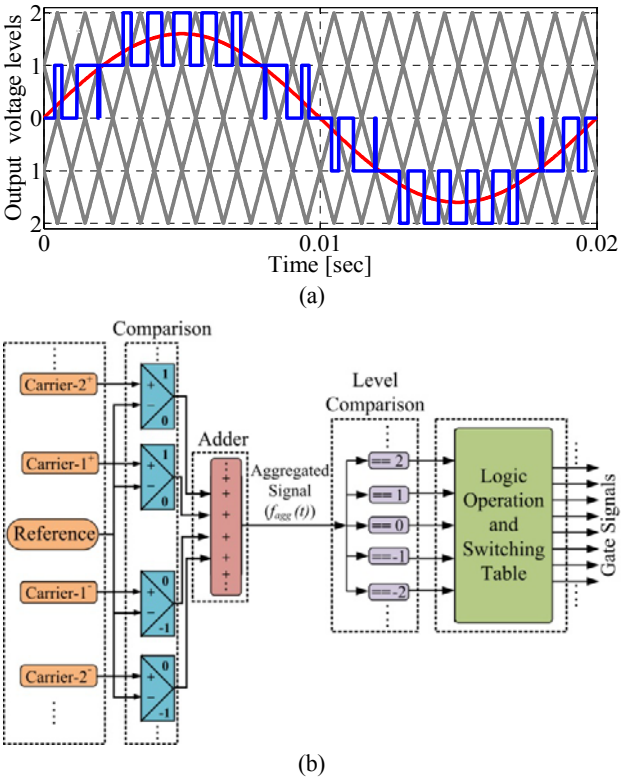


Fig. 2. (a) Multicarrier-Sine PWM for a five-level CHB-MLI, (b) Block diagram of modulation scheme.

An effective remedy for this situation is the incorporation of an efficient charge balance control along with the modulation scheme. The principle and operation of charge balancing schemes are explained in this section.

A. *Charge Balancing Based on Gate-Signal Swapping*

A charge balance control scheme for CHB-MLI was implemented for hybrid vehicle application [16], [17], in which a duty-cycle swapping circuit is used in addition to the duty-cycle calculation stage to implement charge balancing. This duty-cycle swapping circuit swaps the switching pattern among various levels at every half cycle to achieve balanced charging and/or discharging of sources. The drawback of this method is that in addition to the modulation scheme, a duty-cycle swapping circuit is necessary.

B. *Charge Balancing Based on Altered Aggregated Signal*

Another charge balancing method based on the altered aggregated signal has been introduced for a reduced device count MLI topology [19], [20]. This method has been extended to the CHB-MLI and used for modulation charge balancing in this work. The aggregated signal is derived from the comparison of the sinusoidal reference and triangular carrier signals, which are then level-shifted to obtain the 'altered aggregated signal' for charge balancing. The altered aggregated signal for this method for a five-level CHB-MLI is shown in Fig. 3.

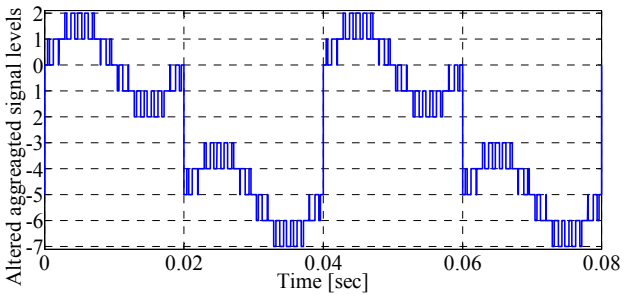


Fig. 3. Altered aggregated signal for 5-level CHB-MLI.

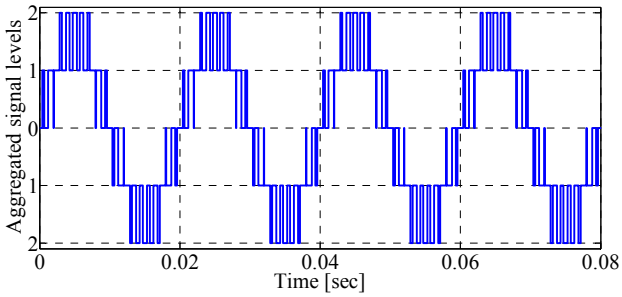


Fig. 4. Aggregated signal in proposed method.

TABLE I
SWITCHING TABLE FOR ALTERED AGGREGATED SIGNAL METHOD

Altered aggregated signal levels	Switching states (1=ON, 0=OFF)							
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
2 ($2V_{dc}$)	1	0	0	1	1	0	0	1
1 (V_{dc})	1	0	0	1	1	1	0	0
0 (0)	1	1	0	0	1	1	0	0
-1 ($-V_{dc}$)	0	1	1	0	1	1	0	0
-2 ($-2V_{dc}$)	0	1	1	0	0	1	1	0
-3 ($2V_{dc}$)	1	0	0	1	1	0	0	1
-4 (V_{dc})	1	1	0	0	1	0	0	1
-5 (0)	1	1	0	0	1	1	0	0
-6 ($-V_{dc}$)	1	1	0	0	0	1	1	0
-7 ($-2V_{dc}$)	0	1	1	0	0	1	1	0

To achieve charge balancing in five-level CHB-MLI, during the first half cycle of the altered aggregated signal source 1 (V_{dc1}) is used for the generation level 1 (V_{dc}) and source 1 (V_{dc1}) and source 2 (V_{dc2}) are used to generate level 2 ($2V_{dc}$). During the second half cycle, the altered aggregated signal (shifted portion) source 2 (V_{dc2}) is used to generate level 1 (V_{dc}) and source 1 (V_{dc1}) while source 2 (V_{dc2}) is used to generate level 2 ($2V_{dc}$). This step results in charge balancing over two cycles of the fundamental component being achieved. The switching table for this method is given in Table I. For a five-level CHB-MLI, this method requires ten level comparisons and the switching table should have ten switching states for charge balancing.

C. Proposed Method of Charge Balancing

To overcome the limitations of the altered aggregated signal method, a modified charge balancing method based on gate-signal swapping using aggregated signal is proposed in this paper. The proposed method uses the concept of both gate-signal swapping and aggregated signal scheme. In this method, an aggregated signal for five-level CHB-MLI is shown in Fig. 4. From the figure, it can be inferred aggregated signal should have only five levels for a five-level CHB-MLI. The altered aggregated signal method has ten levels, as shown in Fig. 3.

TABLE II
SWITCHING TABLE FOR PROPOSED METHOD

Aggregated signal levels	Switching states (1=ON, 0=OFF)							
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
2 ($2V_{dc}$)	1	0	0	1	1	0	0	1
1 (V_{dc})	1	0	0	1	1	1	0	0
0 (0)	1	1	0	0	1	1	0	0
-1 ($-V_{dc}$)	1	1	0	0	0	1	1	0
-2 ($-2V_{dc}$)	0	1	1	0	0	1	1	0

The basic concept of the proposed method is that it swaps the gate signal for each half cycle of the fundamental. For a five-level CHB-MLI, during the first half cycle of the aggregated signal, source 1 (V_{dc1}) is used to generate levels 1 and 2 (V_{dc} and $2V_{dc}$), while source 2 (V_{dc2}) is used to generate level 2 ($2V_{dc}$). During the second half cycle, the aggregated signal, source 2 (V_{dc2}) is used to generate levels 1 and 2 (V_{dc} and $2V_{dc}$), while source 1 (V_{dc1}) is used to generate level 2 ($2V_{dc}$). The switching table for the proposed method is given in Table II. Using the general equation of the bridge voltage given in Eq. (4), the bridge voltage equation for bridges 1 and 2 can be written as

$$v_{o1}(t) = [(TS11 \times TS14)Vdc1 - (TS12 \times TS13)Vdc1] \quad (10)$$

$$v_{o2}(t) = [(TS21 \times TS24)Vdc2 - (TS22 \times TS23)Vdc2] \quad (11)$$

The output voltage equation from Eq. (5) can be rewritten for five-level CHB-MLI as

$$v_{ao}(t) = v_{o1}(t) + v_{o2}(t) \quad . \quad (12)$$

For each level in the aggregated signal shown in Fig. 4, the corresponding bridge and output voltages of the suggested method can be expressed for each state, using the switching table given in Table II and Eqs. (10)–(12). The working states of the proposed method corresponding to each level of the aggregated signal are illustrated in Fig. 5.

State I:

$$v_{o1}(t) = [(TS11 \times TS14)Vdc1 = Vdc$$

$$v_{o2}(t) = [(TS21 \times TS24)Vdc2 = Vdc$$

$$v_{ao}(t) = v_{o1}(t) + v_{o2}(t) = 2Vdc$$

State II:

$$v_{o1}(t) = [(TS11 \times TS14)Vdc1 = Vdc$$

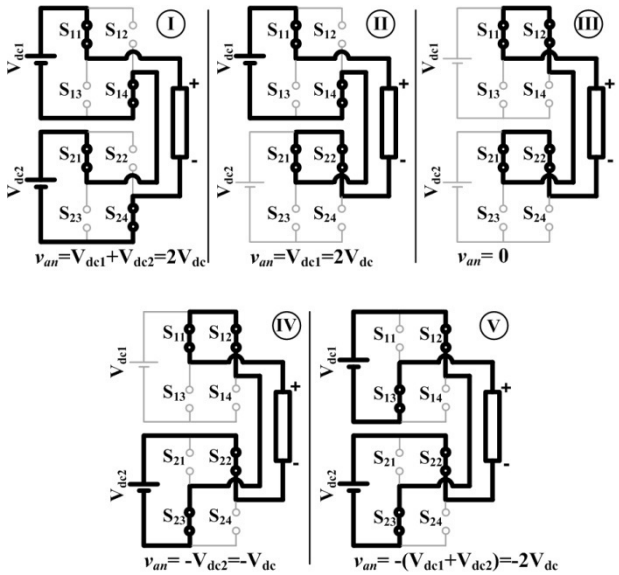


Fig. 5. Working states of charge balancing in proposed method.

$$v_{o2}(t) = 0$$

$$v_{ao}(t) = v_{o1}(t) + v_{o2}(t) = Vdc$$

State III:

$$v_{o1}(t) = 0$$

$$v_{o2}(t) = 0$$

$$v_{ao}(t) = v_{o1}(t) + v_{o2}(t) = 0$$

State IV:

$$v_{o1}(t) = 0$$

$$v_{o2}(t) = -(TS22 \times TS23)Vdc2 = -Vdc$$

$$v_{ao}(t) = v_{o1}(t) + v_{o2}(t) = -Vdc$$

State V:

$$v_{o1}(t) = -(TS12 \times TS13)Vdc1 = -Vdc$$

$$v_{o2}(t) = -(TS22 \times TS23)Vdc2 = -Vdc$$

$$v_{ao}(t) = v_{o1}(t) + v_{o2}(t) = -2Vdc$$

IV. Simulation and Experimental Results

In this section, the simulation and experimental results are presented to prove the effectiveness and validity of the proposed charge balance control scheme. A five-level and a seven-level CHB-MLI was investigated for three different conditions, including conventional method (no-charge balance), charge balancing by altered aggregated signal method and the proposed method through simulation. A five-level CHB-MLI has been implemented for experimental validation. All simulations were carried out on MATLAB/Simulink block sets and the switches are assumed to be ideal.

A prototype of a five-level CHB-MLI with gate driver circuit and RL-load (R=35Ω, L=65mH) was implemented. This setup has been used to implement the conventional charge balancing by altered aggregated signal and proposed schemes

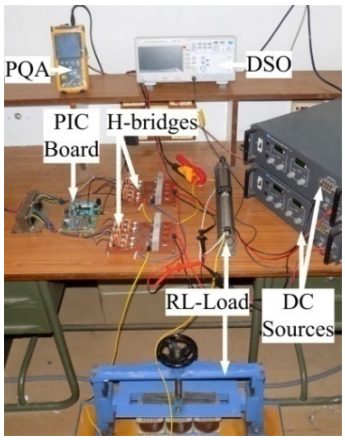


Fig. 6. Experimental setup.

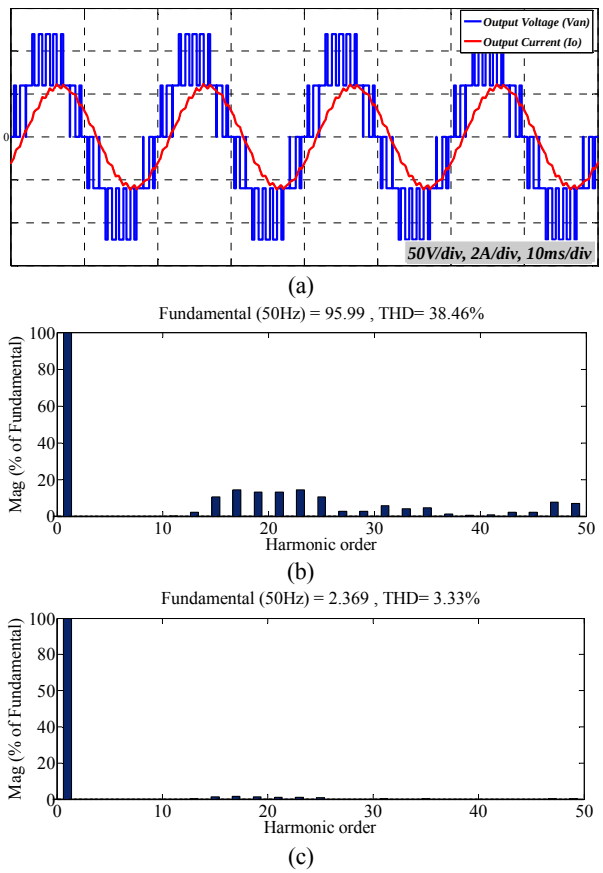
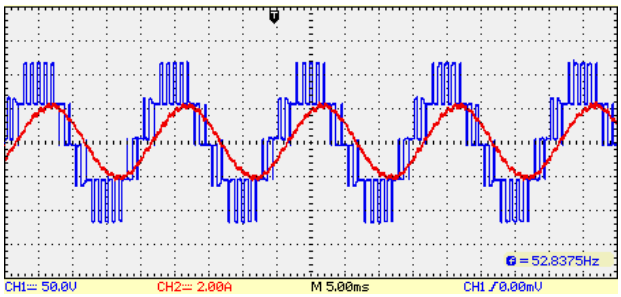


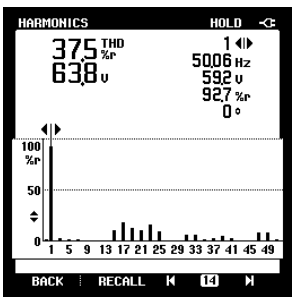
Fig. 7. Simulation results of the five-level CHB (a) Simulated waveforms of output voltage and current, (b) Harmonic spectrum of output voltage, and (c) Harmonic spectrum of output current.

for five-level CHB-MLI. The FGA15N120 IGBTs with internal anti-parallel diodes are used for the prototype. Modulation and charge balance control schemes are implemented using PIC18F4520. The isolated DC source voltages are selected as V_{dc1}=V_{dc2}=V_{dc}=60V for simulations and experiments of five-level CHB-MLI. Using Eq. (2), the maximum output voltage can be achieved is 120V. The experimental setup is depicted in Fig. 6.

Figs. 7(a) and 8(a) show the simulation and experimental



(a)



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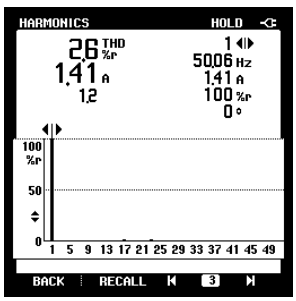


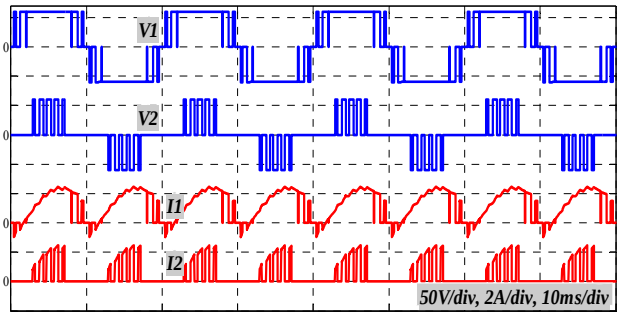
(c)

Fig. 8. Experimental results of five-level CHB (a) Measured waveforms of output voltage and current, (b) Harmonic spectrum of output voltage, and (c) Harmonic spectrum of output current.

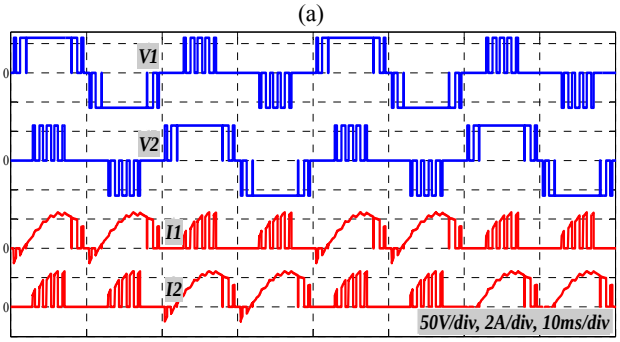
results of the output voltage (v_{ao}) and output current (i_o) for the five-level CHB-MLI. The results remain same for all three cases and thus were not repeated. The current waveform is closer to the sinusoidal waveform compared to voltage waveform because the load is an RL-load that acts as a low-pass filter. A phase difference can be observed between the fundamental component of voltage and current because of the inductive effect. The harmonic spectra of the output voltage and current of the simulated and measured waveforms of five-level CHB-MLIs are shown in Figs. 7(b) and (c) and Figs. 8(b) and (c), respectively.

The simulation and experimental waveforms of H-bridge voltages and corresponding source currents for conventional method (no-charge balance) for a five-level CHB-MLI are shown in Figs. 9(a) and 10, respectively. In the figures, v_1 and v_2 denote the output voltages of H-bridges and i_1 and i_2 denote the source currents. In this method, source 1 (V_{dc1}) is used for the generation of levels 1 and 2 (V_{dc} and $2V_{dc}$) , while source 2 (V_{dc2}) is used to generate level 2 ($2V_{dc}$) for the entire period of operation.

Figs. 9(b) and 11 show the simulation and experimental waveforms of output of H-bridges (v_1 and v_2), and input current to H-bridges (i_1 and i_2) for charge balancing using the altered aggregated signal method for a five-level CHB-MLI. The simulated and experimental results of H-bridge voltages and corresponding source currents and DC source voltages (V_{dc1} and V_{dc2}) for the proposed method for a five-level CHB-MLI are shown in Figs. 9(c) and 12, respectively. The power drawn from the DC sources in each case is given in Table III.



(a)



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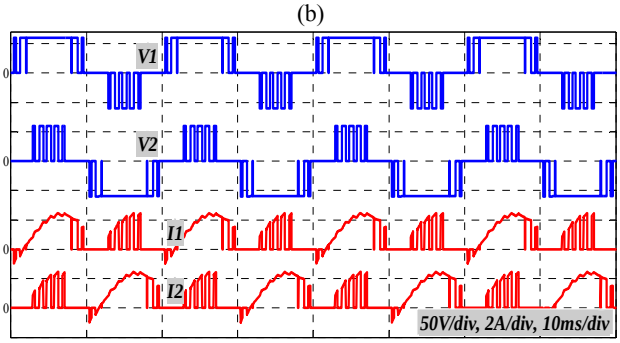


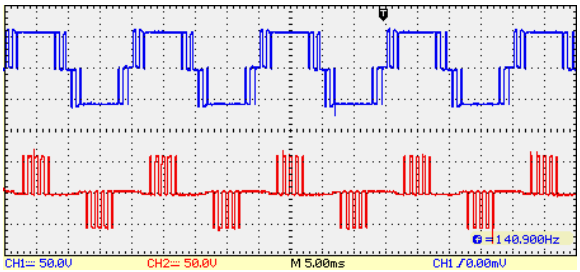
(c)

Fig. 9. Simulated waveforms of H-bridge voltages and source currents for five-level CHB-MLI (a) Conventional method (b) Altered aggregated signal method (c) Proposed Method.

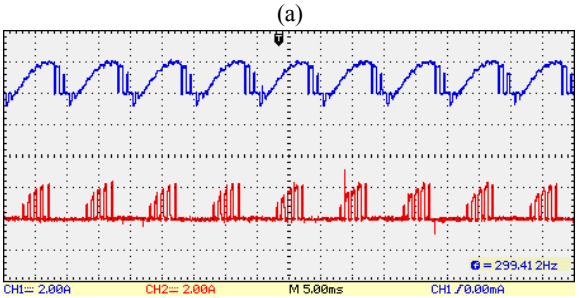
TABLE III
COMPARISON OF POWER DRAWN FROM SOURCES

Charge balancing scheme	Power Drawn	
	H-bridge-1	H-bridge-2
Conventional method	47.12	22.64
Altered aggregated signal	34.86	34.96
Proposed method	34.88	34.95

To demonstrate the effectiveness of the proposed for higher level of MLI, simulations of the conventional method (no-charge balance), charge balancing using the altered aggregated signal and proposed methods was carried out in a seven-level CHB-MLI. In this case, the DC sources were selected as $V_{dc1}=V_{dc2}=V_{dc3}=V_{dc}=60$V. Using Eq. (2), the maximum output voltage that can be achieved in this configuration is 180V. The bridge voltages can be formulated using Eq. (3) by substituting $H=3$ and the output voltage can be calculated using Eq. (4).

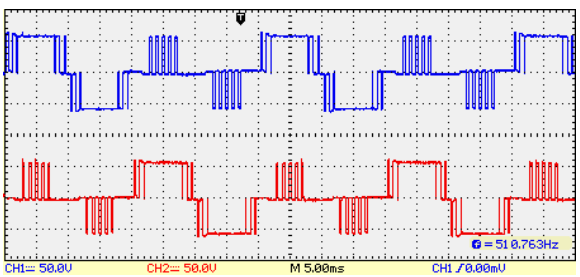


(a)

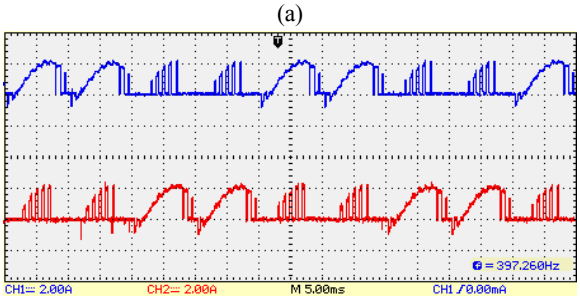


(b)

Fig. 10. Conventional method (a) Measured waveforms of H-bridge voltages, (b) Measured waveforms of source currents.



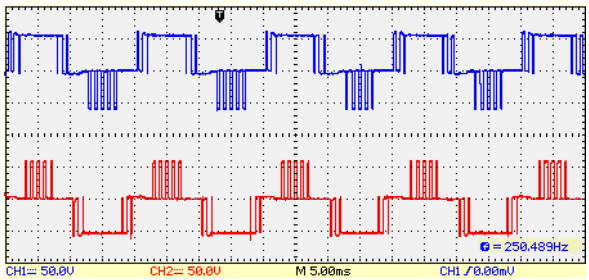
(a)



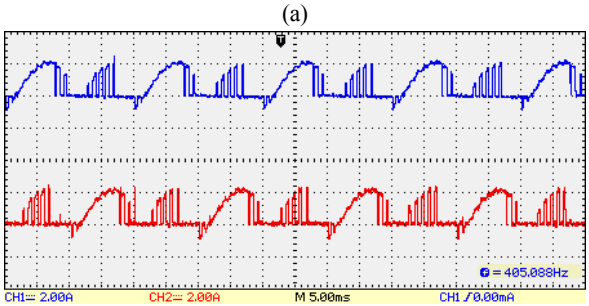
(b)

Fig. 11. Altered aggregated signal method (a) Measured waveforms of H-bridge voltages, (b) Measured waveforms of source currents.

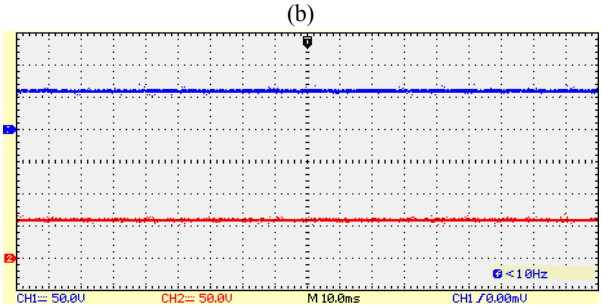
Fig. 13 shows the simulated waveforms of the output voltage (v_{ao}) and output current (i_o) of a seven-level CHB-MLI. Fig. 14(a) shows the simulated waveforms of output voltages of H-bridges (v_1, v_2 and v_3), and input current to H- bridges (i_1, i_2 and i_3) for conventional (no charge balance) in a seven-level MLI. Fig. 14(b) shows the simulation results of charge balancing using altered aggregated signal method for seven-level CHB-MLI. Similarly, the simulation results of H-bridge voltages and corresponding source currents for the proposed method for a seven-level CHB-MLI are shown in Fig. 14(c).



(a)



(b)



(c)

Fig. 12. Proposed method (a) Measured waveforms of H-bridge voltages (b) Measured waveforms of source currents (c) Measured waveforms of source voltages.

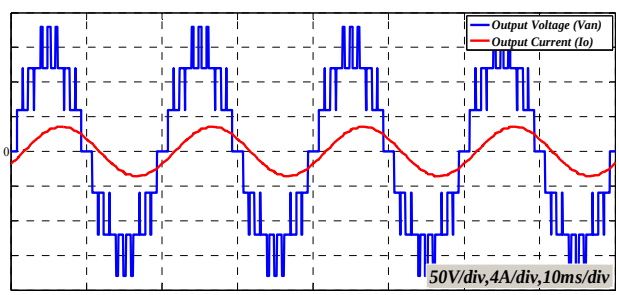


Fig. 13. Simulated waveforms of output voltage and current of 7-level CHB-MLI.

V. DISCUSSION

The experimental results are found to be in close agreement with the respective simulation results in each case. Therefore, MLI with the proposed charge balance scheme can deliver the required power. The results show that the charge balancing successively achieved balanced DC source discharge and power balancing. The power drawn from the DC sources in the case of the conventional, altered aggregated signal method and the proposed methods are indicated in Table III. In the case of the conventional scheme, the power drawn from the sources

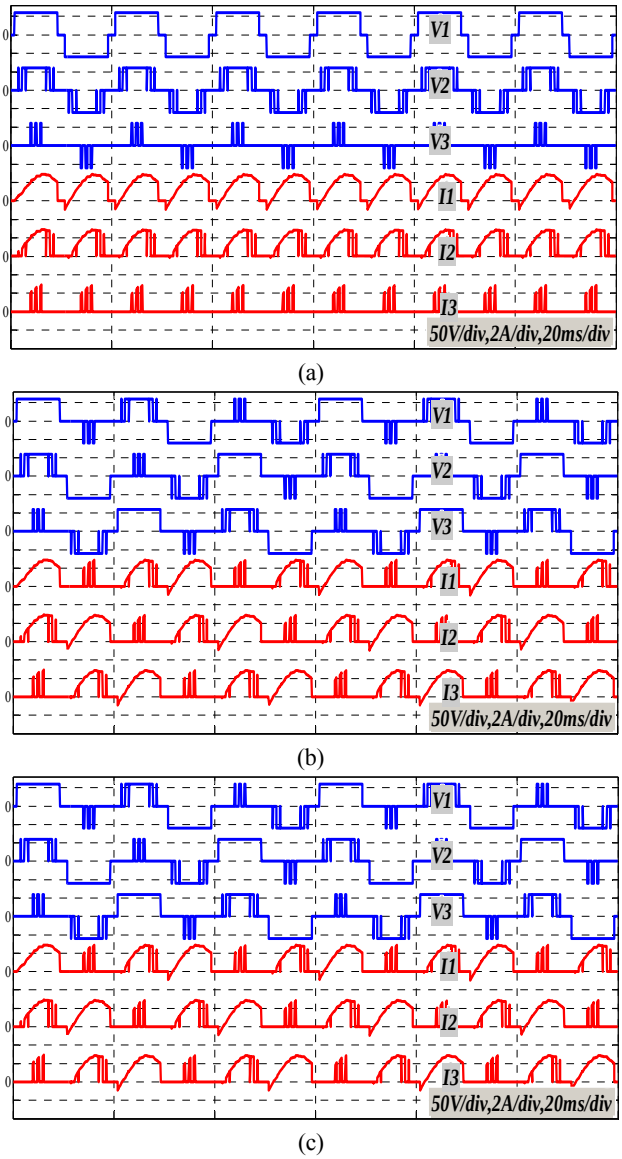


Fig. 14. Simulated waveforms of H-bridge voltages and source currents for 7-level CHB-MLI (a) Conventional method (b) Altered aggregated signal (c) Proposed method.

differs. The least power was drawn from DC source 2 (V_{dc2}). Clearly, the altered aggregated signal and proposed methods achieved charge balancing, as shown in Table III.

Charge balancing based on the gate-signal swapping method requires a duty-cycle swapping circuit in addition to the modulation scheme [16], [17]. The method based on altered aggregated signal is superior to the gate-signal swapping method because it does not require additional stage other than the modulation scheme to implement charge balancing. However, the drawback of this method is that a five-level CHB-MLI requires ten level comparisons because the altered aggregated signal has ten distinctive states, as indicated in Fig. 3 and Table I. As the output levels increases, level comparisons and switching table also increase, leading to increased complexity in modulation and implementation. The realization of the auxiliary signal method for charge balancing requires increased implementation effort and computational requirement [18].

TABLE IV
COMPARISON OF CHARGE BALANCING SCHEMES

Charge balancing scheme	Computational burden and realization effort	Charge balancing time	
		5-level	7-level
Auxiliary signal method [18]	High	2 cycles	3 cycles
Altered aggregated signal method	Medium	2 cycles	3 cycles
Proposed method	Less than altered aggregated signal	1 cycles	1.5 cycles

The proposed scheme does not require additional stage to the modulation scheme for charge balancing. This method only has five level comparisons because the aggregated signal only has five distinctive states, as shown in Fig. 4 and Table II. Table IV shows the comparison of implementation effort and the time taken for charge balancing in different methods for five- and seven-level CHB-MLIs. These results shows that the proposed scheme is superior to the gate signal swapping method, altered aggregated signal method, and auxiliary signal method of charge balancing in terms of the realization requirement, computational burden, realization effort, and time taken for charge balancing.

VI. CONCLUSIONS

A novel approach for charge balancing in symmetric cascaded H-bridge multilevel inverter was presented. The operation and effectiveness of the proposed method were simulated, experimentally verified, and compared with existing methods. The results show that the suggested method has minimum implementation effort and time required for charge balancing without any additional stages, complex circuits, or considerable computational requirement. The proposed method achieves balanced charging/discharging of the sources. The power drawn from the sources are also balanced, thereby extending the life of the sources. This balance enables the proper utilization of sources, which could be effectively adopted in applications employing a number of isolated sources in the integration of renewable energy systems and hybrid vehicle applications.

REFERENCES

[1] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 625-636, Feb. 2013.

[2] J. D. Barros, J. F. A. Silva, and É G. A. Jesus, "Fast-predictive optimal control of NPC multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 2, pp.

619-627, Feb. 2013.
[3] K. M. Kim, W. S. Choi, and K. H. Park, "Novel carrier-based hybrid pulse width modulation method for cascaded capacitor-clamp multilevel inverter," *IET Power Electronics*, Vol. 7, No. 10, pp. 2678-2686, Oct. 2014.
[4] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6712-6724, Dec. 2014.
[5] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Trans. Power Electron.*, Vol. 31, No. 1, pp. 135-151, Jan. 2016.
[6] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Reduction of power electronic elements in multilevel converters using a new cascade structure," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 1, pp. 256-269, Jan. 2015.
[7] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.
[8] Z. Zheng, K. Wang, L. Xu, and Y. Li, "A hybrid cascaded multilevel converter for battery energy management applied in electric vehicles," *IEEE Trans. Power Electron.*, Vol. 29, No. 7, pp. 3537-3546, Jul. 2014.
[9] N. Kumar, T. K. Saha, and J. Dey, "Modeling, control and analysis of cascaded inverter based grid-connected photovoltaic system," *International Journal of Electrical Power & Energy Systems*, Vol. 78, pp.165-173, Jun. 2016.
[10] M. R. Islam, Y. Guo, and J. Zhu, "A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems," *IEEE Trans. Power Electron.*, Vol. 29, No. 8, pp. 4167-4182, Aug. 2014.
[11] W. Liang, H. Abu-Rub, Y. Liu, and B. Ge, "State-of-charge balancing control for battery energy stored quasi-Z source cascaded multilevel inverter based photovoltaic power system," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 8-13, Sep. 2015.
[12] R. Naderi and A. Rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," *IEEE Trans. Power Electron.*, Vol. 23, No. 3, pp. 1257-1269, May 2008.
[13] A. Edpuganti and A. K. Rathore, "A survey of low switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 5, pp. 4212-4228, Sep./Oct. 2015.
[14] E. Babaei and M. S. Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem," *Energy Conversion and Management*, Vol. 51, No.11, pp. 2272-2278, Nov. 2010.
[15] E. Babaei and M. S. Moeinian, "Charge balance control methods for a class of fundamental frequency modulated asymmetric cascaded multilevel inverters," *Journal of Power Electronics*, Vol. 11, No. 6, pp. 811-818, Nov. 2011.
[16] L. A. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.,* Vol. 49, No. 5, pp. 1058-1064, Oct. 2002.
[17] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, Vol. 35, No. 1, pp. 36-44, Jan./Feb. 1999.
[18] C. C. Hua, C. W. Wu, and C. W. Chuang, "A novel dc voltage charge balance control for cascaded inverters," *IET Power Electronics*, Vol. 2, No. 2, pp. 147-155, Mar. 2009.
[19] K. K. Gupta and S. Jain, "A novel universal control scheme for multilevel inverters," in *Proceedings of the 6th IET International Conference on Power Electronics, Machines and Drives (PEMD)*, pp. 1-6, May 2012.
[20] K. K. Gupta and S. Jain, "Topology for multilevel inverters to attain maximum number of levels from given DC sources," *IET Power Electronics*, Vol. 5, No. 4, pp. 435-446, Apr. 2012.

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