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# Improvement on the Laminated Busbar of NPC Three-Level Inverters based on a Supersymmetric Mirror Circulation 3D Cubical Thermal Model

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**Abstract**

Laminated busbars with a low stray inductance are widely used in NPC three-level inverters, even though some of them have poor performances in heat equilibrium and overvoltage suppression. Therefore, a theoretical method is in need to establish an accurate mathematical model of laminated busbars and to calculate the impedance and stray inductance of each commutation loop to improve the heat equilibrium and overvoltage suppression performance. Firstly, an equivalent circuit of a NPC three-level inverter laminated busbar was built with an analysis of the commutation processes. Secondly, on the basis of a 3D (three dimensional) cubical thermal model and mirror circulation theory, a supersymmetric mirror circulation 3D cubical thermal model was built. Based on this, the laminated busbar was decomposed in 3D space to calculate the equivalent resistance and stray inductance in each commutation loop. Finally, the model and analysis results were put into a busbar design, simulation and experiments, whose results demonstrate the accuracy and feasibility of the proposed method.

**Key words:** 3D cubical thermal model, Laminated busbar, Mirror circulation, NPC three-level inverter

## I. INTRODUCTION

The electromagnetic compatibility theory shows that every conductor, including the NPC three-level inverter, has a stray inductance, whose value is related to the frequency, shape, space and magnetic field that the conductor exists in [1]. During the commutation process of high power inverters, the existence of stray inductance in the commutation path causes an instantaneous turn-off overvoltage, which has an impact on the power devices and may cause damages to them when the overvoltage is too high. The overvoltage can be calculated by:

$$V_{off} = L_{stray} \frac{di}{dt} \quad (1)$$

where $V_{off}$ is the turn-off overvoltage, $L_{stray}$ is the stray inductance, and $\frac{di}{dt}$ is the change rate of the current. From (1), it can be known that $V_{off}$ is decided by both $L_{stray}$ and $\frac{di}{dt}$. In medium and small power inverters, the turn-off overvoltage can be suppressed by applying an absorption circuit, such as a RCD circuit. However, in high-power inverters, the stray inductance generates a lot of energy during the commutation process, which requires a high frequency absorption capacitor and an absorption resistance with large power capacities. However, this will introduce new problems in the structure and increases in the power-loss. Therefore, in high power inverters using IGBTs, it does not introduce an additional absorption loop to suppress the turn-off overvoltage.

[2]-[6],[25] and [26] show that at present, to reduce switching loss, high-power inverters usually apply hard switching circuits and their switching rates are in $\mu s$ level. However, this is too fast resulting in a high overvoltage. The most effective way to suppress this is to minimize the

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commutation loop stray inductance $L_{stray}$.

The application of laminated busbars in high-power inverters has several advantages compared with traditional cables, such as a much more compact structure with a flat conductor and insulation layer, excellent heat dissipation performance, low stray inductance, and so on. Some studies on laminated busbars in high-power inverters have been done, among which [3],[5],[7] and [8] made enough of an electromagnetic analysis for laminated busbars, but without an accurate thermal analysis. As proposed in [9], for the laminated busbars used in high-power inverters, the main factor limiting the current carrying capability is the busbar temperature. Too high a temperature will cause damage to the insulation layers of the busbars and too low a temperature means that the busbar is oversized. Therefore, the most basic requirement for busbar design is to minimize the busbar size while keeping its operation temperature under the safe operating temperature of power devices. [10],[11] and [25] hold the point that the stray inductance in high-power inverters has a large affect on the turn-off characteristic of power devices, and that the laminated busbar with its low stray inductance can suppress the turn-off voltage spike of power devices and minimize the structure without using RCD absorption circuits.

In order to estimate the busbar operation temperature at the design period, it is necessary to build an accurate thermal model of a busbar in accordance with the topology of a NPC three-level inverter and commutation loops. This model will be useful in the calculation and estimation of current carrying capacity, stray inductance and operation temperature. Several numerical and analytical methods have been studies in the past few years, among which [12]-[14] made steady-state and transient analyses, while a 2D analysis was carried out in both [15][16]. Because of the slow transient thermal characteristic and fast electric transients of busbars, the temperature change caused by a fast and periodic change current can be ignored [17][18]. A laminated busbar design and a stray parameter analysis of three-level converters based on the HVIGBT series connection were conducted in [19] to provide a practical method. In [20], a compromised optimal design scheme was proposed to realize the modeling and optimization of a high power inverter three-layer laminated busbar. In [21], a resonance analysis method for the DC-side laminated bus-bar of a high speed switching circuit was proposed for the next-generation, such as SiC and GaN. A 3-D numerical analysis was made for the special joints of a complicated busbar for thermal analysis. For digital methods with a high precision, such as the finite element method and computational fluid dynamics, they are rather expensive in terms of model setup and computational time [22]. A reasonable analysis method which asks for an equivalent model for the complex circuit with high accuracy can increase the calculation speed.

In this paper, a thermal network was introduced according to the analysis of an equivalent circuit and the commutation process of a NPC three-level inverter to build a 3D cubical thermal model. This is the basis of the decomposition and calculation of a busbar to 3D space. In [23], a simple thermal network was used to predict the temperature of a busbar superposed by two copper plates and it obtained good performance. However, during the laminated busbar analysis, the accurate power loss of a busbar is the premise of building a precise thermal model. Therefore, the power loss of each commutation path was calculated and put into a thermal model as a heat source. In order to get the supersymmetric mirror circulation in every commutation loop, all of the circulation loops should be as nearly equal as possible, which means that every path should have the same impedance. Based on a supersymmetric mirror circulation 3D cubical thermal model, each commutation circuit was decomposed on the x, y, z axes on the 3D coordinate system in this paper to provide references for the busbar design.

This paper is organized as follows. Section II describes the equivalent circuit and communication loops of a NPC three-level inverter. In Section III, the supersymmetric 3D thermal model was built and then put into the busbar analysis and design. In Section IV, a calculation of stray inductance, a thermal analysis, an overvoltage test and performance experiments were carried out. Finally, some conclusions were drawn in Section V.

## II. Equivalent Circuit and Commutation Loop Analysis

### A. Equivalent Circuit

The equivalent circuit shown in Fig. 1 illustrates the distribution of the stray inductances in a single-phase bridge arm, and for the sake of convenience, all of the stray inductances can be divided as follows. $L_{s1}$, $L_{s2}$, $L_{s3}$, $L_{s4}$, $L_{s5}$, $L_{s6}$, $L_{s7}$ and $L_{s8}$ are the connecting stray inductances of the four IGBTs; $L_{d1}, L_{d2}, L_{d3}$ and $L_{d4}$ are the connecting stray inductances of the two clamping diodes; $L_{c1}, L_{c2}, L_{c3}$ and $L_{c4}$ are the connecting stray inductances of the capacitors; and $L_{DC}$ is the connecting stray inductance of the neutral point.

As shown in Fig. 1, there are six equipotential junctions in a single-phase bridge arm of the three-level topology, where $A$ and $A'$ are the positive and negative junctions of the DC side; $B$ and $B'$ are the junctions of the upper and lower bridge arm and the clamping diodes; $E$ is the midpoint junction of the DC side; and $O$ is the output junction of the bridge arm. Each equipotential junction needs a conducting plate, and six plates were needed in one bridge arm. These

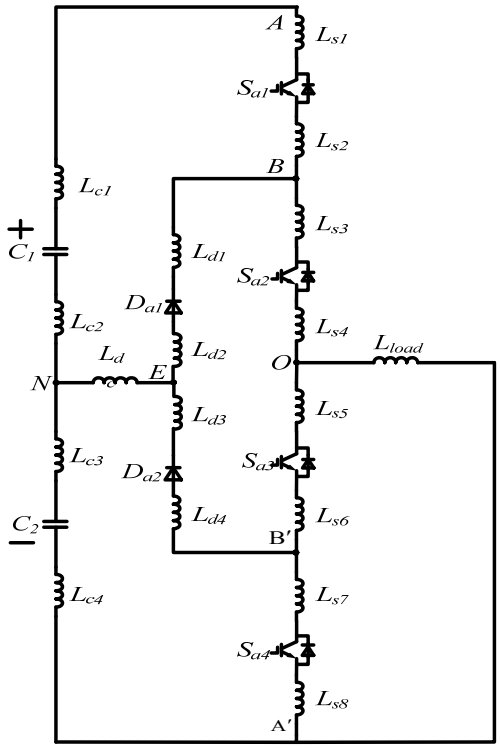



Fig. 1. Stray inductance equivalent circuit of single-phase bridge arm in NPC three-level inverter.

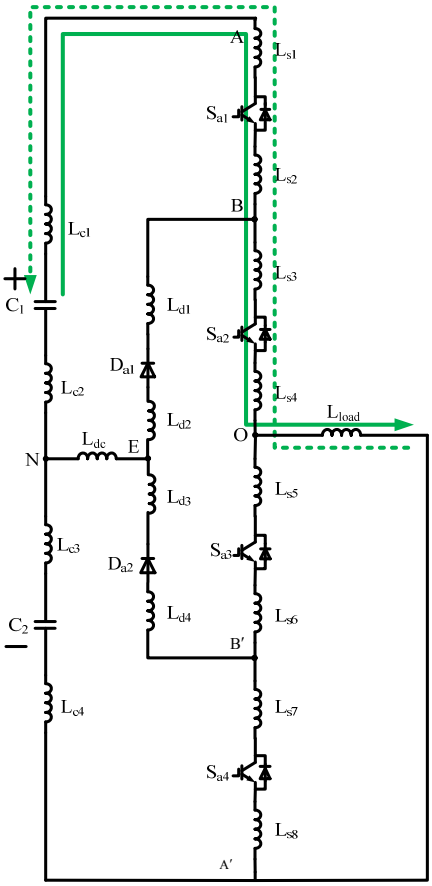
are the positive busbar layer, negative busbar layer, upper bridge arm clamping layer, lower bridge arm clamping layer, zero bus layer and output layer. When the load inductance $L_{load}$ is large enough, the load current can be considered as a constant value during the processes of commutation. Therefore, the output layer does not affect the stray inductance of the commutation loops and during the busbar design it can be placed in each side of the busbar.

There are great differences among the stray inductances generated from conducting plates with different stacked sequences and combinations in different commutation loops. An analysis of the commutation processes will be made in the following section.

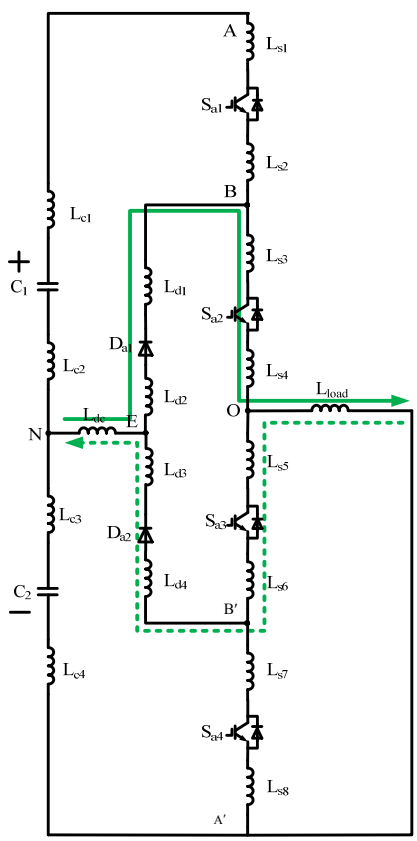
### *B. Analysis of the Commutation Loops*

The stray inductances are different in different commutation loops since they are caused by different switching states and current flows in the three-level topology.

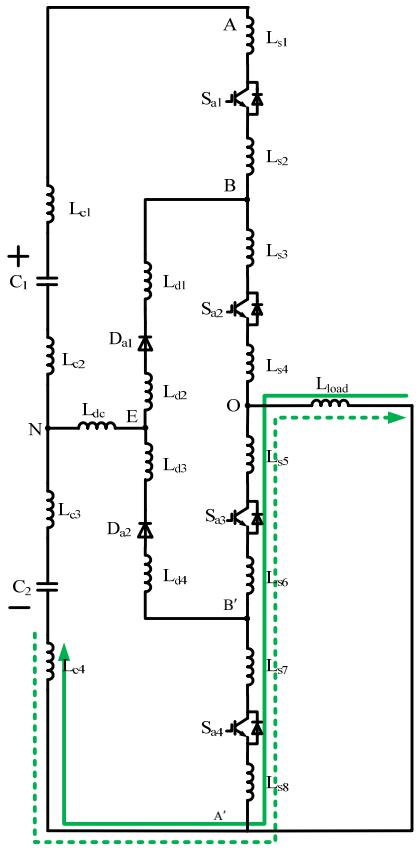
In Fig. 2, the solid line and dotted line stand for the output and input currents, respectively. It can be seen from Fig. 2 that the stray inductances involved in switching state 1 are $L_{c1}$, $L_{c2}$, $L_{s1}$, $L_{s2}$, $L_{s3}$ and $L_{s4}$; the stray inductances involved in switching state -1 are $L_{c3}$, $L_{c4}$, $L_{s5}$, $L_{s6}$, $L_{s7}$ and $L_{s8}$; the stray inductances involved in switching state 0 with an output current are $L_{DC}$, $L_{d1}$, $L_{d2}$, $L_{s3}$ and $L_{s4}$; and the stray inductances involved




(a) Commutation loop of switching state 1.




(b) Commutation loop of switching state 0.




(c) Commutation loop of switching state -1.

Fig. 2. Commutation loops in single bridge arm of three-level inverter.

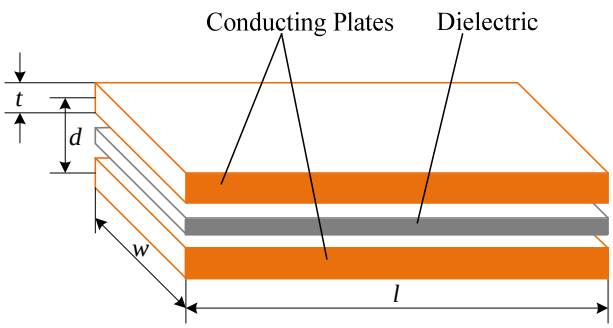



Fig. 3. Diagram of busbar.

in switching state 0 with an input current are $L_{DC}$, $L_{d3}$, $L_{d4}$, $L_{s5}$ and $L_{s6}$. When the switching state changes, the stray inductance of the former commutation loop generates a turn-off overvoltage, which is harmful to the power devices. Suppressing this overvoltage is the basic target of the laminated busbar design.

## III. Analysis and Design

### A. Stray Inductance Analysis

The structure of the busbar is shown in Fig. 3. As a conductor working in multiple magnetic fields, the inductance generated by its own magnetic field is called the inner inductance and the inductance generated by the outside magnetic field is called the external inductance. They are marked with $L_i$ and $L_e$, respectively. The busbar can be equivalent to a lot of conductors in unit length. It was analyzed with one of them as shown in Fig. 4.

As known from the skin effect, when the frequency of the excitation source increases, the current tends to be distributed around the conductor outside as a circular area with a width of $\delta$, and a skin depth which can be defined as follows [25]:

$$\delta = 1/\sqrt{\pi f u \sigma} \tag{2}$$

Suppose the skin depth is equal to the conductor radius at a frequency of $f_\delta$, namely $\delta = r_w$. Then the conclusion can be obtained as:

(1) When $f < f_\delta$, the conductor resistance $R$ is equal to the resistance of the DC current; when $f > f_\delta$, the impedance increases with $\sqrt{f}$.

(2) When $f < f_\delta$, the inner inductance $L_i$ of the conductor is equal to the inductance $L_{iDC}$ of the DC current, and has no relation with the conductor radius; when $f > f_\delta$, the inner inductance of the conductors decreases with an increase of $\sqrt{f}$. The inner inductance can be calculated by:

$$L_i = \frac{\mu_0 \mu_r}{8\pi} l \tag{3}$$

where $\mu_r$ is the relative permeability of the conductor and $l$ is the length of the conductor.

The external inductance of the conductor has no relation with frequency $f$. However, it can be affected by factors such as the shape and distance, and for the laminated busbar, it is very complicated to accurately calculate the external inductance. Generally the approximate calculation, as shown in [24], can be realized by:

$$L_e = 2\mu_0 \mu_r \frac{tl}{\pi(t+w)}, \quad t << w \tag{4}$$

Due to the fact that the commutation frequency of a three-level inverter is over kHz, which is far less than $f_\delta$, both inner and external inductances of the busbar stray inductance should be considered, namely:

$$L_{busbar} = L_i + L_e \tag{5}$$

The magnetic field around the cylindrical conductor is

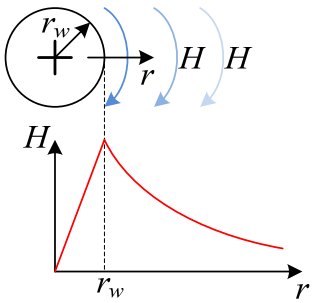



Fig. 4. Magnetic field around conductor.

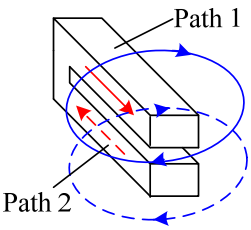



Fig. 5. Magnetic field distribution of busbar.

shown in Fig. 4, where $r_w$ is the radius of the current-carrying conductor, and $r$ stands for the distance to the conductor center. However, for the laminated busbar, because of its irregular structure, different current paths corresponding to different switching states and the existence of current path reuse, an inductance analysis would be difficult using traditional methods, which cannot easily calculate mutual inductance [25]. In addition, to use the mutual elimination of the magnetic field to optimize the busbar design, it is necessary to determine the total inductance. Therefore, to solve these difficulties, a supersymmetric mirror circulation theory was proposed in this paper. It means that two current loops flowing through two parallel laminated plates should be symmetrical in terms of both structure parameters and electrical parameters. The symmetrical structure parameters are basic technical requirements. Therefore, they are beyond the scope of this paper. Symmetrical electrical parameters means that the two current loops should be equal in value and opposite in direction. Both the symmetrical structure parameters and symmetrical electrical parameters from two different fields constitute the supersymmetric mirror circulation. As shown in Fig. 5, the supersymmetric mirror circulation can generate symmetrical magnetic fields with opposite directions, which eliminate each other in and around the conductor. Meanwhile, the inner and external inductances are also weakened greatly compared with the inductances generated by the current flow through only one plate. Therefore, the key point of the laminated busbar design is to design double mirror circulation paths to reduce the commutation stray inductance.

For a laminated busbar, the current-carrying plate is a uniform plane and its magnetic field intensity is:

$$\mathrm{B} = \frac{\mu_0 \alpha}{2} \tag{6}$$

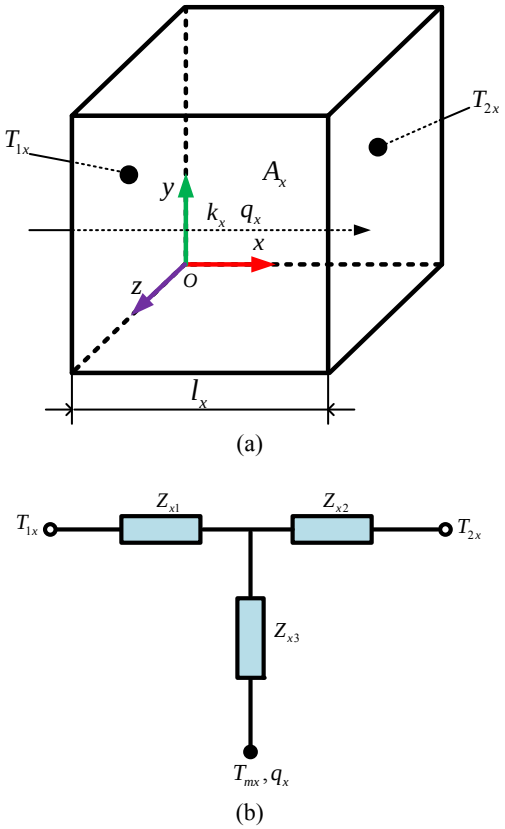



Fig. 6. (a) Supersymmetric 3D thermal model. (b) Equivalent thermal network of 3D thermal model in $X$ axis.

where, α is the current flowing through the unit length.

To achieve the maximum elimination of magnetic fields and excellent heat equilibrium of a laminated busbar, it is necessary to make two equivalent impedances in two commutation loops the same to obtain approximately α in two commutation circuits. However, due to the complicated commutation logic and the existence of the circuit coupling of a three-level inverter, it is difficult to get the overall equivalent circuit. Therefore, the supersymmetric mirror circulation 3D cubical thermal model will be proposed in the next section to build an equivalent model in the 3D coordinate system and to decompose the whole system in each coordinate axis for the purposes of calculating each equivalent impedance.

### *A. 3D Cubical Thermal Model of a Three-Level Inverter Laminated Busbar*

A cube model is put forward in [9], as shown in Fig. 3, and the thermal resistance in each coordinate axis can be calculated with it. On the basis of this model, take point "$O$" in Fig. 1 as the origin of the coordinate system and take the three commutation circuits in Fig. 2 as coordinate axes. Then a supersymmetric mirror circulation 3D cubical thermal model can be built as follows.

In Fig. 6, $T_{1x}$ and $T_{2x}$ are the surface temperatures in the

$x$ axis direction, and $T_{mx}$ is the average temperature in the $x$ axis direction.

From an electrical viewpoint, $Z_{xn}$ (n = 1, 2, 3) is the impedance value after decomposition to three dimensional space, and the expression is as follows:

$$Z_{xn} = R_{xn} + j\omega_h L \tag{7}$$

where $\omega_h$ is the $h$th harmonic frequency.

From the viewpoint of heat transfer, $R_{xn}$ in equation (7) stands for the thermal resistance of the network, which is calculated from equation (8) with no inner thermal source [9].

$$R_{xn} = \frac{l_x}{2k_x A_x} \tag{8}$$

where $l_x$ is the length of the cubical model in the $x$ axis direction, $k_x$ is the heat density in the $x$ axis direction, $q_x$ is the thermal conductivity in the $x$ axis direction, and $A_x$ is the cross-sectional area perpendicular to the $q_x$ direction. According to Fourier law, the definition of the thermal conductivity is as follows:

$$k_x = -\frac{q_x}{\left(\frac{\partial T}{\partial x}\right)} \tag{9}$$

where $\frac{\partial T}{\partial x}$ is the temperature gradient in this direction.

For devices without an inner heat source, such as an insulation layer, they can be equaled by the thermal resistances $R_{x1}$ and $R_{x2}$, and for devices with an inner heat source, such as a copper busbar, the third thermal resistance $R_{x3}$ is brought in to express the average temperature, which is shown in the following equation:

$$R_{x3} = -\frac{l_x}{6k_x A_x}. \tag{10}$$

All of the analyses in the $x$ axis above are also valid for the $y$, $z$ axes. Put all of these analyses into Fig. 1, and the equivalent thermal network of the 3D thermal model of a single bridge arm in a NPC three-level inverter will be obtained as shown in Fig.7.

where, $T_{mxyz}$ stands for the concentrated point of the $x$, $y$, $z$ axes.

To keep the currents flowing in all of the circulation loops equivalent under different switching states, it is necessary to make the impedances of these loops decomposed in the $x$, $y$, $z$ axes under these equal switching states. For three-level inverters, the currents flowing through laminated busbars are non-sinusoidal variables changing with time, and each harmonic will generate heat in them. Therefore, during the heat calculation of a laminated busbar, the Fourier decomposition method was introduced to extract every

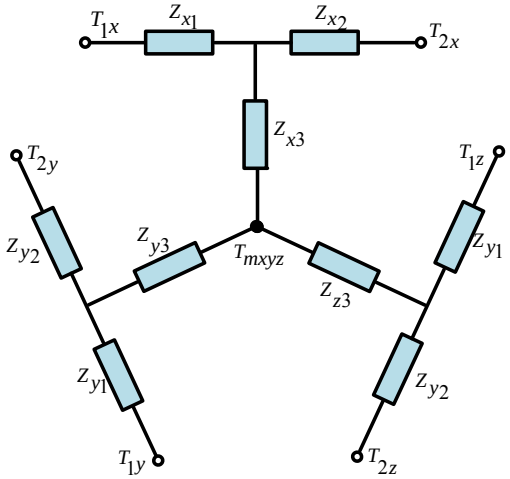



Fig. 7. 3D Equivalent thermal network of 3D thermal model of NPC three-level inverter.

harmonic. This can be expressed as follows [9]:

$$I_h = \frac{1}{\sqrt{2}} \cdot \mathrm{abs}\left(\frac{\mathrm{FFT}(i(t))}{\mathrm{n}}\right) \tag{11}$$

where $I_h$ is the rms value of the $h$th harmonic current, $i(t)$ stands for the current flowing through busbars, and n is the number of the sampling.

According to [9], the power loss of a laminated busbar is as follows:

$$P_b = \sum_{h=0}^{H} R_{b,h}(T_b(i)) \cdot I_h^{\,2} \tag{12}$$

where $P_b$ is the power loss, and $R_{b,h}$ is the thermal resistance of the $h$th harmonic under a temperature of $T_b(i)$.

Since the thermal resistance of a busbar changes with respect to temperature and frequency, in accordance with [9], $T_b$ can be expressed with a linear variation of the resistivity as follows:

$$T_b = \frac{\rho - \rho_0}{\rho_0 \alpha} + T_a \tag{13}$$

where $T_a$ is the ambient temperature, $\alpha$ is the coefficient of the electrical resistivity varying with temperature, $\rho$ is the electrical resistivity, and $\rho_0$ is the electrical resistivity at the ambient temperature.

### *B. Analysis and Design of the Switching States and a Busbar Based on the Supersymmetric Mirror Circulation*

By analyzing design schemes I and II in [23], it can be seen that changing the distribution of the devices can realize the complete mirror circulation and get excellent laminated performance. However, in some switching states, there are still some long one-way current paths. To solve this, the potential connection mode in the DC side can be changed and the distribution of the other devices is still arranged with the

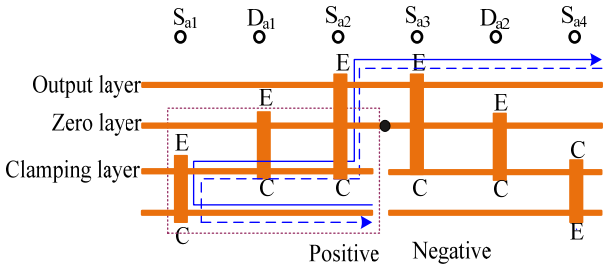



Fig. 8. Commutation loop of switching state 1.

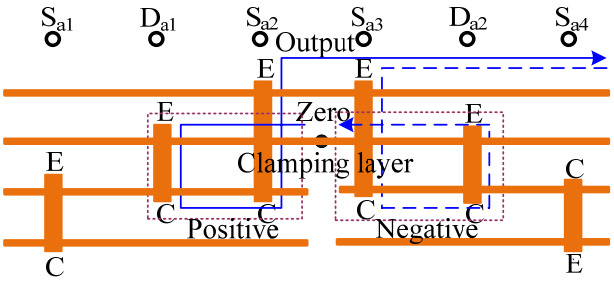



Fig. 9. Commutation loop of status 0.

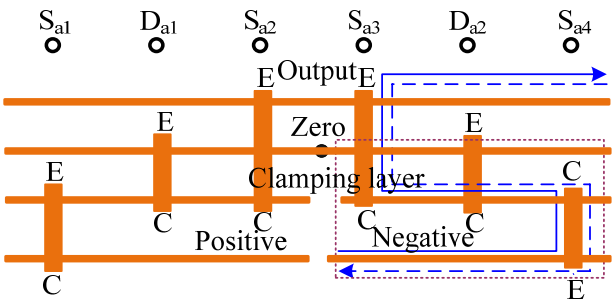



Fig. 10. Commutation loop of Status -1

layout of the schematic diagram.

*1) Switching State 1*: As shown in Fig. 8, the positive, negative and zero point of the DC side are all connected from the middle of the busbar, and the commutation loop, whose current path is a half of the busbar length, is complete under switching state 1 with excellent laminated performance.

In Fig. 8, the Es are the midpoint joints of the DC side.

*2) Switching State 0:* As shown in Fig. 9, although different current directions have different flowing paths in switching state 0, both paths were designed into symmetrical types in the middle layer, with a path length that is 1/4 of the busbar length, and the laminated effect is excellent.

*3) Switching State -1*: It can be seen by comparing Fig. 8 and Fig. 10 that, due to the middle inlet, switching state -1 has a similar laminated effect as switching state 1. In addition, both of them are complete half-busbar mirror circulations.

In this paper, the parameters of a winding asynchronous motor are shown in Table I, and component parameters of the inverter main circuit are shown in Table II.

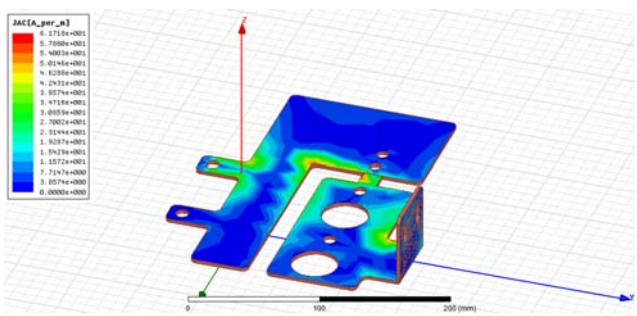
According to the different flowing paths under the three switching states above, the corresponding structure designs and the current density simulations for all of the paths in the busbar are as follows:

TABLE I
PARAMETERS OF WINDING ASYNCHRONOUS MOTOR

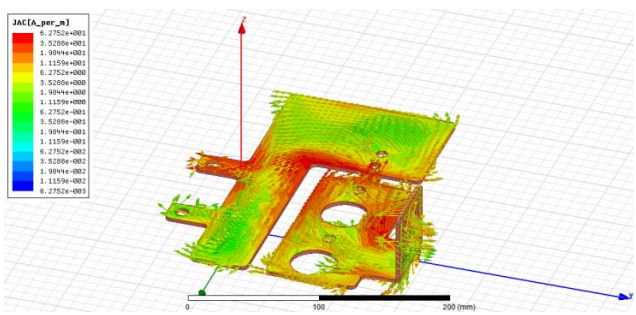
| | |
|---|---|
| Rated power Pd (kW) | 475 |
| Stator voltage $U_s$ (V) | 6000 |
| Stator current $I_d$ (A) | 59 |
| Rotor voltage $U_r$ (V) | 640 |
| Rotor current $I_r$ (A) | 435 |
| Rated speed (r/min) | 735 |
| Power factor | 0.85 |

TABLE II
COMPONENTS PARAMETERS OF INVERTER MAIN CIRCUIT

| | |
|---|---|
| $U_{dc}$ | 1100 V |
| DC-link capacitor parameters | 1800μF / 1300V |
| Power device parameters | Infineon,FF1400R17IE4 series |
| Switching frequency | 2000Hz |



(a) Structure design and current density simulation.

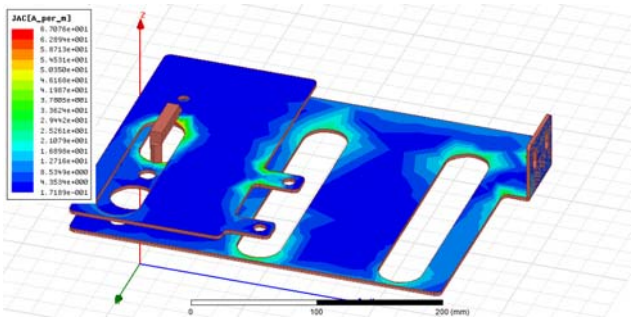


(b) Current flow simulation.

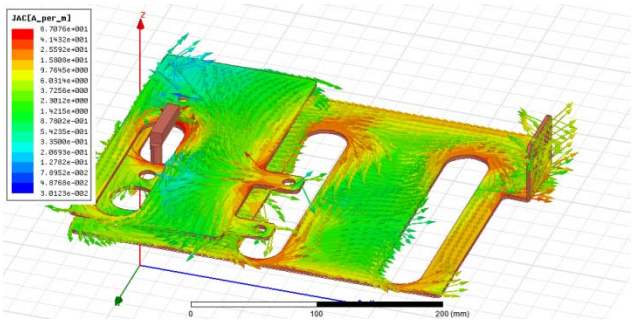
Fig. 11. Structure design and simulations of switching state 1.

It can be seen from Fig. 11, Fig. 12 and Fig. 13 that the structural designs of these three commutation loops have a good symmetry to stack up. It can also be seen in these figures that excellent conductive uniformities are shown in the current density simulations, and that current flows in these three loops are pretty good in terms of consistency.

In accordance with the supersymmetric mirror circulation theory and the parameters of the experimental platforms

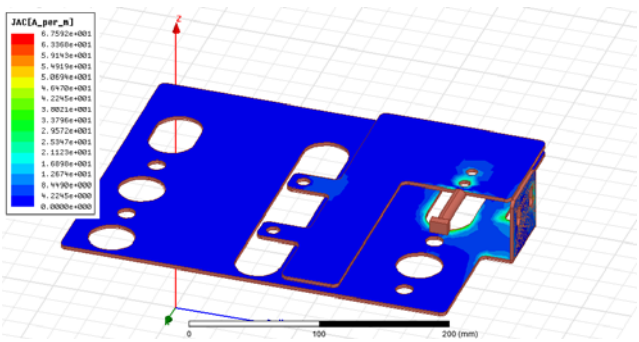


(a) Structure design and current density simulation.

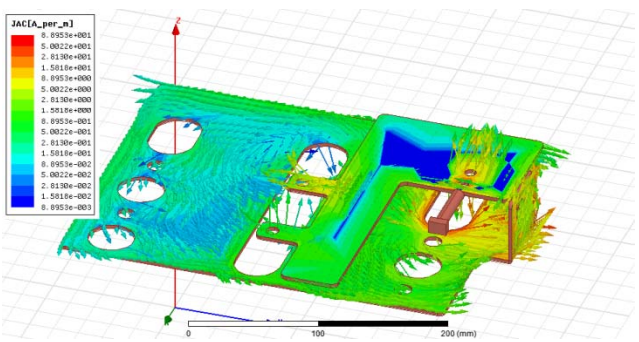


(b) Current flow simulation.

Fig. 12. Structure design and simulations of switching state 0 with current flowing out.



(a) Structure design and current density simulation.



(b) Current flow simulation.

Fig. 13. Structure design and simulations of switching state -1.

stated above, the three switching states were decomposed into 3D space, and the equivalent impedances under the circumstances of currents flowing in and out are shown in TABLE III and TABLE IV.

TABLE III
EQUIVALENT RESISTANCES UNDER THREE SWITCHING STATES IN 3D SPACE

| Switching states | $R_{dc}(\Omega)$ | $R_{ac}(\Omega)$ |
|---|---|---|
| 1 | $4.8175\times10^{-5}$ | 0.021715 |
| 0(current flowing out) | $4.5292\times10^{-5}$ | 0.022469 |
| 0(current flowing in) | $4.5325\times10^{-5}$ | 0.022761 |
| -1 | $4.8048\times10^{-5}$ | 0.020502 |

TABLE IV
CALCULATED VALUES OF STRAY INDUCTANCES UNDER THREE SWITCHING STATES

| Switching states | $L_{dc}$(nH) | $L_{ac}$(nH) |
|---|---|---|
| 1 | 132.39 | 117.57 |
| 0(flowing out) | 121.75 | 95.04 |
| 0(flowing in) | 122.52 | 96.89 |
| -1 | 131.68 | 118.13 |

TABLE V
POWER LOSSES OF THREE COMMUTATION PATHS

| Switching states | Pdc(W) | Pac(W) |
|---|---|---|
| 1 | 9.12 | 40.09 |
| 0(flowing out) | 8.57 | 42.51 |
| 0(flowing in) | 8.57 | 43.06 |
| -1 | 9.09 | 38.79 |

It can be seen from TABLE IV that using the middle inlet can result in complete mirror circulation paths under all of the switching states. In addition, appropriate symmetric parameters can be obtained.

Put these impedance values into equations (6), (7) and (8), and the power losses of the three commutation paths corresponding to the three switching states with the motor under the rated conditions can be acquired as shown in TABLE V.

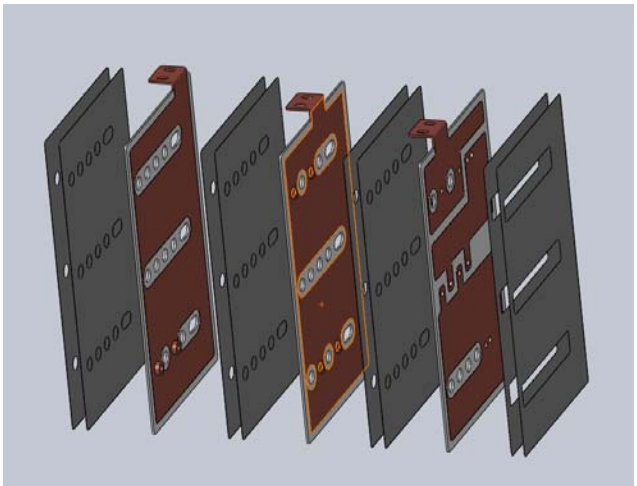
Use these values in the busbar design, and the structure and finished product can be realized as shown in Fig. 14.

## IV. SIMULATION AND EXPERIMENT

In the former sections, the equivalent circuit and equivalent model of a NPC three-level inverter were built, the stray inductances were decomposed and calculated in 3D coordinates, and the laminated busbar was designed based on the proposed theory. In this section, some simulations and experiments, including double pulse testing experiments and 1 MW NPC three-level busbar temperature rise simulations and experiments, will be conducted to validate the theory.

### *A. Double Pulse Testing Experiment of Stray Inductance*

The target of this experiment is to show whether the stray inductance of the laminated busbar design based on supersymmetric mirror circulation 3D cubical thermal model conforms to the theoretical analysis. The judgment standards include whether the stray inductance is similar, whether the reverse recovery current of the diode is appropriate, and



(a) The structure model.

(c) The finished product.

Fig. 14. The structure and finished product.

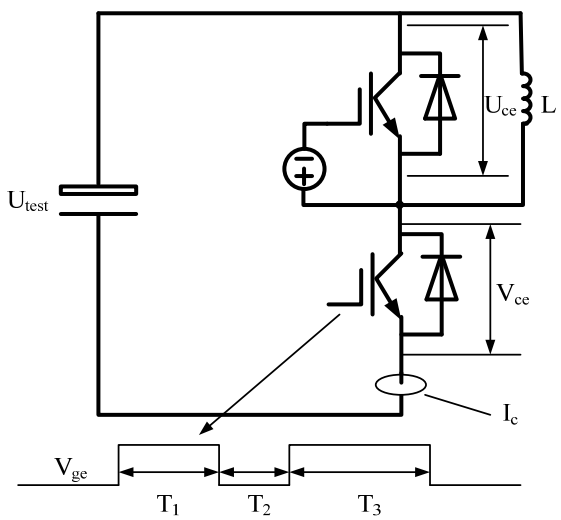



Fig. 15. Structure of double pulse testing experiment.

whether the voltage spike during turn-off is suitable. The structure of this experiment is shown in Fig. 15.

In Fig. 15, the lower IGBT and upper diode are the testing objects. $V_{ce}$, $I_c$ and $V_{ge}$ were captured with a High Voltage Isolation Probe, a Roche Coil Current Probe and an Oscilloscope Probe, respectively. A negative voltage is

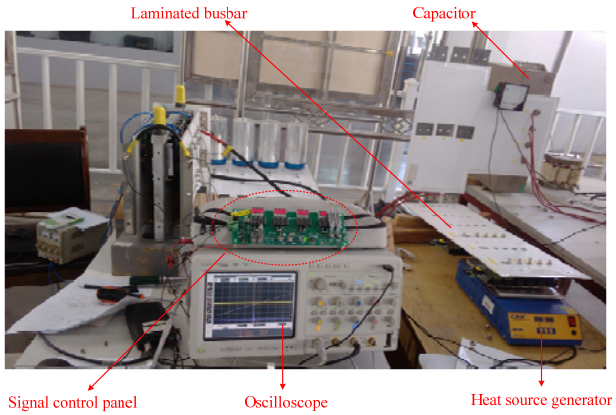



Fig. 16. Platform of double pulse testing experiment.

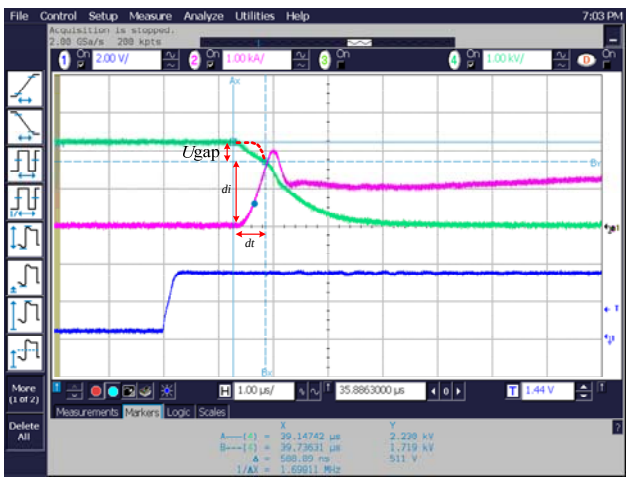



Fig. 17. Diagram of stray inductance calculation principle.

placed on the gate of the upper IGBT to keep it turned off, and only the freewheeling diode works. The experimental platform is shown in Fig. 16.

When the lower IGBT turns on, $I_c$ starts to increase immediately, and at the same time the freewheeling diode of the upper IGBT stays in the reverse recovery state with no blocking-off capability, which means that $U_{ce}$=0. With the increase of $I_c$, the direction of the induction voltage on the stray inductance is opposite the direction of the DC-bus voltage $U_{test}$. Therefore, there is a voltage gap in the tested waveform of $V_{ce}$ on the lower IGBT, which is shown in Fig. 17 and marked with a red dotted line. The reason for the voltage gap is that the reverse voltage generated by the stray inductance counteracts some of the DC-bus voltage. That is to say, the voltage gap is the induction voltage of the stray inductance, which satisfies equation in (1), and when $U_{gap}$ and $\frac{di}{dt}$ are put into the equation, the stray inductance $L_{stray}$ can be determined.

Based on the above principle and three kinds of switching states, the experiment results can be obtained as follows:

Fig. 18 shows a complete test waveform from double

Fig. 18. Full waveform of double pulse test.

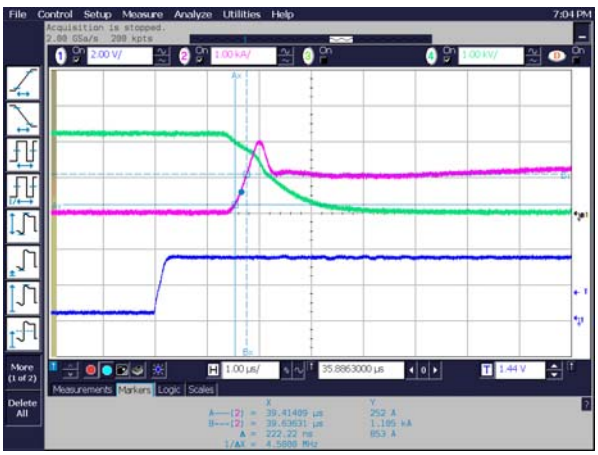


Fig. 19. Waveform of switching state 1.

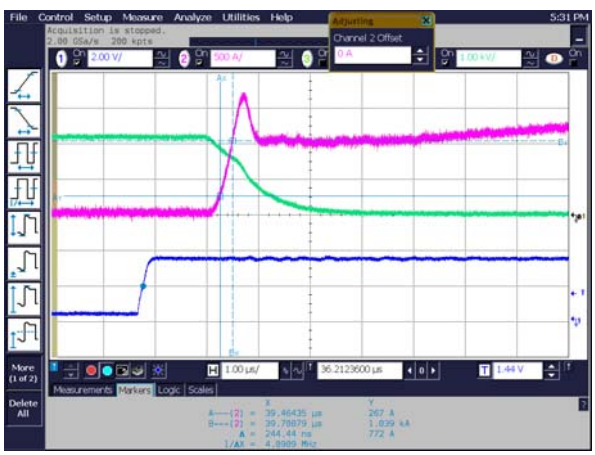


Fig. 20. Waveform of switching state 0 with current flowing out.

testing, and the double testing waveforms above are the results of three circulation paths under three switching states, whose calculation results are as follows:

It can be seen from Fig. 19 that the stray inductance of switching state 1 is:

$$L_{stray-1} = \frac{530}{853} \times 222.2 \approx 138.1\,\text{nH}$$

Fig. 21. Waveform of switching state 0 with current flowing in.

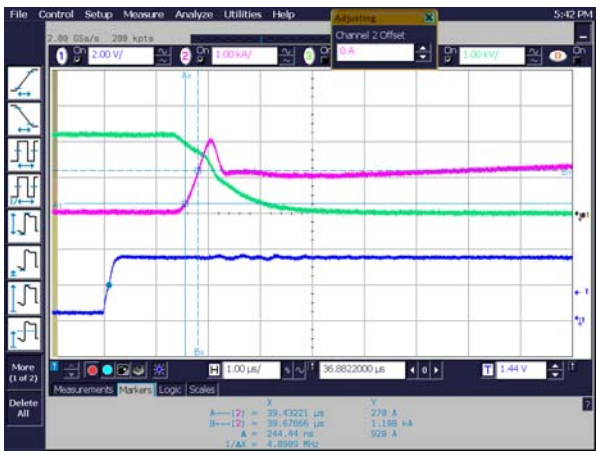


Fig. 22. Waveform of switching state -1.

The calculated value has a 4.1% error rate.

It can be seen from Fig. 20 that the stray inductance of switching state 0 with current flowing out is:

$$L_{stray-0-in} = \frac{400}{772} \times 244.4 \approx 126.6\,\text{nH}$$

The calculated value has a 3.8% error rate.

It can be seen from Fig. 21 that the stray inductance of switching state 0 with current flowing in is:

$$L_{stray-0-out} = \frac{410}{845} \times 255.6 \approx 124.0\,\text{nH}$$

The calculated value has a 1.2% error rate.

It can be seen from Fig. 22 that the stray inductance of switching state -1 is:

$$L_{stray--1} = \frac{510}{928} \times 244.4 \approx 134.1\,\text{nH}$$

The calculated value has a 1.8% error rate.

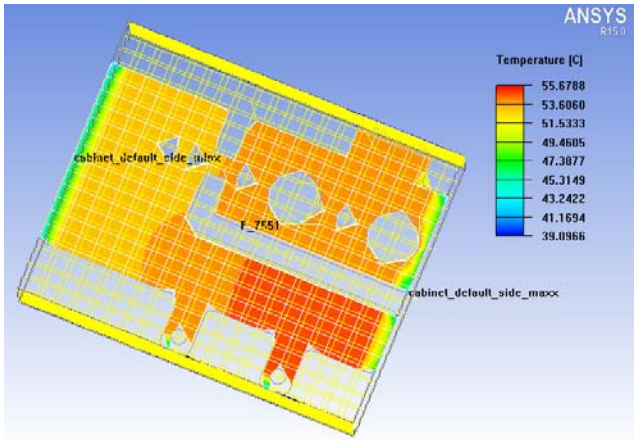
The actual values of the stray inductance have a 2.7% average error rate with respect to the calculated ones decomposed in the 3D space coordinate system in Section III. This shows the accuracy and effectiveness of the proposed model in the stray inductance analysis and the design of the laminated busbar.


Fig. 23. Experiment platform of 1MW NPC three-level inverter.

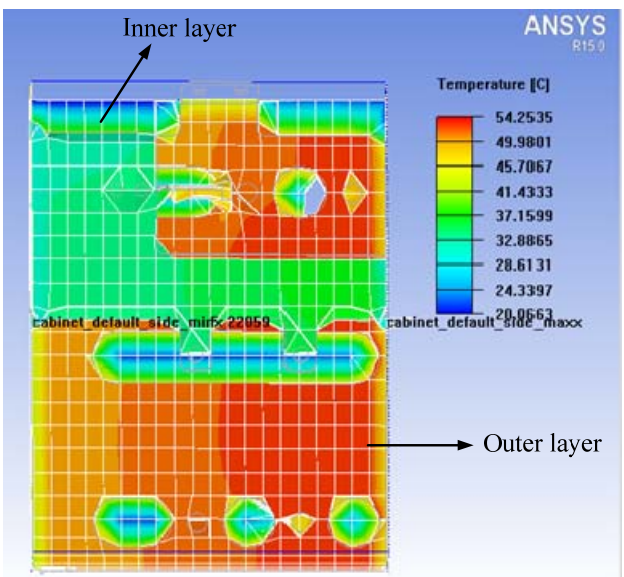
### *B. Performance Simulation and Experiment of a 1 MW NPC Three-Level Inverter Busbar*

In this section, a thermal simulation of the laminated busbar was carried out to analyze the temperature rise. Then, a 1MW NPC three-level inverter was used to drive the asynchronous motor mentioned above to conduct a performance experiment to demonstrate the heat equilibrium and over-voltage performance. The experiment platform is shown in Fig. 23.

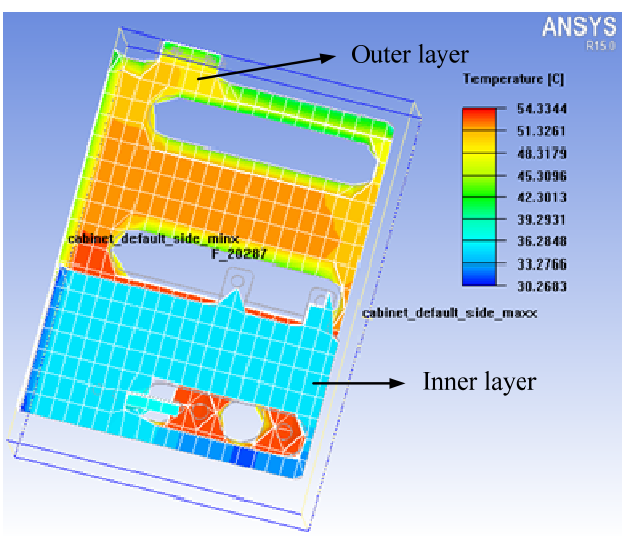
*1) Performance of Heat Equilibrium:* It can be seen from Fig. 24 (a) that the maximum temperature difference in the temperature simulation of switching state 1 is less than 5℃, except for the edges exposed to the air, and that the highest temperature is below 55.7℃. It can be seen form Fig. 24 (b) that the maximum temperature differences in the temperature simulation of switching state 0 is less than 6℃ in outer layer and less than 4℃ in inner layer, except for the edges exposed to the air, and that the highest temperature is below 54.2℃. It can be seen form Fig. 24 (c) that the maximum temperature differences in temperature simulation of switching state -1 is less than 6℃ in outer layer and less than 3℃ in inner layer, except for the edges exposed to the air, and that the highest temperature is below 54.3 ℃. The simulations above expresses good temperature uniformity and provides a reference for the busbar design to ensure that the three circulation paths have the same heat equilibrium. It can be known by analyzing Fig. 25(a) that the laminated busbar of phase B has a uniform energy flow and a good heat equilibrium, which is an isothermal surface with the highest temperature, basically below 49℃. Meanwhile, the highest temperature area is the contact area. If this is ignored, the simulation result will have an error rate less of than 8% compared with the theoretical analysis results. A conclusion can be drawn by analyzing the laminated busbars of three phases in Fig. 25(b) that busbars designed based on the same theory have a high precision in terms of consistency and that all of the temperatures are under the highest 49℃ isothermal surface, which demonstrates the accuracy and feasibility of the theoretical analysis.




(a) Temperature simulation of switching state 1.

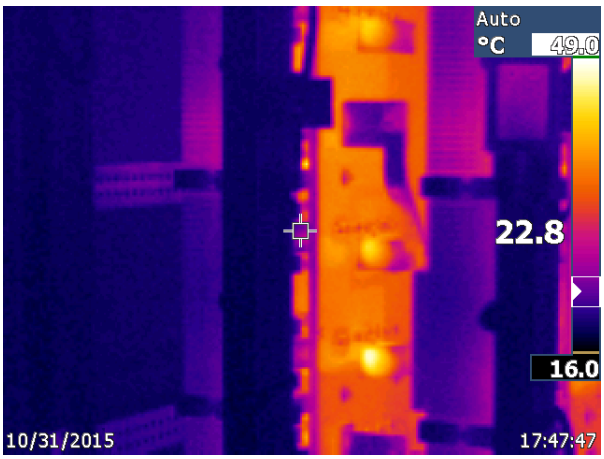



(b) Temperature simulation of switching state 0.

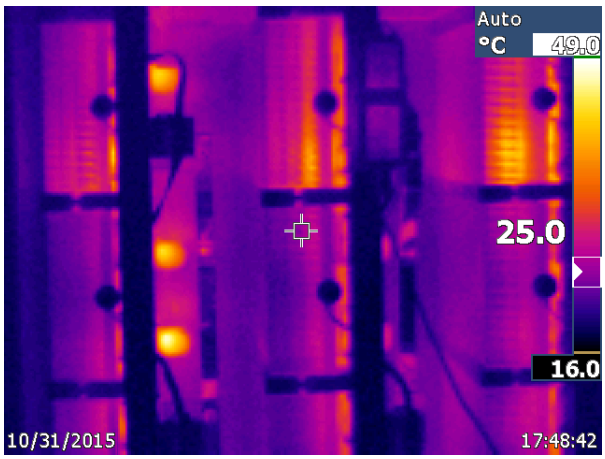



(c) Temperature simulation of switching state -1.

Fig. 24. Heat equilibrium simulation of laminated busbar.

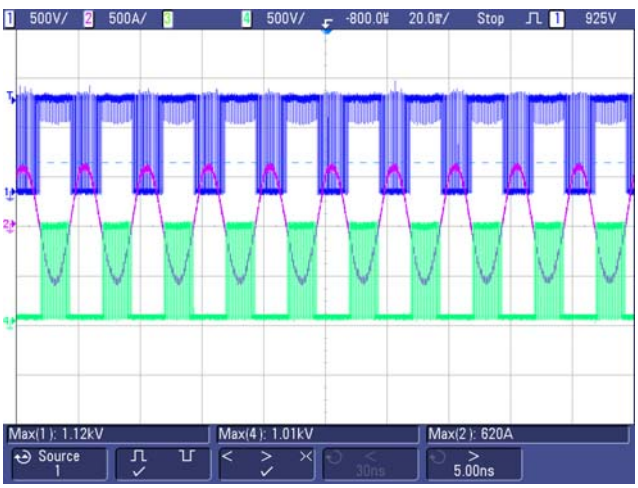



(a)Temperature rise of laminated busbar in phase B.

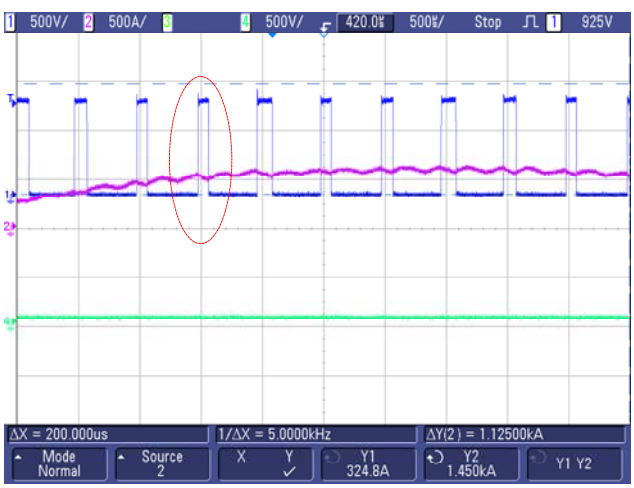



(b) Temperature rise of laminated busbar in three phases.

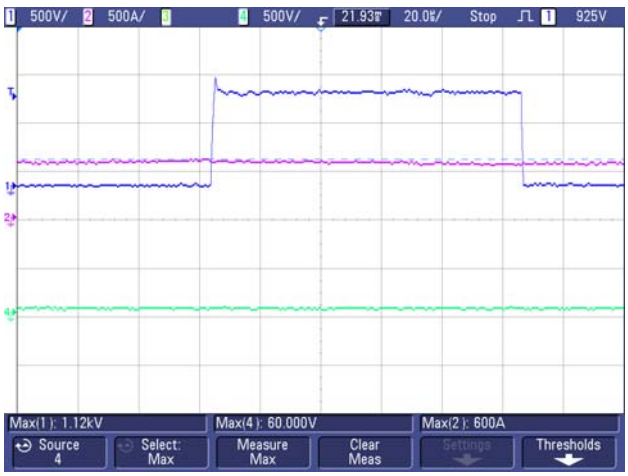
Fig. 25. Temperature rises of laminated busbar with inverter working under rated conditions.




(a) Working waveforms of IGBT in phase B bridge arm.




(b) Expanded view.




(c) Enlarged view.

Fig. 26. Overvoltage suppression performance of laminated busbar in phase B bridge arm.

*2) Overvoltage Suppression Performance:* A test was carried out with the motor running under the rated conditions, and the IGBT in the phase B bridge arm was taken as research object to demonstrate its over-voltage condition. The results are shown in Fig. 26.

It can be known by analyzing Fig. 26 that the maximum overvoltage using the proposed laminated busbar is 230V, and that the maximum withstanding voltage of the IGBT is 1330V, which is far less than the rated withstanding voltage of 1700V. The overvoltage coefficient is 1.21 times, which shows an excellent overvoltage suppression performance.

## V. CONCLUSION

A supersymmetric mirror circulation 3D cubical thermal model was proposed in this paper. On the basis of this, a laminated busbar was decomposed in 3D space to calculate the equivalent resistance and stray inductance in each

commutation loop. During the design of the laminated busbar, maintaining the approximate symmetry of the stray inductance and resistance in each commutation loop, and a good heat equilibrium and a low stray inductance performance can be realized by mutual elimination of the magnetic fields generated by different circulation loops. Based on the proposed theory, the stray inductance and impedance calculation provides a precise theoretical support for busbar design. Finally the feasibility and effectiveness of the theoretical analysis was verified by both double pulse testing experiments and 1 MW NPC three-level busbar temperature rise simulations and experiments.

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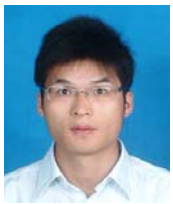

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