JPE 16-6-12

http://dx.doi.org/10.6113/JPE.2016.16.6.2109
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

# A Neutral-Point Voltage Balance Controller for the Equivalent SVPWM Strategy of NPC Three-Level Inverters

Jianguo Lyu†, Wenbin Hu*, Fuyun Wu**, Kai Yao*, and Junji Wu***

†,*School of Automation, Nanjing University of Science and Technology, Nanjing, China
**College of Mechanical and Electrical Engineering, Sanjiang University, Nanjing, China
***School of Energy and Power Engineering, Nanjing University of Science and Technology, Nanjing, China

## Abstract

Based on the space vector pulse width modulation (SVPWM) theory, this paper realizes an easier SVPWM strategy, which is equivalently implemented by CBSPWM with zero-sequence voltage injection. The traditional SVPWM strategy has no effect on controlling the neutral-point voltage balance. In order to solve the neutral-point voltage unbalance problem for neutral-point-clamped (NPC) three-level inverters, this paper proposes a neutral-point voltage balance controller. The proposed controller realizes controlling the neutral-point voltage balance by dynamically calculating the offset superimposed to the three-phase modulation waves of an equivalent SVPWM strategy. Compared with the traditional SVPWM strategy, the proposed neutral-point voltage balance controller has a strong ability to balance the neutral-point voltage, has good steady-state performance, improves the output waveforms quality and is easy for digital implementation. An experiment has been carried out on a NPC three-level inverter prototype based on a digital signal processor-complex programmable logic device (DSP-CPLD). The obtained experimental results verify the effectiveness of the proposed neutral-point voltage balance controller.

**Key words:** Neutral-point voltage balance, Output harmonics, Space vector pulse width modulation (SVPWM)

## I. INTRODUCTION

Multi-level inverters have been widely used in high power and medium voltage conversions [1], [2]. As a result, their topologies and control strategies have been the focus of a lot of research. Compared with two-level inverters, multi-level inverters have better performances, such as lower voltage derivatives (d$v$/d$t$), reduced voltage stress on power switching devices, and lower total harmonic distortion (THD) of output waveforms [3]-[10]. Akira Nabae proposed a new neutral-point-clamped (NPC) pulse width modulation (PWM) inverter in 1980, which is a typical topology for three-level inverters [11], as shown in Fig. 1. Among various PWM strategies for three-level inverters in industrial applications, space vector pulse width modulation (SVPWM) is preferred [12]. When compared with carrier-based sinusoidal PWM (CBSPWM), the SVPWM strategy has a higher dc bus voltage utilization [12]-[15], which is suitable for digital signal processor (DSP) implementation. Based on the relationship between the space vector and the carrier modulation of two-level inverters, Ref. [16] presents a similar equivalence between the phase disposition carrier and the space vector modulation strategies for multilevel inverters, which is the same as the phase disposition modulation, which has the lowest THD [17].

For NPC three-level inverters, in order to realize that the line voltage of the output leg contains five-levels and that the phase voltage of the output leg contains three-levels, this circuit uses two dc bus capacitors in series. Ideally, the voltage on each capacitor is equal to half of the dc bus voltage. However, due to capacitance errors, different parameters of the switching devices, unbalanced three-phase operation and so on [8], the neutral-point voltage unbalance problem exists.

Manuscript received Aug. 10, 2015; accepted Jul. 20, 2016
Recommended for publication by Associate Editor Rae-Young Kim.
†Corresponding Author: lvgd2008@163.com
Tel: +86-025-84303113,Fax: +86-025-84303113, NUST
*School of Automation, Nanjing Univ. of Science & Tech., China
**College of Mechanical & Electrical Eng., Sanjiang University, China
***School of Energy & Power Eng., Nanjing Univ. of Sci. & Tech., China

It increases the voltage stress of switching devices, and influences the output waveform quality [9], [18], [19], Even worse, if the neutral-point voltage unbalance problem becomes serious, it may damage switching devices and magnetic components, and prevent the system from working normally.

Therefore, to solve this problem, many methods have been proposed [5], [6], [8]-[10], and [19]-[33]. An optimized modulation strategy that balances the neutral-point voltage is proposed in [5], [6], [23], which modifies the dwell time of the positive and negative small vectors by correctly selecting other vectors. Those do not have an impact on the neutral-point voltage when they the small vectors. In [9], [20], [27], [31], modified zero-sequence voltage strategies are proposed to control the neutral-point voltage balance. Ref. [9] proposes a control strategy based on SVPWM by injecting zero-sequence voltage which is calculated by using an optimal search and interpolation method to achieve the neutral-point voltage balance. However, its algorithm is complex and not easy to implement. In [22], [24], [25], novel modified SVPWM strategies are proposed to solve the neutral point voltage problem. In [30], a novel controller is proposed by intentionally re-injecting a third-harmonic NP current pattern with a gain modification. Ref. [32] uses a neutral-point voltage balance controller based on SVPWM by modifying the angle of the reference vectors to balance the neutral-point voltage. However, the parameter design of its controller has not been presented. Based on the CBSPWM strategy, an optimal controller using two modulation waveforms per phase is presented in [33]. However, its drawbacks are an increased switching frequency and an increased THD of the output waveforms [33], which results in the need for extra filters. Ref. [34] proposes a new average d-q model and a control approach with a carrier-based PWM implementation for VIENNA-type rectifiers, which controls the neutral-point voltage balance. Ref. [35] proposes a new modulation strategy, which maintains the current balance of the intermediate link inductors based on available redundant space vector selections. In [36][37], a simple neutral-point voltage regulator for NPC three-level inverters is presented, which uses a multiple-carrier sine-triangle modulator in conjunction with a closed-loop controller for neutral-point regulation.

The objective of this paper is to propose a neutral-point voltage balance controller for the equivalent SVPWM strategy, which is implemented by CBSPWM with zero-sequence voltage injection for NPC three-level inverters. Based on an analysis of the neutral-point voltage unbalance, the average neutral-point voltage module is derived in this paper. In addition, the neutral-point voltage balance controller is designed in this paper, which dynamically calculates the offset value superimposed to the three-phase modulation waves. Therefore, the neutral-point voltage balance control can be realized. According to the experimental analysis presented in this paper, the designed neutral-point voltage balance controller has a strong ability to balance the neutral-point voltage, has good steady-state performance, improves the output waveforms quality, and effectively decreases the ripple value of the neutral-point voltage, when compared with the traditional SVPWM strategy.

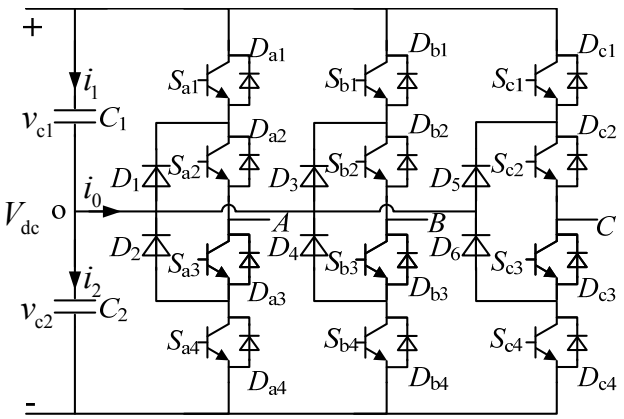



Fig. 1. Main circuit of NPC three-level inverter.

## II. Analysis of the Equivalent Modulation Strategy for SVPWM Implementation

Fig 1 shows the main circuit of a NPC three-level inverter. Taking phase a as an example, its output leg has 4 switches ($S_{a1}$, $S_{a2}$, $S_{a3}$, $S_{a4}$), 4 anti-parallel free-wheeling diodes ($D_{a1}$, $D_{a2}$, $D_{a3}$, $D_{a4}$), and 2 clamping diodes ($D_1$, $D_2$). $V_{dc}$ is the dc bus voltage, supposing that the voltage of the capacitor $C_1$, $C_2$ is equal to $V_{dc}/2$, so that each phase leg outputs three different levels (P, 0, N). Where "P", "0", and "N" represents "$V_{dc}/2$", "0", and "$-V_{dc}/2$", respectively. Each phase has 3 working states. Therefore, this inverter has 27($3^3$) working states in total, which corresponds to 27 space vectors.

When the SVPWM strategy operates, the space vector diagram is divided into 6 main sectors. There are 4 regions in each main sector, as shown in Fig. 2. In addition, there are 27 space voltage vectors in the space vector diagram, which including 6 big vectors, 6 medium vectors, 12 small vectors and 3 zero vectors.

In order to realize the SVPWM strategy more easily, the SVPWM can be equivalently implemented by a CBSPWM with a zero-sequence voltage injection. Ideally, suppose that the carrier amplitude is unity. Then the three phase sinusoidal modulation waves for CBSPWM can be expressed as:

$$\begin{cases} u_a = m\sin(\omega t) \\ u_b = m\sin(\omega t - 2\pi/3) \\ u_c = m\sin(\omega t + 2\pi/3) \end{cases} \quad (1)$$

Where $m$ is the modulation ratio were $0<m<1$, and $\omega$ is the

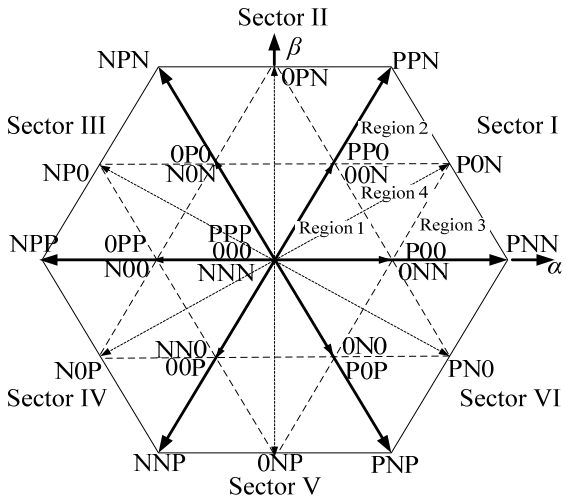



Fig. 2. The space vector diagram of NPC three-level inverter.

angular frequency of the modulation waves.

In a line cycle, $\max(u_a, u_b, u_c)$ and $\min(u_a, u_b, u_c)$ are defined as the maximum and minimum instantaneous values of the three-phase sinusoidal modulation waves, which can be expressed as:

$$\max(u_a,u_b,u_c)=\begin{cases}u_a, & \pi/6<\omega t\le 5\pi/6\\ u_b, & 5\pi/6<\omega t\le 3\pi/2\\ u_c, & 0\le\omega t\le\pi/6 \text{ or } 3\pi/2<\omega t\le 2\pi\end{cases} \tag{2}$$

$$\min(u_a,u_b,u_c)=\begin{cases}u_a, & 7\pi/6<\omega t\le 11\pi/6\\ u_b, & 0\le\omega t\le\pi/2 \text{ or } 11\pi/6<\omega t\le 2\pi\\ u_c, & \pi/2<\omega t\le 7\pi/6\end{cases} \tag{3}$$

The zero-sequence voltage is shown as follows:

$$u_z=-\frac{\max(u_a,u_b,u_c)+\min(u_a,u_b,u_c)}{2} \tag{4}$$

Therefore, using the equivalent SVPWM strategy, the expressions of its three-phase modulation waves can be expressed as:

$$\begin{cases}u_{az}=u_a+u_z\\ u_{bz}=u_b+u_z\\ u_{cz}=u_c+u_z\end{cases} \tag{5}$$

From (1)-(5), $u_{az}, u_{bz}, u_{cz}$ can be derived as:

$$u_{az}=\begin{cases}\sqrt{3}m\sin(\omega t) & 0\le\omega t<\frac{\pi}{6},\frac{5\pi}{6}\le\omega t<\frac{7\pi}{6},\frac{11\pi}{6}\le\omega t\le 2\pi\\ m\sin(\omega t+\frac{\pi}{6}) & \frac{\pi}{6}\le\omega t<\frac{\pi}{2},\frac{7\pi}{6}\le\omega t<\frac{3\pi}{2}\\ m\sin(\omega t-\frac{\pi}{6}) & \frac{\pi}{2}\le\omega t<\frac{5\pi}{6},\frac{3\pi}{2}\le\omega t\le\frac{11\pi}{6}\end{cases} \tag{6}$$

$$u_{bz}=\begin{cases}\sqrt{3}m\sin(\omega t-\frac{2\pi}{3}) & \frac{\pi}{2}\le\omega t<\frac{5\pi}{6},\frac{3\pi}{2}\le\omega t<\frac{11\pi}{6}\\ m\sin(\omega t-\frac{\pi}{2}) & 0\le\omega t<\frac{\pi}{6},\frac{5\pi}{6}\le\omega t<\frac{7\pi}{6},\frac{11\pi}{6}\le\omega t\le 2\pi\\ m\sin(\omega t-\frac{5\pi}{6}) & \frac{\pi}{6}\le\omega t\le\frac{\pi}{2},\frac{7\pi}{6}\le\omega t<\frac{3\pi}{2}\end{cases} \tag{7}$$

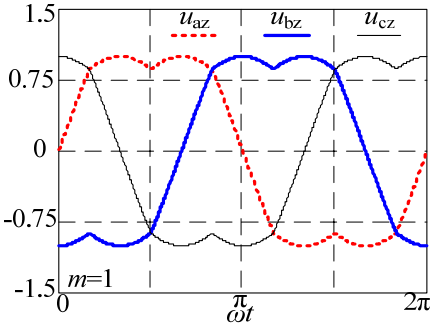



Fig. 3. The waveforms of $u_{az}$, $u_{bz}$, $u_{cz}$ at $m$=1.

$$u_{cz}=\begin{cases}\sqrt{3}m\sin(\omega t+\frac{2\pi}{3}) & \frac{\pi}{6}\le\omega t<\frac{\pi}{2},\frac{7\pi}{6}\le\omega t<\frac{3\pi}{2}\\ m\sin(\omega t+\frac{5\pi}{6}) & \frac{\pi}{2}\le\omega t<\frac{5\pi}{6},\frac{3\pi}{2}\le\omega t<\frac{11\pi}{6}\\ m\sin(\omega t+\frac{\pi}{2}) & 0\le\omega t<\frac{\pi}{6},\frac{5\pi}{6}\le\omega t<\frac{7\pi}{6},\frac{11\pi}{6}\le\omega t\le 2\pi\end{cases} \tag{8}$$

For example, when $m$=1, the three-phase modulation waveforms are shown in Fig. 3.

## III. Neutral-Point Voltage Unbalance Problem

### A. Analysis of Neutral-Point Voltage Unbalance

The three-phase load currents are defined as:

$$\begin{cases}i_a=I_m\sin(\omega t-\varphi)\\ i_b=I_m\sin(\omega t-2\pi/3-\varphi)\\ i_c=I_m\sin(\omega t+2\pi/3-\varphi)\end{cases} \tag{9}$$

Where $I_m$ is the amplitude of the phase load current, and $\varphi$ is the load power factor angle.

In a switching cycle, the duty cycle of the "0" state for each leg output level can be expressed as:

$$D_{xo}=\begin{cases}1-u_{xz} & u_{xz}\ge 0\\ 1+u_{xz} & u_{xz}<0\end{cases} \tag{10}$$

Where $D_{xo}$(x=a,b,c) represents the duty cycle of the "0" state for each output leg level in a switching cycle. $u_{xz}$(x=a,b,c) represents the three-phase modulation waves of the equivalent SVPWM strategy.

Define $i_o$ so that it represents the average value of the neutral-point current in a switching cycle ($T_s$), and $i_o$ is approximately the instantaneous neutral-point current, which flows out from the neutral-point O, as shown in Fig. 1. In addition, $i_o$ can be expressed as:

$$i_o=D_{ao}i_a+D_{bo}i_b+D_{co}i_c \tag{11}$$

In Fig. 1, the relationship among $i_o$, $i_1$ and $i_2$ is:

$$\begin{cases}i_1=C\,dv_{c1}/dt\\ i_2=C\,dv_{c2}/dt\\ i_o=i_1-i_2\end{cases} \tag{12}$$

Where $v_{c1}$ and $v_{c2}$ are the instantaneous voltages of the capacitors $C_1$ and $C_2$; $i_1$ and $i_2$ are the instantaneous currents of the capacitors $C_1$ and $C_2$; and $C$ is the capacitance value of $C_1$

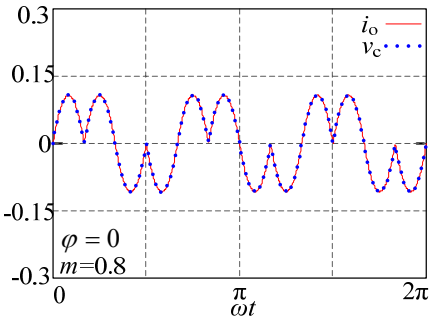



Fig. 4. Curves of $i_o$ and $v_c$.

and $C_2$.

Define $v_c$ so that it represents the voltage difference between $v_{c1}$ and $v_{c2}$. As a result, $v_c$ can be expressed as:

$$v_c = v_{c1} - v_{c2} \tag{13}$$

From (12)-(13), the expression of $v_c$ can be derived as:

$$v_c = \frac{1}{C}\int_0^{T_s} i_0 dt = \frac{T_s}{C} i_0 \tag{14}$$

Where $T_s$ is a switching cycle.

Substituting (11) into (14), (14) can be expressed as:

$$v_c = \frac{T_s}{C}(D_{ao} i_a + D_{bo} i_b + D_{co} i_c) \tag{15}$$

According to (15), when $I_m$, $T_s$ and $C$ are normalized, the curves of $v_c$ and $i_o$, are shown in Fig. 4.

From Fig. 4, it can be seen that the wave shapes of $i_o$ and $v_c$ are same. They both fluctuate at three times the line frequency in a line cycle, not considering the values. The fluctuation of the neutral-point voltage is caused by a fluctuation of the neutral-point current.

### *B. The Influence of the Space Vector on the Neutral-Point Voltage*

The space vector classification is described in Section II. When the zero vector operates, the neutral-point current is zero. Therefore, the zero vector has no effect on the neutral-point voltage. When the big, medium and small vectors operate, the influence of space vectors on the neutral-point voltage can be obtained.

The impact of the load currents on the neutral-point voltage is shown in Fig. 5, where the big vector [PPN], medium vector [P0N], positive small vector [PP0], and negative small vector [00N] operate.

Where $i_a$, $i_b$, $i_c$ represents the three-phase load currents respectively, $v_o$ represents the neutral-point voltage, $i_o$ represents the neutral-point current.

Suppose the three-phase loads are symmetrical, as shown in Fig. 5(a). When the big vector [PPN] operates, the three-phase loads are not connected with the neutral-point O. Therefore, the load currents have no effect on the neutral-point voltage. From Fig. 5(b), it can be seen that the flow direction of $i_b$ cannot be determined when the medium vector [PON] is operating. Therefore, its influence on the neutral-point voltage

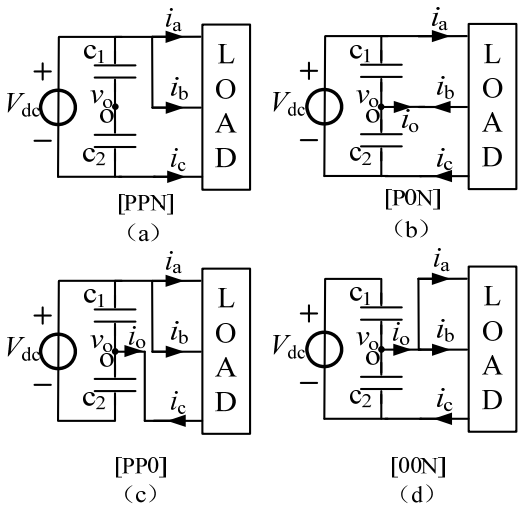



Fig. 5. The impact on the neutral-point voltage of load currents.

cannot be determined. From Fig. 5(c), it can be seen that when the positive small vector [PP0] operates, $i_o$ is equal to $-i_c$, and $i_c$ flows into the neutral-point O, and $v_o$ increases. When the negative small vector [00N] operates in Fig. 5(d), it can be seen that $i_o$ flows out of the neutral-point O, and $v_o$ decreases.

Comparing Fig. 5(c) with Fig. 5(d), it can be seen that when the positive small vector [PP0] and the negative small vector [00N] operate, their impact on $v_o$ is opposite. Therefore, the neutral-point voltage unbalance problem can be solved by selecting proper dwell times for the positive and negative small vectors.

## IV. Design of a Neutral-Point Voltage Balance Controller

Based on the analysis of the neutral-point voltage unbalance, and the influence of the space vector on the neutral-point voltage in Section III, a neutral-point voltage balance controller is designed in this section.

### *A. The Principle of Neutral-Point Voltage Balance Control*

When an equivalent SVPWM strategy that is implemented by a CBSPWM with zero-sequence voltage injection is operated, a block diagram of the neutral-point voltage balance control is shown in Fig. 6. It can be seen that the neutral-point voltage balance is controlled by a proportional controller (P controller), which dynamically calculates the offset value superimposed to the three-phase modulation waves based on the equivalent SVPWM strategy.

Therefore, the following equations must be met:

$$\begin{cases} u_{az}' = u_{az} + u_0 \\ u_{bz}' = u_{bz} + u_0 \\ u_{cz}' = u_{cz} + u_0 \end{cases} \tag{16}$$

Where $u_{az}$, $u_{bz}$, and $u_{cz}$ represent the three-phase modulation

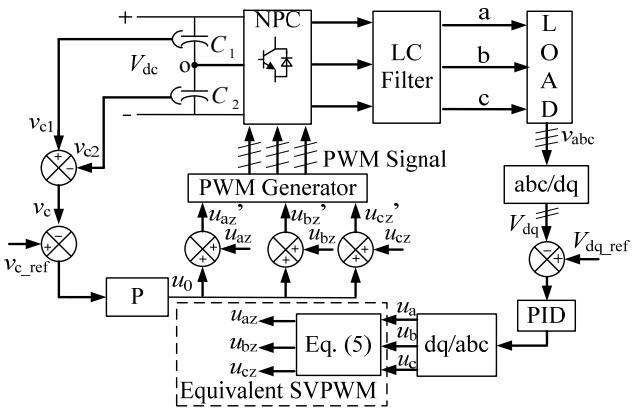



Fig. 6. Block diagram of the neutral-point voltage balance control.

waves without the proposed P controller. $u_{az}$', $u_{bz}$', and $u_{cz}$' represent the modified three-phase modulation waves with the proposed P controller. $v_{c+}$ and $v_{c-}$ represent the positive and negative triangle carrier waves, respectively. $u_0$ represents the offset value superimposed to the three-phase modulation waves.

When the equivalent SVPWM strategy operates, taking Region 1 of Sector I as an example, Fig. 7 shows the modification of the three-phase modulation waves. Define $v_{c\_ref}$=0, and suppose $v_c$>0. According to the influence of the space vector on the neutral-point voltage, the dwell time of [P00] should be increased, and the dwell time of [00N] should be decreased. As a result, by (16), the three-phase modulation waves are modified, and the neutral-point voltage balance can be achieved.

In order to dynamically calculate the offset value $u_0$ for controlling the neutral-point voltage balance, the P controller must be designed.

### *B. Design of the Neutral-Point Voltage Balance Controller*

With the P controller for the neutral-point voltage balance, the duty cycle of the "0" state for each leg output level can be obtained by:

$$D_{xo}' = \begin{cases} 1-u_{xz}' & u_{xz}' \geq 0 \\ 1+u_{xz}' & u_{xz}' < 0 \end{cases} \tag{17}$$

Where $D_{xo}$'(x=a,b,c) represents the duty cycle of the "0" state for each leg output level.

Therefore, from (11), with the P controller, the average value of $i_o$ can be derived by:

$$I_o^{avg} = \frac{1}{T_{line}/3}\int_0^{T_{line}/3} i_o dt = I_{oa}^{avg} + I_{ob}^{avg} + I_{oc}^{avg} \tag{18}$$

Where $T_{line}$ represents the line cycle time. $I_{oa}^{avg}$, $I_{ob}^{avg}$, $I_{oc}^{avg}$ represent the average value of $i_o$ for each phase:

$$I_{oa}^{avg} = \frac{1}{T_{line}/3}\int_0^{T_{line}/3} (D_{ao}' i_a) dt \tag{19}$$

$$I_{ob}^{avg} = \frac{1}{T_{line}/3}\int_0^{T_{line}/3} (D_{bo}' i_b) dt \tag{20}$$

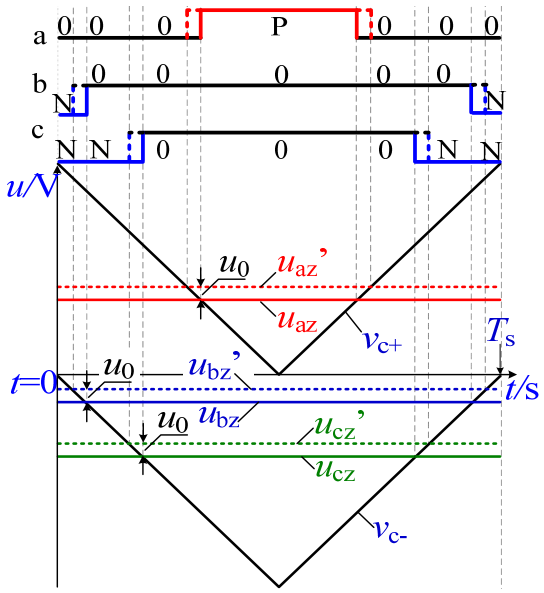



Fig. 7. Modification for the equivalent modulation waves.

$$I_{oc}^{avg} = \frac{1}{T_{line}/3}\int_0^{T_{line}/3} (D_{co}' i_c) dt \tag{21}$$

From (6)-(9), (16)-(17), and (19), the average value of $i_o$ for phase a can be obtained by:

$$\begin{aligned} I_{oa}^{avg} = \frac{-3I_m}{2\pi}\{\cos(\varphi)[&\frac{5\sqrt{3}\pi}{24}m + \frac{m}{8} - \frac{\sqrt{3}}{4}m\theta_0 + \frac{3\sqrt{3}}{8}m\sin(2\theta_0) \\ &+ \frac{3u_0}{2}\cos(\theta_0) + \frac{m}{8}\cos(2\theta_0) + \frac{\sqrt{3}u_0}{2}\sin(\theta_0)] \\ &+ \sin(\varphi)[\frac{-\pi m}{24} + \frac{\sqrt{3}}{8}m + \frac{\theta_0 m}{4} - \frac{3\sqrt{3}m}{8}\cos(2\theta_0) \\ &+ \frac{3u_0}{2}\sin(\theta_0) + \frac{m}{8}\sin(2\theta_0) - \frac{\sqrt{3}u_0}{2}\cos(\theta_0)]\} \end{aligned} \tag{22}$$

Where:

$$\theta_0 = -\arcsin(\frac{\sqrt{3}u_0}{3m}) \tag{23}$$

As a result, $I_{ob}^{avg}$, $I_{oc}^{avg}$ can be derived, and $I_o^{avg}$ can be expressed as:

$$I_o^{avg} = \frac{-3I_m\cos(\varphi)}{\pi}\{2u_0\cos(\theta_0) + \sqrt{3}m\sin(\theta_0)\cos(\theta_0) - \sqrt{3}m\theta_0\} \tag{24}$$

From (24), it can be seen that the relationship between $u_0$ and $I_o^{avg}$ is non-linear. Therefore, the average neutral-point current module should be linearized. Then the classical control theory can be utilized. $I_o^{avg}$ can be linearized as:

$$I_o^{avg}(u_0) = I_{o\,(u_0=0)}^{avg} + \frac{\partial I_o^{avg}}{\partial u_0}_{(u_0=0)} u_0 \tag{25}$$

Where:

$$\frac{\partial I_o^{avg}}{\partial u_0} = \frac{-6I_m\cos(\varphi)}{\pi}\sqrt{1-\frac{u_0^2}{3m^2}}, \quad |u_0| \leq \sqrt{3}m \tag{26}$$

Therefore, the linearized average neutral-point current module is a first-order module, as follows:

$$I_o^{avg}(u_0) = \frac{-6I_m\cos(\varphi)}{\pi}u_0 \tag{27}$$

From (12)-(13) and (27), the relationship between $v_c$ and $u_0$ can be expressed as:

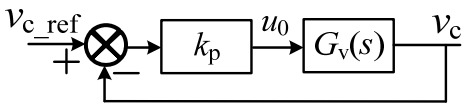



Fig. 8. Simplified control diagram of the neutral-point voltage.

$$\frac{-6I_m\cos(\varphi)}{\pi}u_0 = C\,dv_c/dt \tag{28}$$

By a Laplace transformation of (28), the transfer function of the input offset value $u_0$ to the output $v_c$ is given as:

$$G_V(s) = \frac{v_c(s)}{u_0(s)} = \frac{-6I_m\cos(\varphi)}{\pi}\frac{1}{sC} \tag{29}$$

Thus, the average neutral-point voltage module is given by (29), and the average neutral-point voltage module is a first-order integral system. Therefore, a proportional controller (P controller) can be used for the neutral-point voltage balance. A simplified control diagram of the neutral-point voltage is shown in Fig. 8.

Where $k_p$ is the proportional parameter of the P controller for the neutral-point voltage balance.

From Fig. 8, the open-loop transfer function of the neutral-point voltage control system is given by:

$$G_{OL}(s) = k_p G_v(s) = -k_p\frac{6I_m\cos(\varphi)}{\pi}\frac{1}{sC} \tag{30}$$

Meanwhile, the close-loop transfer function of the neutral-point voltage control system can be obtained as:

$$G_{CL}(S) = \frac{1}{1+1/(k_p G_v(S))} \tag{31}$$

According to the gain characteristic of the system, the gain crossover angular frequency ($\omega_c$) is given by:

$$\omega_c = k_p\frac{-6I_m\cos(\varphi)}{\pi C} \tag{32}$$

The bandwidth of the close-loop transfer function should be smaller than the switching frequency under all conditions [36], and $k_p$ should be designed for the maximum output power. Meanwhile, in order to decrease fluctuations of the neutral-point voltage at three times the line frequency in a line cycle, $\omega_c$ of the control system is selected at $f_s/10$, where $f_s$ is the switching frequency [37], [38]. Therefore, according to the parameters of the system, $k_p$ can be easily obtained as:

$$k_p = -\frac{\omega_c\pi C}{6I_m\cos(\varphi)} = -0.516 \tag{33}$$

Bode plots of $G_V(s)$ and $G_{OL}(s)$ are shown in Fig. 9.

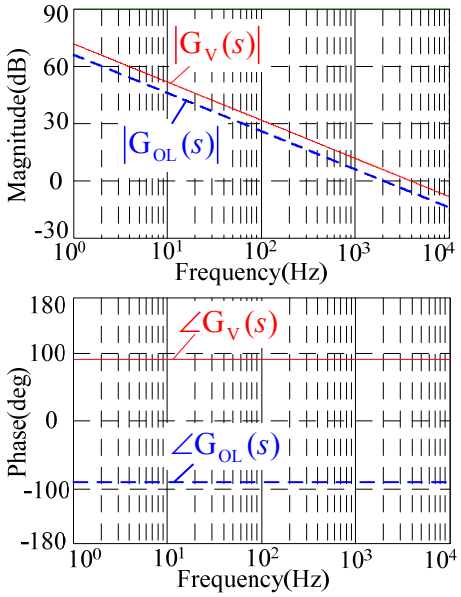



Fig. 9. The bode plots of $G_V(s)$ and $G_{OL}(s)$.

## V. Experimental Verification

In order to demonstrate the validity of the proposed P controller, a prototype of a NPC three-level inverter has been built and tested in the lab. It is based on a digital signal processor and complex programmable logic device (DSP-CPLD).

The specifications of the prototype are as follows:

DC bus voltage: $V_{dc}$=200V,

DC bus capacitors: $C_1$=$C_2$=150uF,

Switching frequency: $f_s$=20kHz,

Output power: $P_o$=200W,

Digital Process Unit: TMS320F28335 DSP,

Logical Driving Unit: EPM1270T(CPLD),

Power switch module: IGBT FZ06NPA070FP,

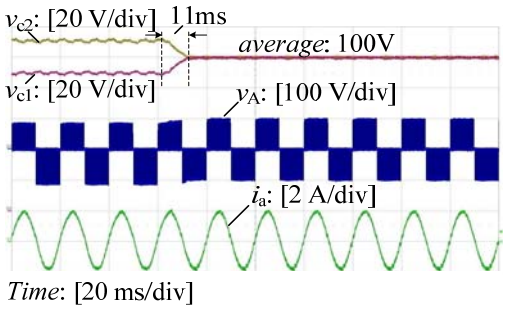
Output phase filter: L: 1.5mH, C: 10uF,

A resistor is parallel to capacitor $C_1$ of the NPC three-level inverter in Fig. 1. Therefore, a neural-point voltage unbalance appears. When the equivalent SVPWM strategy operates, the waveforms of $v_{c1}$, $v_{c2}$, $v_A$, $i_a$ are shown in Fig. 10. Where $v_A$ is the leg voltage of phase a, and $i_a$ is the load current of phase a. Before and after the proposed p controller is operated, the different voltage numbers of $v_{c1}$ and $v_{c2}$ are shown in TABLE I.

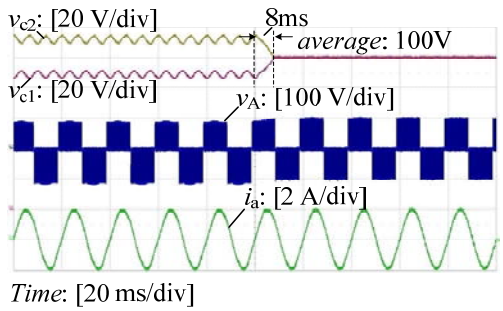
At the different load power factor conditions in Fig. 10, before using the proposed P controller, the neutral-point voltage is unbalanced, and the average value of $v_{c2}$ is higher than that of $v_{c1}$. In a line cycle, the amplitude of $v_A$ in the negative half cycle is higher than that in the positive half cycle. When the proposed P controller operates, the voltage difference between the average value of $v_{c2}$ and that of $v_{c1}$ decreases almost to zero, and the ripple of $v_{c1}$ or $v_{c2}$ becomes very low. The system reaches the steady-state rapidly.

Fig. 11-12 shows a THD analysis of the output waveform with or without P controller at different load power factor conditions. Where $i_{rms}$ and $u_{rms}$ represent the root-mean-square (rms) value of the load current ($i_a$) and voltage ($v_a$) for each phase.

From Fig. 11(a) and Fig. 12(a), it can be seen that when using the P controller, the THD value of $i_a$ decreases from 4.81% to 2.8%, and the THD value of $v_a$ decreases from 4.77% to 2.78% at cos($\varphi$)=1. In addition, at cos($\varphi$)=0.866 as shown in Fig 11(b) and Fig. 12(b), the THD value of $i_a$




(a) cos($\varphi$) = 1.




(b) cos($\varphi$) = 0.866.

Fig. 10. Experimental waveforms.

TABLE I

THE EXPERIMENTAL RESULTS ANALYSIS

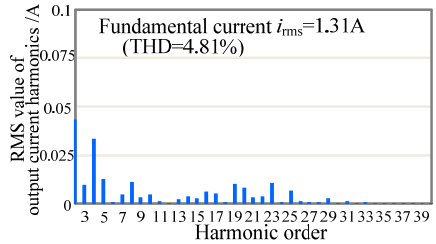
| Load condition | The average voltage difference of $v_{c1}$ and $v_{c2}$ / The ripple of $v_{c1}$ or $v_{c2}$ | |
|---|---|---|
| | Before the proposed P controller | After the proposed P controller |
| cos($\varphi$)=1 | 20V/4.5V | 0V/0.8V |
| cos($\varphi$)=0.866 | 20V/6V | 0V/0.6V |

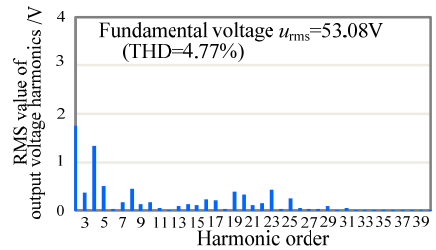
decreases from 4.82% to 2.39%, and the THD value of $v_a$ decreases from 5.52% to 2.77%.

Therefore, under different load power factor conditions, the proposed P controller has a strong ability to control the neutral-point voltage balance. In addition, the output waveforms quality has been effectively improved.

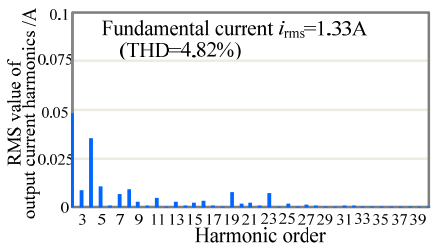
Fig 13-14 show the THD of the output current and the ripple value of $v_{c1}$ under different resistive load conditions with and without the proposed P controller. When using the P controller under different output power conditions, the ripple value of the neutral-point voltage is effectively decreased, and the output waveforms quality is improved.

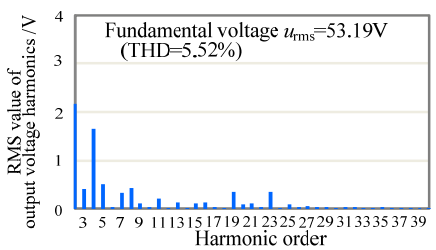
According to the experimental results above, when the neutral-point voltage is unbalanced, the P controller has a strong ability to control the neutral-point voltage balance under different load conditions, which shows a good dynamic response ability and a low steady-state error. It also effectively improves the quality of the output waveforms.



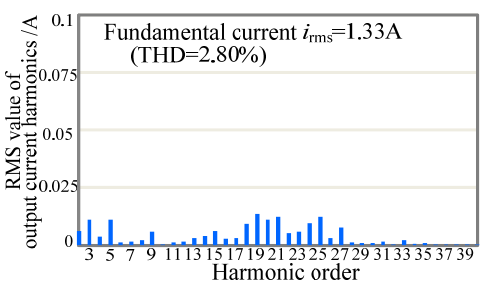

(a) Without P controller at cos($\varphi$)=1.

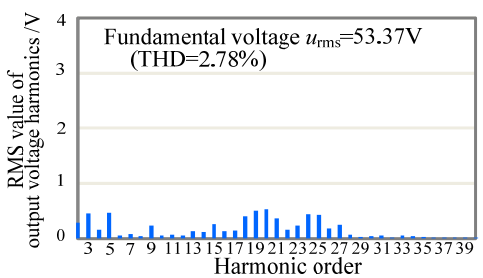


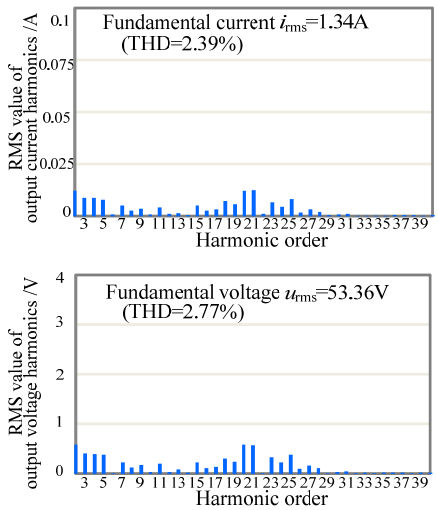

(b) Without P controller at cos($\varphi$)=0.866.

Fig. 11. The THD analysis of output waveforms without P controller.




(a) With P controller at cos($\varphi$) = 1.




(b) With P controller at cos($\varphi$) = 0.866.

Fig. 12. The THD analysis of output waveforms with P controller.

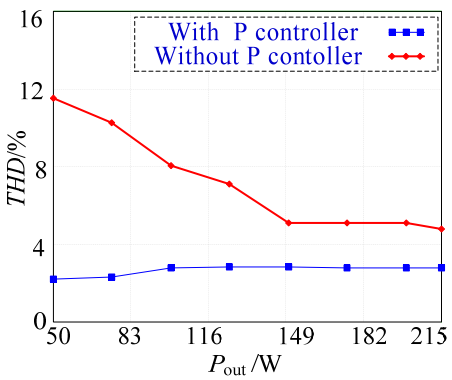



Fig. 13. Measured THD of the output current.

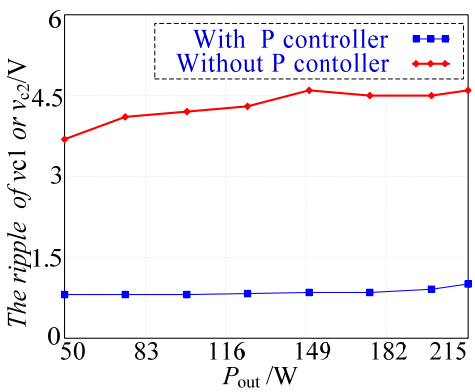



Fig. 14. Measured neutral-point voltage ripple.

## VI. Conclusion

This paper proposes a neutral-point voltage balance controller for the equivalent SVPWM strategy, which is implemented by a CBSPWM with zero-sequence voltage injection for NPC three-level inverters. The principle of the equivalent SVPWM strategy and its expressions for three-phase modulation waves are derived. The neutral-point voltage unbalance, and the influence of space vectors on the neutral-point voltage are analyzed. Based on the derived average neutral-point voltage module, the neutral-point voltage balance controller is designed. It has good steady-state performance, improves the output waveforms quality, and effectively decreases the ripple value of the neutral-point voltage. A theory analysis and experimental results verify the effectiveness of the proposed neutral-point voltage balance controller.

## Acknowledgment

This work was supported by Science and Technology Support Program of Jiangsu Province (BE2013125), Excellent Youth Fund Project of Jiangsu Natural Science Foundation (BK20160086), National Natural Science Foundation of China (51307085).

## References

[1] A. R. Beig, "Synchronized SVPWM algorithm for the overmodulation region of a low switching frequency medium-voltage three-level VSI," *IEEE Trans. Ind. Electron*., Vol. 59, No. 12, pp. 4545-4554, Dec. 2012.

[2] I. Lopez, S. Ceballos, J. Pou, J. Zaragoza, J. Andreu, I. Kortabarria, and V. G. Agelidis, "Modulation strategy for multiphase neutral-point-clamped converters," *IEEE Trans. Power Electron*., Vol. 31, No. 2, pp. 928-941, Feb. 2016.

[3] M. A. Sayed, M. Ahmed, M. G. Elsheikh, and M. Orabi, "PWM control techniques for single-phase multilevel inverter based controlled DC cells," *Journal of Power Electronics*, Vol. 16, No. 2, pp. 498-511, Mar. 2016.

[4] J. S. Lee and K. B. Lee, "Tolerance control for inner open-switch faults of a T-type three-level rectifier," *Journal of Power Electronics*, Vol. 14, No. 6, pp. 1157-1165, Nov. 2014.

[5] J. S. Lee and K. B. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Trans. Power Electron*., Vol. 29, No. 4, pp. 1720-1732, Apr. 2014.

[6] U. M. Choi, J. S. Lee, and K. B. Lee, "New modulation strategy to balance the neutral-point voltage for three-level neutral-clamped inverter systems," *IEEE Trans. Energy Convers*., Vol. 29, No. 1, pp. 91-100, Mar. 2014.

[7] H. G. Jeong, K. B. Lee, S. W. Choi, and W. J. Choi, "Performance improvement of LCL-filter based grid connected-inverters using PQR power transformations," *IEEE Trans. Power Electron*., Vol. 25, No. 5, pp. 1320-1330, May 2010.

[8] U. M. Choi, H. H. Lee, and K. B. Lee, "Simple neutral-point voltage control for three-level inverters using a discontinuous pulse width modulation," *IEEE Trans. Energy Convers*., Vol. 28, No. 2, pp. 434-443, Jun. 2013.

[9] C. C. Wang and Y. D. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Trans. Ind. Electron*., Vol. 57, No.7, pp. 2262-2271, Jul. 2010.

[10] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level

neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron*., Vol. 15, No. 2, pp. 242-249, Mar. 2000.

[11] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Appl*., Vol. IA-17, No. 5, pp.518-523, Sep./Oct. 1981.

[12] J. Chen, Y. He, S. U. Hasan, and J. Liu, "A comprehensive study on equivalent modulation waveforms of the SVM sequence for three-level inverters," *IEEE Trans. Power Electron*., Vol. 30, No. 12, pp. 7149-7158, Dec. 2015.

[13] S. Das and G. Narayanan, "Novel switching sequences for space vector modulated three-level inverters," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 3, pp. 1477-1487, Mar. 2012.

[14] F. A. Ramirez and M. A. Arjona, "An improved SVPWM control of voltage imbalance in capacitors of a single-phase multilevel inverter," *Journal of Power Electronics*, Vol. 15, No. 5, pp. 1235-1243, Sep. 2015.

[15] D. M. Lee, J. W. Jung, and S. S. Kwak, "Simple space vector PWM scheme for 3-level NPC inverters including the overmodulation region," *Journal of Power Electronics*, Vol. 11, No. 5, pp. 688-696, Sep. 2011.

[16] B. P. McGrath, D. G. Holmes, and T. Lipo. "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron*., Vol. 18, No. 6, pp. 1293-1301, Nov. 2003.

[17] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto. "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron*., Vol. 7, No. 3, pp. 497-505, Jul. 1992.

[18] J. Lyu, W. Hu, F. Wu, K. Yao, and J. Wu, "A new DPWM method to suppress the low frequency oscillation of the neutral-point voltage for NPC three-level inverters," *Journal of Power Electronics*, Vol. 15, No. 5, pp. 1207-1216, Sep. 2015.

[19] U. M. Choi and K. B. Lee, "Space vector modulation strategy for neutral-point voltage balancing in three-level inverter systems," *IET Power Electronics*, Vol. 6, No. 7, pp. 1390-1398, Aug.2013.

[20] S. W. Hyun, S. J. Hong, J. H. Lee, C. B. Lee, and C. Y. Won, "A method to compensate the distorted space vectors in the unbalanced neutral point voltage of 3-level NPC PWM inverters," *Journal of Power Electronics*, Vol. 16, No. 2, pp. 455-463, Mar. 2016.

[21] N. Li, Y. Wang, W. Lei, R. Niu, and Z. Wang, "Novel carrier-based PWM strategy of a three-level NPC voltage source converter without low-frequency voltage oscillation in the neutral point," *Journal of Power Electronics*, Vol. 14, No. 3, pp. 531-540, May 2014.

[22] C. J. Zhang, Y. Tang, D. Han, H. Zhang, X. Zhang, and K. Wang, "A novel virtual space vector modulation strategy for the neutral-point potential comprehensive balance of neutral-point-clamped converters," *Journal of Power Electronics*, Vol. 16, No. 3, pp. 946-959, May 2016.

[23] Y. He, J. Liu, J. Tang, Z. Wang, and Y. Zou, "Theoretical analysis and control of DC neutral-point voltage balance of three-level inverters in active power filters," *Journal of Power Electronics*, Vol. 12, No. 2, pp. 344-356, Mar. 2012.

[24] Z. Ye, Y. Xu, F. Li, X. Deng, and Y. Zhang, "Simplified PWM strategy for neutral-point-clamped (NPC) three-level converter," *Journal of Power Electronics*, Vol. 14, No. 3, pp. 519-530, May 2014.

[25] U. M. Choi and K. B. Lee, "Neutral-point voltage balancing method for three-level inverter systems with a time-offset estimation scheme," *Journal of Power Electronics*, Vol. 13, No. 2, pp. 243-249, Mar. 2013.

[26] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos, and D. Boroyevich, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Trans. Ind. Electron*., Vol. 54, No. 4, pp. 2288-2294, Aug. 2007.

[27] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, Vol. 27, No. 2, pp. 642-651, Feb. 2012.

[28] Y. Jiao, F. C. Lee, and S. Z Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, Vol. 29, No. 10, pp. 5579-5591, Oct. 2014.

[29] H. B. Zhang, S. J. Finney, A. Massoud, and B. W. Williams, "An SVM algorithm to balance the capacitor voltages of the three-level NPC active power filter," *IEEE Trans. Power Electron.*, Vol. 23, No. 6, pp. 2694-2702, Nov. 2008.

[30] J. Shen, S. Schroder, B. Duro, and R. Roesner, "A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2011.

[31] W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. Power Electron*., Vol. 28, No. 3, pp. 1083-1095, Mar. 2013.

[32] A. H. Bhat and N. Langer, "Capacitor voltage balancing of three-level neutral-point-clamped rectifier using modified reference vector," *IEEE Trans. Power Electron*., Vol. 29, No. 2, pp. 561-568, Feb. 2014.

[33] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Trans. Ind. Electron*., Vol. 56, No. 2, pp. 305-314, Feb. 2009.

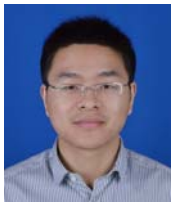
[34] R. Lai, F. Wang, R. Burgos, D. Boroyevich, D. Jiang, and D. Zhang. "Average modeling and control design for VIENNA-type rectifiers considering the DC-link voltage balance," *IEEE Trans. Power Electron*., Vol. 24, No. 11, pp. 2509-2522, Nov. 2009.

[35] Y. L. Familiant, D. G. Holmes, T. A. Lipo, and B. P. McGrath. "A general modulation strategy for a five-level three-phase current source inverter with regulated intermediate DC link currents," in *IEEE Industry Applications Conference (IAS)*, pp. 581-588, Sep. 2007.

[36] R. K. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge. "Neutral-point current modeling and control for neutral-point clamped three-level converter drive with small DC-link capacitors," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2087-2094, Sep. 2011.

[37] R. K. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge. "Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors," *IEEE Trans. Ind. Electron*., Vol. 60, No. 5, pp. 1861-1871, May 2013.

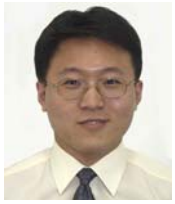
[38] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, Second Edition, Secaucus, NJ, USA, Kluwer Academic Publishers, pp.348-352, 2000.



**Jianguo Lyu** was born in Jiangsu Province, China, in 1987. He received his Ph.D. degree in Control Science and Engineering from the Nanjing University of Science and Technology (NUST), Nanjing, China, in 2016. In 2016, he joined the School of Automation, NUST, where he has been engaged in teaching and research in the field of power electronics. His current research interests include the modeling and control of power converters, power factor correction converters, renewable energy generation systems and electric traction systems for rail vehicles.

**Wenbin Hu** was born in Jiangsu Province, China, in 1970. He received his B.S. degree in Electrical Engineering and Automation from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1992; his M.S. degree in Control Theory and Control Engineering from the Nanjing University of Science and Technology (NUST), Nanjing, China, in 1999; and his Ph.D. degree in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics, in 2003. In 2004, he joined the Faculty of Electrical Engineering, School of Automation, Nanjing University of Science and Technology (NUST). In 2010, he became an Associate Professor at NUST, where he has been engaged in teaching and research in the field of power electronics. His current research interests include power factor correction converters, renewable energy generation systems and electric traction systems for rail vehicles.

**Fuyun Wu** was born in Jiangsu Province, China, in 1988. She received her B.S. and M.S. degrees in Electrical Engineering and Automation from the Nanjing University of Science and Technology (NUST), Nanjing, China, in 2012 and 2015, respectively. In 2015, she joined the College of Mechanical and Electrical Engineering (Originally known as College of Electrical and Automatic Engineering), Sanjiang University, Nanjing, China, where she has been engaged in teaching and research in the field of power electronics. Her current research interests include the modeling and control of power converters, and renewable energy generation systems.



**Kai Yao** was born in Jiangsu Province, China, in 1980. He received his B.S. degree in Industrial Automation from Nantong University, Nantong, China, in 2002. He also received his M.S. degree in Mechanical Design and Theory, and his Ph.D. degree in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2005 and 2010, respectively. In 2011, he joined the Faculty of Electrical Engineering, School of Automation, Nanjing University of Science and Technology (NUST), Nanjing, China. In 2016, he became an Associate Professor at NUST, where he has been engaged in teaching and research in the field of power electronics. His current research interests include power factor correction converters, renewable energy generation systems and power supplies for LEDs.

**Junji Wu** was born in Henan Province, China, in 1955. He received his M.S. degree from the Nanjing University of Science and Technology (NUST), Nanjing, China, in 1990. In 1970, he joined in Nanjing University of Science and Technology. He became a professor at NUST, in 2000, where he has been engaged in teaching and research in the field of control science and engineering. His current research interests include the modeling and control of electrical systems, modern data acquisition technology, renewable energy generation systems and electric traction systems for rail vehicles.