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Analysis and Design of a Separate Sampling Adaptive PID Algorithm for Digital DC-DC Converters

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Abstract

Based on the conventional PID algorithm and the adaptive PID (AD-PID) algorithm, a separate sampling adaptive PID (SSA-PID) algorithm is proposed to improve the transient response of digitally controlled DC-DC converters. The SSA-PID algorithm, which can be divided into an oversampled adaptive P (AD-P) control and an adaptive ID (AD-ID) control, adopts a higher sampling frequency for AD-P control and a conventional sampling frequency for AD-ID control. In addition, it can also adaptively adjust the PID parameters (i.e. K_p, K_i and K_d) based on the system state. Simulation results show that the proposed algorithm has better line transient and load transient responses than the conventional PID and AD-PID algorithms. Compared with the conventional PID and AD-PID algorithms, the experimental results based on a FPGA indicate that the recovery time of the SSA-PID algorithm is reduced by 80% and 67% separately, and that overshoot is decreased by 33% and 12% for a 700mA load step. Moreover, the SSA-PID algorithm can achieve zero overshoot during startup.

Key words: DC-DC converter, digital controller, fast transient response, SSA-PID algorithm

I. INTRODUCTION

With the rapid development of communication, computer and consumer electronic industries, digitally controlled DC-DC converters have stood out in recent years. Compared with analog control, digital control has significant advantages in terms of online programmability, advanced control algorithms, efficiency optimization, high operation precision and reliability [1]-[4]. Meanwhile, the digital PID algorithms is one of the most widely used control methods in discrete systems [5]-[8].

Research in the PID control field has developed rapidly in recent years. D. Trevisan et.al from Udine built a model of a voltage-mode controlled converter that included a PID controller [9]. K.-W. Seo from Dongguk University designed a precise fuzzy PID controller for DC-DC converters in 2012, where a precise matrix model was used to adjust the PID parameters [10]. However, the relatively high complexity and extra hardware and software costs are their drawbacks. Meanwhile, unexpected output oscillations can be introduced by these techniques [11]-[15]. To overcome the above mentioned limitations, this paper proposed a separate sampling adaptive PID (SSA-PID) algorithm to reduce the recovery time and overshoot/undershoot during the transient process. In addition, the proposed algorithm is easy to implement.

The following section introduces the SSA-PID control algorithm. In addition, it gives a description of the differences between the adaptive PID (AD-PID) and the SSA-PID control. Section III briefly describes the simulation process of a digital DC-DC Buck converter using MATLAB/Simulink. This section also presents simulation results. Section IV elaborates on the process of FPGA implementation and presents an experimental comparison between the PID, AD-PID and SSA-PID controllers. Finally, some conclusions are given in Section V.

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II. PRINCIPLE OF THE SSA-PID ALGORITHM

A. AD-PID Algorithm

A system diagram of an AD-PID /PID controlled DC-DC

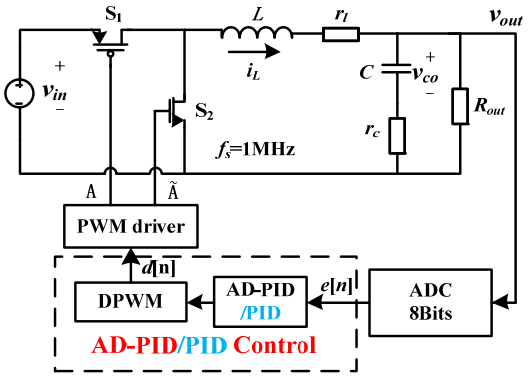


Fig. 1. System diagram of an AD-PID/PID controlled Buck converter.

Buck converter is presented in Fig. 1. In addition, the transfer function of a digital PID algorithm can be described as:

$$G_{PID}(z) = K_p + K_i/(1-z^{-1}) + K_d(1-z^{-1}) \quad (1)$$

where K_p, K_i and K_d are the constant coefficients of the proportional gain, integral term and derivative term, respectively.

Considering the A/D converter, PID compensator and digital pulse width modulator (DPWM), the open-loop transfer function of a Buck converter can be written as Equ. (2).

$$G_o(s) = \frac{1}{U_m}\frac{V_{out}}{D}\frac{(1+sCr_c)(K_i+K_ps+K_ds^2)}{s+s^2[\frac{L+CR_{out}r_l}{R_{out}+r_l}+Cr_c]+s^3LC\frac{R_{out}+r_c}{R_{out}+r_l}} \quad (2)$$

where L, R_{out} and C represent the inductor value, load resistance and capacitor value, respectively. r_l and r_c are the DCR of the inductor and the ESR of the capacitor, separately. V_{out} and D represent the mean value of the output voltage and duty ratio, respectively. U_m is the amplitude of a saw-tooth wave in the DPWM module, which is equal to 1 in the proposed design.

In general, under the premise of system stabilization, the greater the loop bandwidth, the better the transient performance of the closed-loop system. Actually, the loop bandwidth is often designed at about 1/10 of the switching frequency. Nevertheless, the dynamic performance of the system can be improved by appropriately increasing the bandwidth during the transient process. Meanwhile, the steady-state accuracy of the system can also be effectively improved with a moderate increase in the low-frequency gain. Table I shows the variation trend of the system performance when the PID parameters are changed.

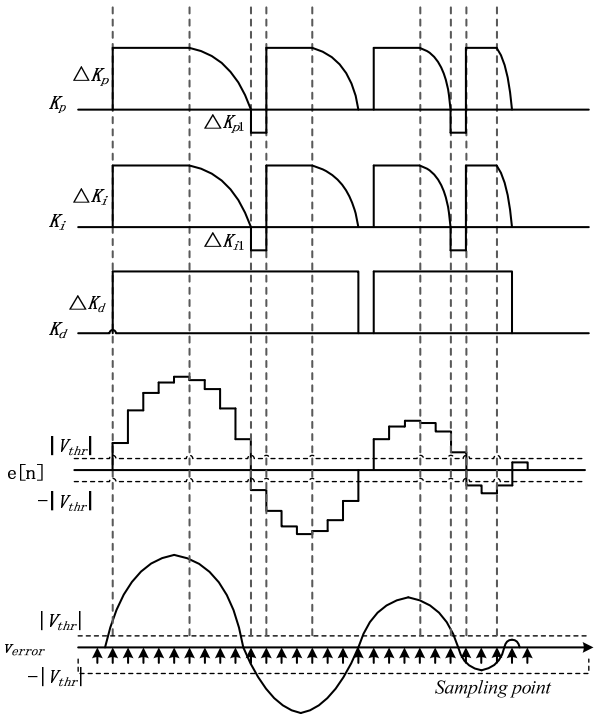


Fig. 2. Operational waveforms of AD-PID controller.

TABLE I
RELATIONSHIPS BETWEEN SYSTEM CHARACTERISTICS AND PID PARAMETERS

Variation Trend of Parameters	Low-frequency Gain	Bandwidth	Phase Margin
K_p increase	Constant	Increase	Reduce
K_i increase	Increase	Constant	Reduce
K_d increase	Constant	Increase	Increase

The AD-PID algorithm allows the PID parameters to adaptively adjust as needed in different situations. Thus, effectively depressing overshoot/undershoot and reducing the output voltage deviation as well as the recovery time. Therefore, the AD-PID algorithm should maintain an appropriate bandwidth to stabilize the system in the steady state, while a larger bandwidth and low-frequency gain in transient process are helpful to reduce the recovery time and output voltage deviation. The transfer function of the AD-PID compensator in the z domain is:

$$G_{AD-PID}(z) = (K_p+\alpha) + \frac{K_i+\beta}{1-z^{-1}} + (K_d+\gamma)*(1-z^{-1}) \quad (3)$$

$$\alpha = \begin{cases} 0, & |v_{error}(n)| < |V_{thr}| \\ \left.\begin{cases} \Delta K_p, & |v_{error}(n-1)| \le |v_{error}(n)| \\ \dfrac{|v_{error}(n)|}{|V_{error-peak}|} * \Delta K_p, & |v_{error}(n-1)| > |v_{error}(n)| \end{cases}\right\} & v_{error}(n)*v_{error}(n-1) > 0 \\ \Delta K_{p1}, & v_{error}(n)*v_{error}(n-1) \le 0 \end{cases} \Bigg\} |v_{error}(n)| \ge |V_{thr}| \quad (4)$$

where α, β and γ are set to zero in the steady state. However, they can change adaptively according to the error signal v_{error} in transient process.

Operational waveforms of the AD-PID compensator are shown in Fig. 2. The basic procedure is outlined as follows. Firstly, the present error signal $v_{error}(n)$ is compared with the threshold voltage V_{thr}. If $v_{error}(n)$ is no more than V_{thr}, the system is identified as being in the steady state. At the same time, α, β and γ are set to 0 to ensure the stability of the system. If $v_{error}(n)$ is greater than V_{thr}, the system is considered to be in the transient state. Meanwhile, α, β and γ change quickly to increase the loop bandwidth. This in turn, accelerates the transient response of the system. Eqns. (4)-(6) summarize the selection rules of α, β and γ in different states.

ΔK_p, ΔK_{p1}, ΔK_i, ΔK_{i1} and ΔK_d are the adaptive variable coefficients of the proportional gain, integral term and derivative term, respectively.

B. SSA-PID Algorithm

One of the key points of digital control is to accelerate the transient response. However, the conversion time of an A/D converter and the computation time of a digital compensator may have bad effects on the transient performance. In order to solve this problem, a SSA-PID algorithm is proposed on the basis of an AD-PID algorithm, which divides the AD-PID control into an oversampled adaptive P (AD-P) control and an adaptive ID (AD-ID) control. Regarding the AD-P control, the system uses a high-speed but low-resolution A/D converter for rapid detection and correction. Meanwhile, a high-resolution but low-speed A/D converter for precise adjustment is adopted in the AD-ID control. The sampling frequency of the AD-ID control is the same as that of the AD-PID control, while the AD-P control is oversampled. A system diagram of a SSA-PID controlled Buck converter is shown in Fig. 3.

In Fig. 3, v_{in} is the input voltage and v_{out} is the output voltage, S_1 and S_2 are MOSFETs, and f_s is the switching frequency, which is equal to 1MHz in this design. It can be seen from Fig. 3 that the two control loops are parallel, and that oversampling is only adopted in the AD-P control for a trade-off between performance and cost.

Based on the above analysis, the SSA-PID control algorithm can be expressed as Equ. (7):

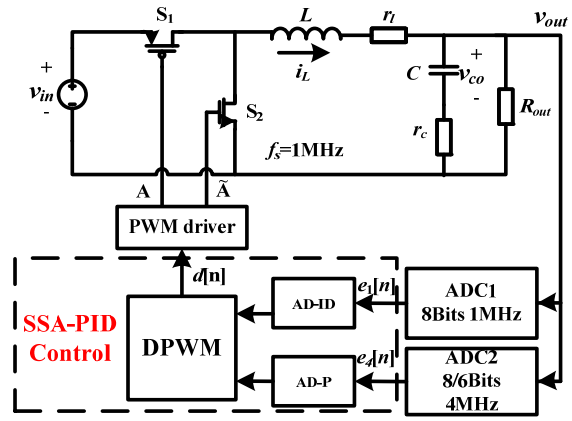


Fig. 3. System diagram of a SSA-PID controlled Buck converter.

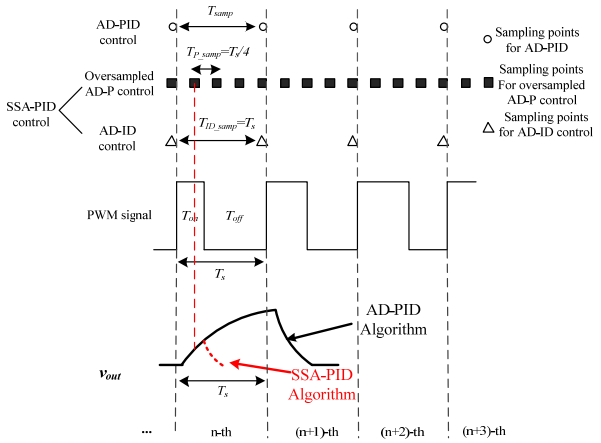


Fig. 4. The comparison of sampling methods between the two algorithms.

$$H(s) = \hat{H}_p\, e^{-s\tau_1} + (\frac{\hat{H}_i}{s} + s\,\hat{H}_d)e^{-s\tau_2} \tag{7}$$

where $\hat{H}_p$, $\hat{H}_i$ and $\hat{H}_d$ are the self-adaptive gains of the proportional term, integral term and differential term, respectively. Usually, the delay time τ_2 is equal to the switching period T_s, while τ_1 is reduced to $T_s/4$.

A comparison of the sampling points between the AD-PID algorithm and the SSA-PID algorithm can be seen from Fig. 4, where T_{samp}, T_{ID_samp} and T_{P_samp} are the sampling periods of the AD-PID control, AD-ID control and oversampled AD-P control, respectively. In the AD-PID algorithm, the output voltage is sampled once in a switching cycle T_s. In terms of the SSA-PID algorithm, the sampling frequency of the

$$\beta = \begin{cases} 0, & |v_{error}(n)| < |V_{thr}| \\ \left.\begin{cases} \Delta K_i, & |v_{error}(n-1)| \le |v_{error}(n)| \\ \dfrac{|v_{error}(k)|}{|V_{error-peak}|} * \Delta K_i, & |v_{error}(n-1)| > |v_{error}(n)| \end{cases}\right\} & v_{error}(n) * v_{error}(n-1) > 0 \\ \Delta K_{i1}, & v_{error}(n) * v_{error}(n-1) \le 0 \end{cases} \Bigg\} |v_{error}(n)| \ge |V_{thr}| \tag{5}$$

$$\gamma = \begin{cases} 0, & |v_{error}(n)| < |V_{thr}| \\ \Delta K_d, & |v_{error}(n)| \ge |V_{thr}| \end{cases} \tag{6}$$

TABLE II
DESIGN SPECIFICATIONS FOR THE BUCK CONVERTER

Parameter	Value	Unit
Input voltage (v_{in})	5	V
Output voltage (v_{out})	1.8	V
Inductor (L)	4.7	μH
DCR of Inductor (r_l)	80	mΩ
Output capacitor (C)	10	μF
ESR of Capacitor (r_c)	70	mΩ
Switching frequency (f_s)	1	MHz

AD-ID control is the same as the switching frequency, while the output voltage is sampled four times in a switching cycle for the AD-P control. Meanwhile, the SSA-PID algorithm has the advantage of the AD-PID algorithm that the control parameters (K_p, K_i and K_d) change adaptively according to the system state. It is obvious that output voltage errors will be detected more quickly because of the oversampled AD-P control, and the feedback control loop will work immediately to reduce the recovery time and overshoot/undershoot, which is why the SSA-PID algorithm possesses better transient performance than the AD-PID algorithm. Fig. 5 shows an implementation diagram of the SSA-PID algorithm.

III. SIMULATION OF THE SSA-PID ALGORITHM

The integrated DC-DC converter is composed of a Buck topology, an A/D converter, a digital compensator and a DPWM. Fig. 6 shows a Simulink model of the whole system, where the Buck topology is constructed by using the state space averaging method. In addition, the design specifications of the Buck converter are shown in Table II.

Simulation data from the conventional PID, AD-PID and SSA-PID control algorithms are imported into the Origin software for comparison. Figs. 7-8 indicate that SSA-PID algorithm possesses a shorter recovery time and less overshoot/undershoot compared with the PID algorithm or the AD-PID algorithm.

IV. EXPERIMENTAL RESULTS OF THE SSA-PID ALGORITHM

In order to observe the effects of these three compensation algorithms in an actual power system, a prototype of a FPGA-based digital Buck converter is built (see Fig. 9). The integrated power MOSFET transistor is a μPA2791, and the driver chip is a UCC27524. An Altera Cyclone II device (EP2C5Q208C8) is used to implement the SSA-PID compensator and DPWM. The input voltage is v_{in} = 5V and the output voltage is v_{out} =1.8V.

The duty ratio signal of the conventional PID algorithm or the AD-PID algorithm is as follows:

$$\begin{aligned} d[n] &= d[n-1] + (K_p + K_i + K_d) * e[n] \\ &\quad - (K_p + 2K_d) * e[n-1] + K_d * e[n-2] \\ &= d[n-1] + a * e[n] - b * e[n-1] + c * e[n-2] \\ &= d[n-1] + \Delta d[n] \end{aligned} \tag{8}$$

where $d[n\text{-}1]$ is the duty ratio signal of the previous cycle, and $d[n]$ is the present duty ratio signal. K_p, K_i and K_d are the constant coefficients of the PID algorithm or the adaptive gain coefficients of the AD-PID algorithm.

The SSA-PID algorithm uses a separate sampling structure, and its duty ratio signal can be described as:

$$d[n] = d_4[n] + d_1[n] \tag{9}$$

$$\begin{aligned} d_1[n] &= d_1[n-1] + K_i * e_1[n] \\ &\quad + K_d * (e_1[n] - 2e_1[n-1] + e_1[n-2]) \\ &= d_1[n-1] + (K_i + K_d) * e_1[n] - 2K_d * e_1[n-1] \\ &\quad + K_d * e_1[n-2] \\ &= d_1[n-1] + a * e_1[n] - b * e_1[n-1] + c * e_1[n-2] \end{aligned} \tag{10}$$

$$d_4[n] = d_4[n-1] + K_p * (e_4[n] - e_4[n-1]) \tag{11}$$

Fig. 10 shows an implementation diagram of the SSA-PID algorithm. The two sampling channels are calculated separately in the SSA-PID algorithm. The output voltage, sampled at 1MHz, is compared with the reference voltage in the error1 module to obtain the present error signal e_1n, the previous moment error signal e_1n1, the error signal of two cycles ago e_1n2 as well as their corresponding sign bits e_1n-*sign*, e_1n1-*sign* and e_1n2-*sign*. Meanwhile, the output voltage sampled at 4MHz is compared with the reference voltage in the error2 module to obtain the present error signal e_4n, the previous moment error signal e_4n1, and the corresponding sign bits e_4n-*sign* and e_4n1-*sign*. Next, the values of $|a*e_1n|$, $|b*e_1n1|$, $|c*e_1n2|$, $|d*e_4n|$ and $|d*e_4n1|$ are calculated by the corresponding algorithm. Then, the d_correction module calculates the values of *delta_d*$_1$ (=$a*e_1n$-$b*e_1n1$+$c*e_1n2$) and *delta_d*$_2$ (=$d*e_4n$-$d*e_4n1$) based on the sign bits and the error signals. Finally, the duty ratio command signal dn (=d_1n+d_4n) can be calculated by the dn_output module, where d_1n=d_1n_last+*delta_d*$_1$ and d_4n=d_4n_last+ *delta_d*$_4$.

Figs. 11-13 show experimental results of the transient response of the three control algorithms, including the start-up process and load transient response. It can be seen that the transient performance of the conventional PID algorithm, AD-PID algorithm and SSA-PID algorithm are successively getting better and better. The start-up time of the SSA-PID algorithm is significantly reduced compared with the conventional PID algorithm, and the overshoot is eliminated in the proposed algorithm. This provides excellent start-up protection for the power system. In addition, compared with the PID and AD-PID algorithm, the recovery time and overshot/undershoot of the SSA-PID algorithm are effectively improved.

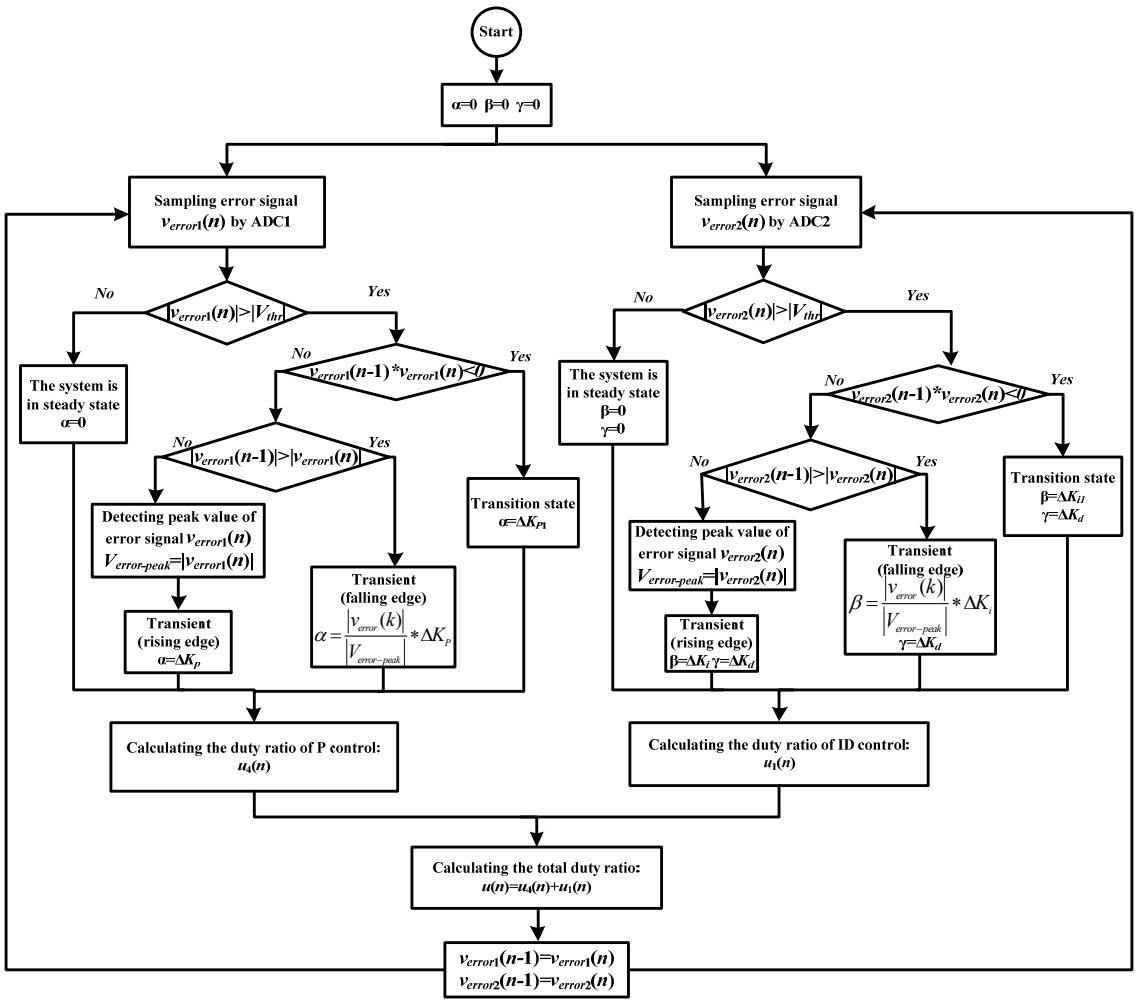


Fig. 5. The flowchart of SSA-PID algorithm.

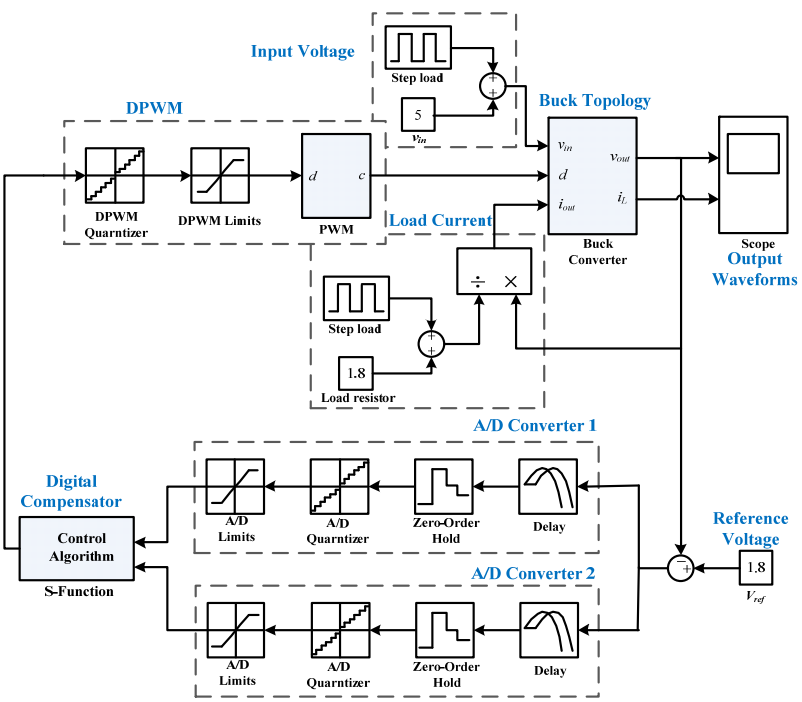


Fig. 6. The Simulink model of a digital SSA-PID controlled Buck converter.

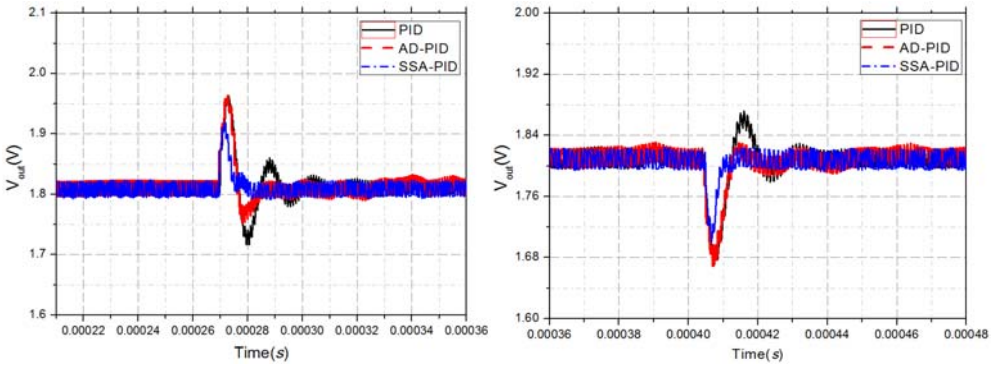


Fig. 7. Load transient response for 500mA load step ((a) overshoot, (b) undershoot).

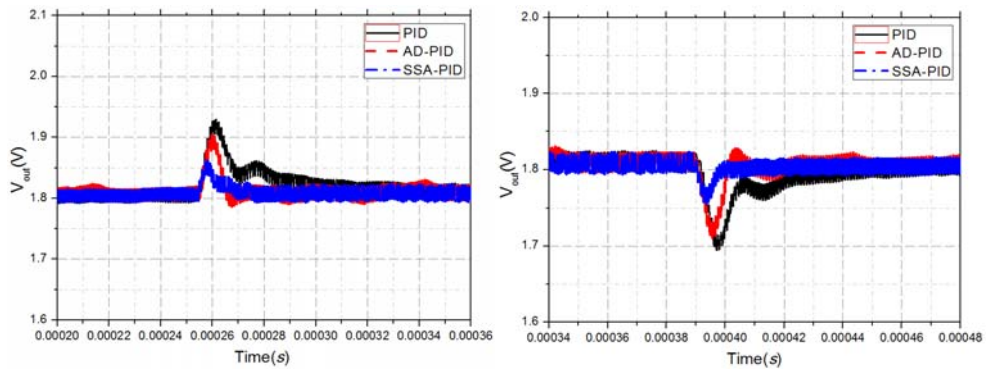


Fig. 8. Line transient response for 1V input voltage step ((a) overshoot, (b) undershoot).

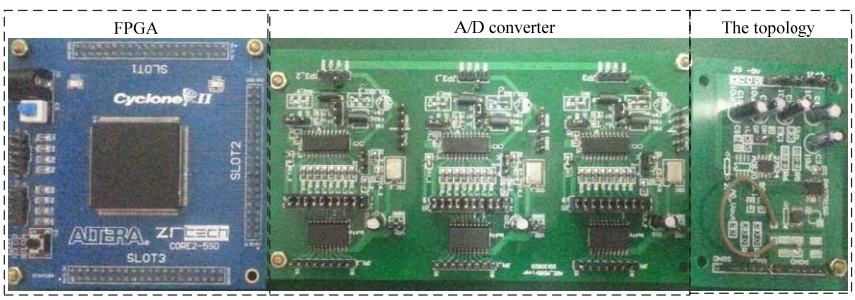
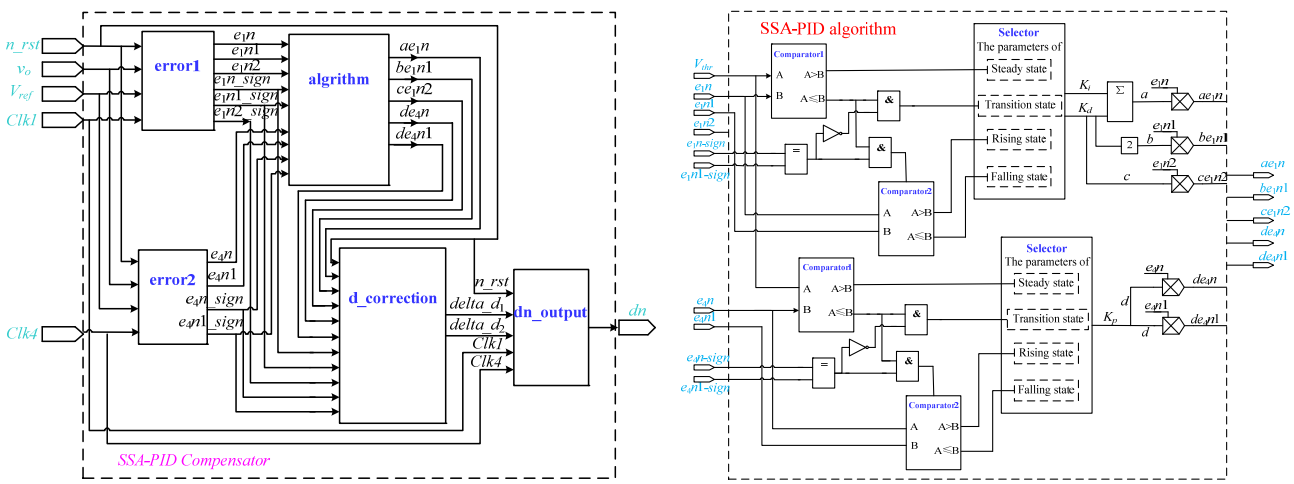
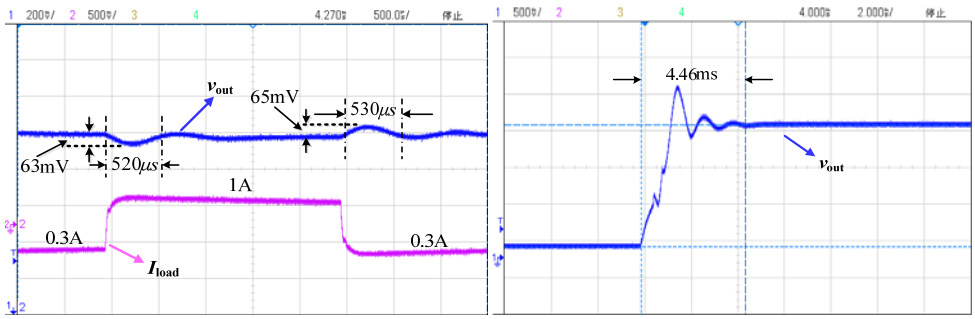


Fig. 9. The verification platform of a digital Buck converter.



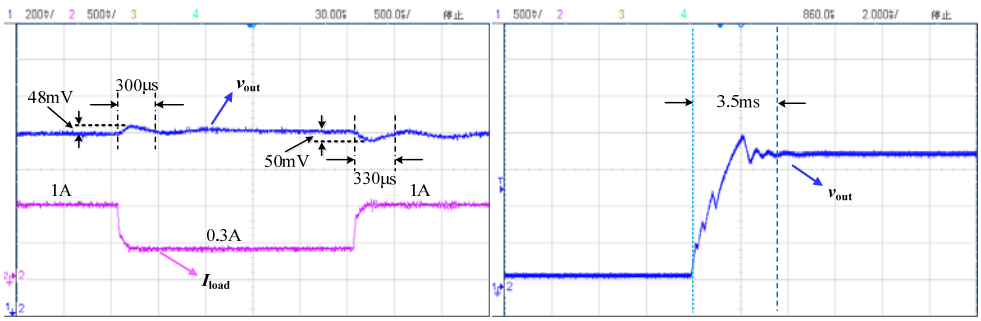
(a) The architecture of SSA-PID compensator. (b) The structure of SSA-PID algorithm.

Fig. 10. Implementation of the SSA-PID algorithm.



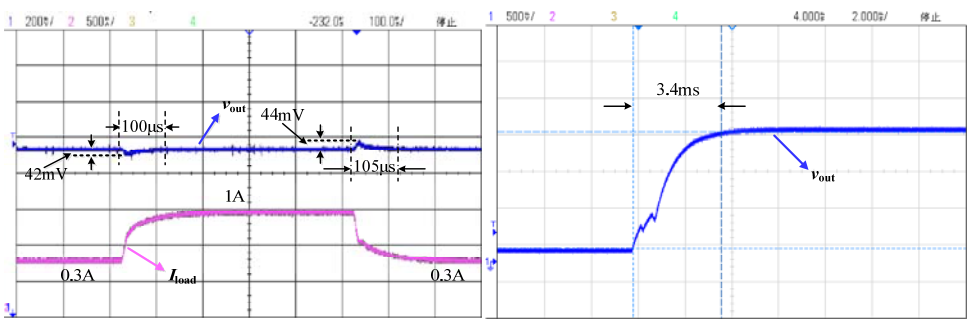
(a) Load current change between 0.3A and 1A. (b) Start-up process.

Fig. 11. Transient response of conventional PID algorithm.



(a) Load current change between 0.3A and 1A. (b) Start-up process.

Fig. 12. Transient response of AD-PID algorithm.



(a) Load current change between 0.3A and 1A. (b) Start-up process.

Fig. 13. Transient response of SSA-PID algorithm.

TABLE III
TRANSIENT RESPONSE COMPARISON OF THE THREE ALGORITHMS

Algorithm	Line transient response (1V)	Load transient response	
		Simulation (500mA)	Experiment (700mA)
	Overshoot/ undershoot	Overshoot/ undershoot	Overshoot/ undershoot
PID	40μs (80mV)/ 60μs (75mV)	30μs (140mV)/ 20μs (130mV)	530μs (65mV)/ 520μs (63mV)
AD-PID	15μs (80mV)/ 15μs (90mV)	15μs (140mV)/ 10μs (130mV)	300μs (48mV)/ 330μs (50mV)
SSA-PID	10μs (40mV)/ 11μs (45mV)	10μs (100mV)/ 5μs (95mV)	105μs (44mV)/ 100μs (42mV)

Table III summarizes a comparison of the simulation and experimental results among the three algorithms, where the time before a bracket represents the recovery time and the value in a bracket means the overshoot/undershoot voltage. It is obvious that the SSA-PID algorithm shows better transient performance than the PID and AD-PID algorithms.

Table IV summarizes a comparison of the hardware resource occupancy between the conventional PID, AD-PID and SSA-PID algorithms. It can be seen that the number of used logic elements of the SSA-PID algorithm is the lowest. However, the number of pins is the highest. Unlike the AD-PID algorithm, the SSA-PID algorithm and the conventional PID algorithm do not require embedded 9-bit-multiplier elements. Therefore, the SSA-PID algorithm can achieve better transient performance and less resource consumption compared with the AD-PID algorithm.

A comparison between the proposed SSA-PID algorithm and prior arts is summarized in Table V. According to this table, the SSA-PID algorithm has advantages in terms of hardware cost and transient response compared with the controllers in references [16], [17] and the LTC3530 chip.

TABLE IV
COMPARISON OF HARDWARE RESOURCE OCCUPANCY

Resource (EP2C5Q208C8)	Control Scheme		
	PID	AD-PID	SSA-PID
Logic elements	1089/4608 (24%)	1104/4608 (24%)	961/4608 (21%)
Combinational functions	808/4608 (18%)	849/4608 (18%)	688/4608 (15%)
Dedicated logic registers	599/4608 (13%)	637/4608 (14%)	654/4608 (14%)
Pins	12/142 (8%)	12/142 (8%)	20/142 (14%)
Bits of memory	2176/119808 (2%)	2176/119808 (2%)	2176/119808 (2%)
Embedded 9-bit multiplier elements	0/26 (0%)	7/26 (27%)	0/26 (0%)
PLLs	1/2 (50%)	1/2 (50%)	1/2 (50%)

TABLE V
COMPARISON BETWEEN THE PROPOSED SSA-PID CONTROL ALGORITHM AND PRIOR ARTS

	This paper	[16]	[17]	LTC3530
Control type	Digital	Digital	Digital	Analog
Control algorithm	SSA-PID	Improved digital peak current	First-order digital filter	N/A
Switching frequency	1MHz	50kHz	3.125MHz	1MHz
Input voltage	3.6-5V	5V	0-3.3V	1.8-5.5V
Output voltage	1.8V	1.5V	0.1-3.3V	3.3V
Maximum current	1A	2A	N/A	500mA
Filter inductor	4.7μH	20μH	2.2μH	4.7μH
Filter capacitor	10μF	1420μF	10μF	22μF
Number of A/D	2	2	1	0
Digits of A/D	6bits/8bits	8bits	10bits	N/A
Digits of DPWM	10bits	10bits	>10bits	N/A
Load Step Response	0.15μs/mA 0.06V/A	1.24μs/mA 0.07V/A	2μs/mA 0.08V/A	1μs/mA 0.33V/A

V. CONCLUSIONS

A Separate Sampling Adaptive PID algorithm for digitally controlled DC-DC converters is proposed in this paper. The proposed algorithm exploits the oversampled AD-P control and the AD-ID control to improve the transient response of the system. In addition, simulation results based on MATLAB/Simulink software and experimental verification based on a FPGA are presented. Both the simulation and experimental results indicate that the proposed control algorithm possesses better startup and transient performance compared with the conventional PID and AD-PID algorithms, while the hardware occupancy is kept at an appropriate level. The proposed algorithm provides useful guidance on the design of digital controllers for DC-DC converters.

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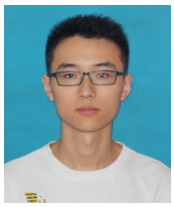

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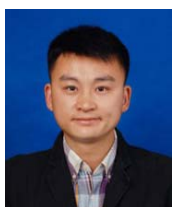

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