JPE 17-1-3

https://doi.org/10.6113/JPE.2017.17.1.20
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Novel Zero-Voltage-Switching Push-Pull Forward Converter with a Parallel Resonant Network

Chunwei Cai†, Chunyu Shi*,**, Yuxing Guo*, Zi Yang*, and Fangang Meng*

†,*School of Information and Electrical Engineering, Harbin Institute of Technology, Weihai, China
**CRRC Qingdao Sifang Rolling Stock Research Institute Co., Ltd., Qingdao, China

Abstract

A novel zero-voltage-switching (ZVS) push-pull forward converter with a parallel resonant network is presented in this paper. The novel topology can provide a releasing loop for the energy storage in a leakage inductor for the duration of the power switching by the resonant capacitors paralleled with the primary windings of the transformer. Then the transformer leakage inductor is utilized to be resonant with the parallel capacitor, and the ZVS operation is achieved. This converter exhibits many advantages such as lower duty-cycle losses, limited peak voltage across the rectifier diodes and a higher efficiency. Furthermore, the operating principles and key problems of the converter design are analyzed in detail, and the ZVS conditions are derived. A 500W experimental converter prototype has been built to verify the effectiveness of the proposed converter, and its maximum efficiency reaches 94.8%.

Key words: High efficiency, Parallel resonant, Push-pull forward, Zero voltage switching (ZVS)

I. INTRODUCTION

In applications where the input source exhibits a low voltage and a high current, such as photovoltaic energy and fuel cells, the push-pull converter is a desirable DC-DC converter topology. Compared with the conventional push-pull converter, the push-pull forward converter (PPFC) can solve the problems of high turn-off voltage spikes across switches and it can improve the efficiency of the magnetic core [1]. In order to further improve the efficiency and reduce the size, the technology of integrated magnetics is applied [2], [3]. All of the magnetic components including the input filter inductor, step-down transformer and output filter inductors are integrated into a single EE core. Moreover, the improved structure can make the converter more compact and less expensive. A novel PPFC has been proposed to achieve a high reliability and high input voltage applications in [4]. In this topology, the high utilization factor of the transformer is achieved by using two forward cells coupled via an integrated magnetizing core and operating the two cells in an interleaving fashion. In addition, the high reliability is guaranteed since no direct-short path exists in the proposed converter.

A three-level converter has been proposed to reduce the voltage stresses of the switches, the size of the input filter and the output filter [5]. A novel three-level PPFC has been proposed to reduce both the input current ripple and the output filter inductor current ripple in [6], [7]. Moreover, the voltage stress of the rectifier diode can be reduced by this control strategy and an appropriate external paralleled capacitor. However, in three-level topologies, the circuit topology needs more active devices and the drive circuit is complicated.

In order to increase the power density and to reduce the size and weight of the magnetic element, the switching frequency needs to be increased. Then, the turn-off voltage spikes of the transistors cannot be eliminated in the hard switching mode for the conventional PPFC, resulting in severe EMI and a high switching loss. In the dc-dc converter family, soft-switching technology is proposed to solve the above mentioned problems [8], [9]. An LCL resonant Push-Pull dc/dc converter was presented in [10], [11], with C-L resonant components located behind the output stage rectifiers. The MOSFET switches in the primary side operate under the zero-voltage switching (ZVS) conditions due to the

Manuscript received Aug. 20, 2016; accepted Nov. 14, 2016
Recommended for publication by Associate Editor Chun-An Cheng.
†Corresponding Author: caichunwei@hit.edu.cn
Tel: +86-631-5687800, Fax: +86-631-5687028, HIT, Weihai
*School of Information and Electrical Engineering, China
**CRRC Qingdao Sifang Rolling Stock Research Institute CO., LTD., China

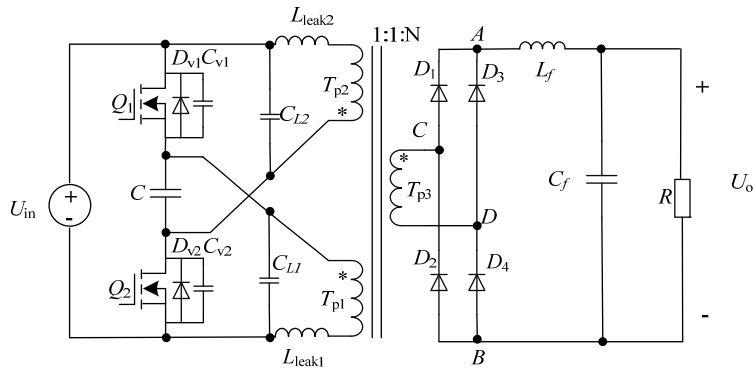


Fig. 1. Parallel resonant push-pull forward converter.

commutation of the transformer magnetizing current and the snubbing effect of the inherent drain-source capacitance. A pair of auxiliary circuits was added to the primary side of the transformer to clamp the voltage spike and to recycle the energy trapped in the leakage inductors

in [12]. As a result, the main switches can be turned on with ZVS.

In isolated bidirectional applications, the symmetric structure with the phase-shift control enables the ZVS operation for all of the power switches in [13]. The low voltage side used a push-pull structure and the high voltage side employed a full bridge structure in [14-15]. With the phase-shift control strategy, all of the switches operate under the ZVS condition.

However, only a few articles demonstrate that PPFCs can operate under the ZVS condition. A push-pull forward half-bridge bidirectional dc-dc converter was presented in [16], with all of the switches operating under zero-voltage using the phase-shift control strategy. However, the half-bridge part works in the boost mode when the voltage is step-up, resulting in adverse effects on the dynamic characteristics. At same time, the effective duty ratio is lost and the conversion efficient decreases. The magnetizing current was used to achieve the ZVS operation for the switches in the improved PPFC in [17]. The magnetizing inductance should be sufficiently small. Therefore, the transformer must be designed with the appropriate air-gap. However, a small magnetizing inductance causes a large magnetizing current. As a result, all the no-load loss, the reactive current and current stress increases.

As shown in Fig.1, a novel zero voltage switching push-pull forward converter with a parallel resonant network is proposed. The converter is analyzed and designed. Due to the presence of parallel capacitors and transformer leakage inductors, the resonance makes the switches maintain zero voltage switching even under light loads. The proposed converter operates with soft-switching, which reduces the switches losses and rectifier diodes turn-off voltage. The efficiency can be significantly enhanced.

This paper is organized as follows. The steady-state operation and different intervals of operation in the proposed converter are analyzed in Section II. The design issue of the converter is described in detail in section III. Simulation results using SABER are demonstrated to verify the analysis and design in IV. A 500W laboratory prototype has been built and tested to validate the operation of the proposed converter in the analysis of the ZVS. Section IV presents some experimental results, and Section V provides some conclusions.

II. Operation and Analysis of the Converter

Fig. 1 shows the main circuit of the proposed converter. It is a novel zero voltage switching push-pull forward converter with a parallel resonant network. In this figure, U_{in} is the input voltage, Q_1 and Q_2 are the main power switches, and D_{v1} and D_{v2} are the anti-parallel body diodes corresponding to Q_1 and Q_2 respectively. C is the clamping capacitor, L_{leak1} and L_{leak2} are the leakage inductances of the windings T_{p1} and T_{p2}, L_{m1} and L_{m2} are the magnetizing inductances of the windings T_{p1} and T_{p2}, C_{L1} and C_{L2} are the parallel resonant capacitors, D_1-D_4 are the rectifying diodes, and L_f and C_f are the output filter inductor and capacitor, respectively. The turn ratio of the transformer is n=1:1:N. The proposed converter works in the PWM mode. The duty cycle of the gating signal for the switches Q_1 and Q_2 is approximately 0.5, and their phase shift is 180°. There are 10 intervals in one cycle. The main waveforms are shown in Fig. 2.

The following assumptions are made before analyzing the converter operation principles:

a) All of the semiconductor devices are ideal and lossless.

b) All of the inductors, capacitors and transformer are ideal.

c) C_{v1} and C_{v2} are equal i.e., $C_{v1}=C_{v2}=C_v$.

d) The leakage inductances of the transformers are equal i.e., $L_{leak1}=L_{leak2}=L_{leak}$, and the magnetizing inductance is large enough.

e) The two parallel resonant capacitors are equal i.e., $C_{L1}=C_{L2}=C_L$.

The operation principle is only analyzed in the first half cycle. In the second half cycle, these intervals are the same as

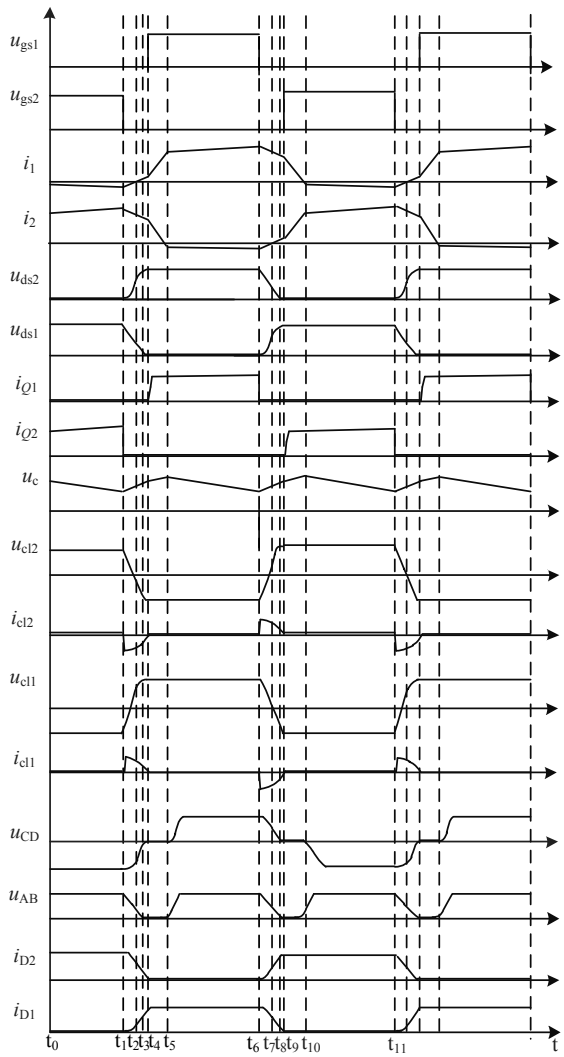


Fig. 2. Steady-state operating waveforms of novel PPFC.

those in the first half cycle, and the other symmetrical devices conduct. Fig. 3 illustrates the equivalent circuits in different modes of operation for the first half cycle.

A. Interval 0 (Fig. 3(a): $t_0<t<t_1$)

In this interval, the transistor Q_2 and the diodes D_2 and D_3 are conducting. The voltage source energy is transferred to the load by loop1, U_{in}—L_{leak2}—T_{p2}—Q_2—U_{in}, and loop2, C—Q_2—L_{leak1}—T_{p1}—C. At the end of this interval, the current i_1 reaches its minimum value and the current i_2, which flows through the magnetizing inductors, increases to its maximum value.

B. Interval 1 (Fig. 3(b): $t_1<t<t_2$)

At t=t_1, the transistor Q_2 is turn off. Q_2 can achieve zero-voltage turn-off if the capacitors C_{v2} and C_{L2} are large enough.

During this interval, the rectifier diodes D_2 and D_3 are conducting while D_1 and D_4 are turned OFF. The output filter inductor L_f is transformed to the primary side to resonate with the leakage inductors of the transformer, C_{v2}, C_{L2}, C_{v1} and C_{L1}. Consequently, the capacitors C and C_{v2} are charged and the capacitor C_{L2} gets to be discharged by the current i_2. The voltage u_{cv2} (i.e., u_{ds2}) rises up from zero while u_{cL2} falls down from U_{in}. Meanwhile, the capacitors C_{L1} and C_{v1} are discharged by i_1. As a result, the voltage u_{cv1} (i.e., u_{ds1}) starts falling down from $2U_{in}$, and u_{cL1} also begins falling down from U_{in}. In this mode, i_2 decreases slowly and i_1 decreases reversely. Accordingly, i_{D2} also decreases. At the end of this interval, the current i_1 decreases to zero. The node voltage equations are established as shown in Equ. (1).

$$\begin{cases} i_1 = \dfrac{[i_1(t_{1-})+i_2(t_{1-})]}{2}\cos[\omega((t-t_1)]+\dfrac{I_p}{2} \\ i_2 = \dfrac{(C_v+C_L)[i_1(t_{1-})+i_2(t_{1-})]}{2(2C+C_L+C_v)}\cos[\omega((t-t_1)]-\dfrac{I_p}{2} \\ u_p = U_{in}+\dfrac{I_p}{2(C_v+C_L)}(t-t_1)+\dfrac{L_{leak}I_p}{2}\delta(t-t_1)-\dfrac{L_{leak}i_1(t_{1-})}{2}\delta(t-t_1) \\ u_{ds1} = 2U_{in}+\dfrac{I_p}{2(C_v+C_L)}(t-t_1)-\dfrac{L_{leak}[i_1(t_{1-})+i_2(t_{1-})]}{2\omega}\sin[\omega((t-t_1)] \\ u_{ds2} = \dfrac{L_{leak}[i_1(t_{1-})+i_2(t_{1-})]}{2\omega}\sin[\omega((t-t_1)]-\dfrac{I_p}{2(C_v+C_L)}(t-t_1) \end{cases} \tag{1}$$

where:

$$\omega = \frac{1}{\sqrt{2CL_{leak}+C_vL_{leak}+C_LL_{leak}}},\ I_p=i_1-i_2<0.$$

At t=t_2:

$$\begin{cases} i_1 = 0 \\ i_2 = -I_p \\ u_{cL1} = u_{cL2} = 0 \end{cases} \tag{2}$$

By solving Eqns. (1) and (2), the duration can be derived by:

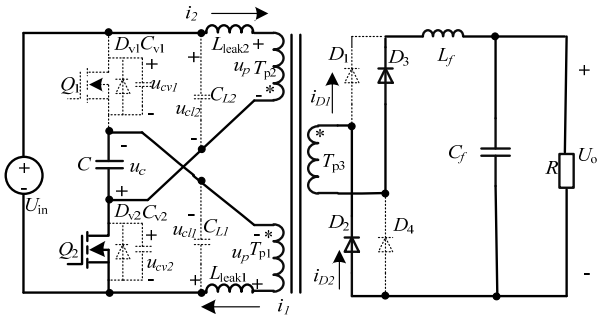
$$t_{12} = -\frac{2U_{in}(C_v+C_L)}{I_p} \tag{3}$$

C. Interval 2(Fig. 3(c): $t_2<t<t_3$)

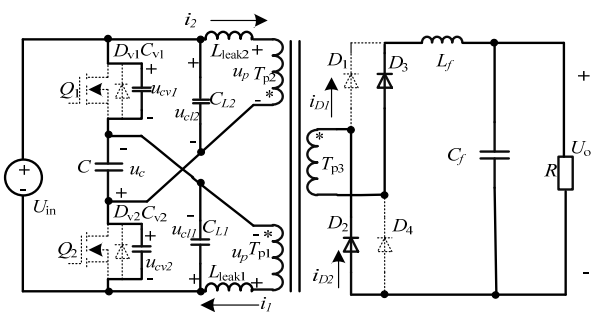
At t=t_2, the current i_1 decreases to zero reversely, and starts increasing. The capacitor C_{L1} can be charged by i_1. Meanwhile, the current i_2 continues decreasing and the capacitors C_{v2} and C_{L2} are charged. In this interval, the values of i_1 and i_2 are positive so that the rectifier diodes D_1~D_4 are conducting. Correspondingly, the current i_{D1} increases and i_{D2} decreases.

The second winding is in the freewheeling state. In this mode, the leakage inductor of the transformer L_{leak2} is resonant with the parallel resonant capacitors C_{L2} and the junction capacitors C_{v2}. At t=t_3, the voltage u_{cv2} increases to $2U_{in}$ and u_{cv1} reaches zero. The anti-parallel body diodes of the transistor Q_2 can be naturally conducted. According to the calculation method in interval 1, the equations for this interval are shown as:

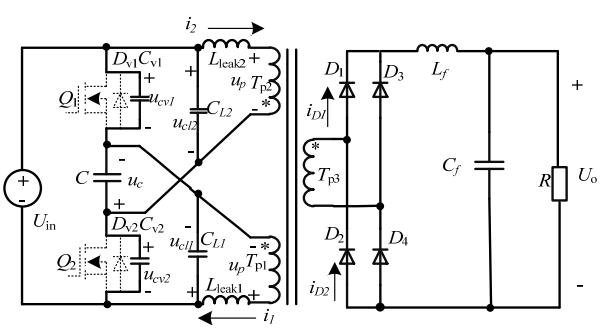
$$i_1 = \omega C(U_c-U_{in})\sin[\omega(t-t_2)]-\frac{I_p}{2}\cos[\omega(t-t_2)] + \frac{I_p}{2}\cos[\omega_1(t-t_2)] \tag{4a}$$



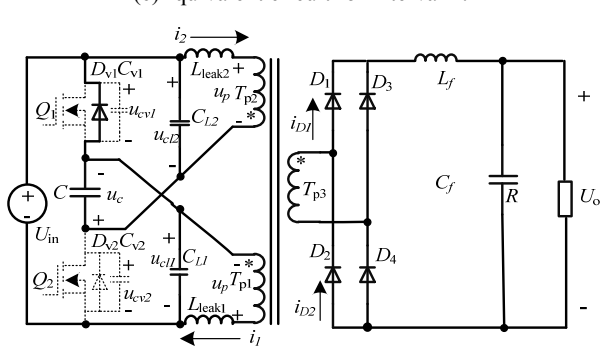
(a) Equivalent circuit for interval 0.



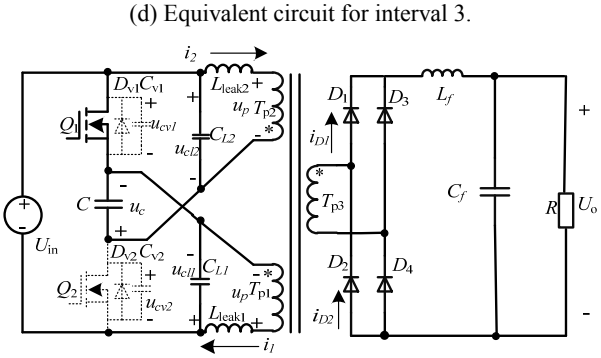
(b) Equivalent circuit for interval 1.



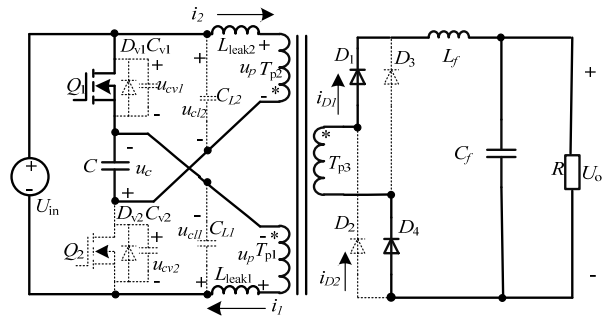
(c)Equivalent circuit for interval 2.



(d) Equivalent circuit for interval 3.



(e) Equivalent circuit for interval 4.



(f) Equivalent circuit for interval 5.

Fig. 3. Equivalent circuits during different intervals of the proposed converter.

$$i_2 = -\frac{I_p}{2}\cos[\omega(t-t_2)] - \frac{I_p}{2}\cos[\omega_1(t-t_2)] - \omega C(U_c - U_{in})\sin[\omega(t-t_2)] \tag{4b}$$

$$u_{ds1} = U_{in} - \frac{\omega L_{leak} I_p}{2}\sin[\omega(t-t_2)] + \frac{C(U_c - U_{in})}{2C + C_L + C_v}\cos[\omega(t-t_2)] + \frac{\omega_1 L_{leak} I_p}{2}\sin[\omega_1(t-t_2)] \tag{4c}$$

$$u_{ds2} = U_{in} - \frac{\omega L_{leak} I_p}{2}\sin[\omega(t-t_2)] + \frac{C(U_c - U_{in})}{2C + C_L + C_v}\cos[\omega(t-t_2)] + \frac{\omega_1 L_{leak} I_p}{2}\sin[\omega_1(t-t_2)] \tag{4d}$$

At the end of this mode, the voltage u_{ds1} reaches zero. As a result, the transistor Q_1 can achieve zero voltage turn on. Therefore, the duration of this interval is shown as:

$$t_{23} = \frac{[U_{in}(C + C_v + C_L) + CU_c](C_v + C_L)}{CI_p} \tag{5}$$

where:

$$U_c = U_{in} + \omega L_{leak}[i_1(t_{1-}) + i_2(t_{1-})]\sin[-\frac{2\omega U_{in}(C_v + C_L)}{I_p}] \tag{6}$$

D. Interval 3(Fig. 3(d): $t_3<t<t_4$)

At $t=t_3$, the anti-parallel body diode of the transistor D_{V1} is turned on. The clamp capacitor C acts on the leakage inductor of the primary winding T_{p2}. The voltage on the he leakage inductor of the winding T_{p1} is the voltage source U_{in}. The current i_2 is decreasing while i_1 is rapidly increasing. During this interval, the value of i_2 is still higher than i_1. This interval ends when the transistor Q_1 conducts.

E. Interval 4 (Fig. 3(e): $t_4<t<t_5$)

At $t=t_4$, the transistor Q_1 is conducting. The voltage u_{ds1} has dropped to zero before conducting Q_1. The procedure for the operation in this interval is similar to that in the last interval. The currents i_1 and i_2 through the transformer during this interval are determined as follows:

$$\begin{cases} i_1 = i_1(t_{4-}) + \dfrac{U_{in}}{L_{leak}}(t - t_4) \\ i_2 = i_2(t_{4-}) + \dfrac{U_c}{L_{leak}}(t - t_4) \end{cases} \tag{7}$$

During this interval, the current increases form $\frac{I_{Lf\min}}{1+i_2/i_1}$ to $I_{Lf\min}$. Therefore, the duration of this interval is shown as:

$$t_{45}=\frac{nL_{leak}I_{Lf\min}}{U_{in}[1+i_2(t_{4-})/i_1(t_{4-})]} \tag{8}$$

F. Interval 5 (Fig. 3(f): $t_5<t<t_6$)

The current i_2 reached zero at the end of the last interval. In this interval, the voltage across the winding T_{p2} is the clamp capacitor voltage U_c, and voltage across the winding T_{p1} is U_{in}. Therefore, the current i_2 begins to rise reversely. Meanwhile, i_1 increases rapidly. The rectifier diodes D_2 and D_3 are blocking. The equations for this interval are:

$$\begin{cases} i_1=i_1(t_{5-})+\dfrac{N^2U_{in}}{2L_{leak}}(t-t_5) \\ i_2=i_1(t_{5-})-\dfrac{N^2U_{in}}{2L_{leak}}(t-t_5) \\ u_{ds1}=2U_{in} \\ u_{ds2}=0 \end{cases} \tag{9}$$

This analysis has been carried out for the first half cycle, and the above intervals repeat in the same sequence with the other symmetrical devices conducting in the second half cycle.

III. CONVERTER DESIGN

A. Voltage and Current Stress of the Semiconductor Devices

The maximum voltage across the main power transistors Q_1 and Q_2 is $2U_{in}$. The rms current through the primary switches is shown as:

$$i_{Q1}=i_{Q2}=nP_0/\eta U_0 \tag{10}$$

where n is the turns ratio of the transformer, P_0 is the output power, U_o is the output voltage, and η is the conversion efficiency.

The RMS current through the rectifier diodes D_1-D_4 is given as:

$$I_{D1}=I_{D2}=I_{D3}=I_{D4}=P_0/2\eta U_0 \tag{11}$$

B. ZVS Realization Condition

Based on the above mentioned analysis, it can be concluded that when this circuit works in the stage of interval 1, the equivalent inductors of the primary windings, which originate from the transformation of L_{leak} and L_f, resonate with the parallel capacitor and parasitic capacitor. The energy saving in L_f is adequate to make the discharge voltage of C_{v2} decrease to zero, and is easy to achieve ZVS. However, when the circuit works in interval 2, only L_{leak}, the parallel capacitor and the parasitic capacitor resonate. Due to the fact that L_{leak} is far less than L_f, it is more difficult to achieve zero-voltage turn-on than zero-voltage turn-off for Q_1. As long as the novel topology meets the zero-voltage turn-on conditions, the ZVS for Q_1 and Q_2 can be accomplished.

Taking Q_1 as an example, it is necessary to ensure that u_{ds1}=0 before turning on the transistor Q_1 to achieve the zero-voltage turn-on for Q_1. According to interval 3, formula (5) can be used to calculate the time at which the voltage across C_{v1} decreases to zero from U_{in}. Thus, the dead-time is derived as:

$$t_d>t_{12}+t_{23}=-\frac{2U_{in}(C_v+C_L)}{I_p}+\frac{[U_{in}(C+C_v+C_L)+CU_c](C_v+C_L)}{CI_p} \tag{12}$$

where t_d is the dead-time.

In addition, the capacitor C_{L1}, C_{L2} and C_{v2} are charged by the energy saved in L_{leak1}. The energy has to be adequate to make the voltage u_{CL1} increase to U_{in} from 0, to make u_{CL2} decrease to U_{in} from 0, and to make u_{Cc2} increase to $2U_{in}$ from U_{in}. Thus, the energy condition to achieve ZVS is determined by:

$$E_{L_{leak}}\geqslant E_{C_{L1}}+E_{C_{L2}}+E_{C_{v2}} \tag{13}$$

$$L_{leak}(\frac{I_p}{2})^2>2\times\frac{C_L}{2}U_{in}^2+\frac{C_v}{2}[(2U_{in})^2-U_{in}^2] \tag{14}$$

Ignoring the current ripple, formula (13) can be derived as:

$$L_{leak}(\frac{P_0}{2\eta U_{in}D})^2>C_LU_{in}^2+\frac{3C_v}{2}U_{in}^2\Rightarrow \frac{L_{leak}}{4}(\frac{P_0}{\eta D})^2>C_LU_{in}^4+\frac{3C_v}{2}U_{in}^2 \tag{15}$$

Formulas (12) and (14) indicate that heavy loads and high leakage inductances are conducive to achieving ZVS.

C. Duty Cycle Loss

During interval 3, although the voltage across the primary transformer winding is positive, the current is too low to provide energy to the load. All of the rectifier diodes are conducting. As a result, the voltage across the secondary winding is zero, which produces duty cycle losses. During interval 1, the primary side is in the stage of dead-time. Meanwhile, due to parallel resonant capacitance, the currents i_1 and i_2 slowly decrease. Therefore, the voltage across the secondary winding is negative in mode1. Thus, the duty cycle loss in the novel ZVS PPFC can be lower than that in the conventional PPFC. The duty cycle loss can be shown as:

$$D_{loss}=\frac{2nL_{leak}I_{Lf\min}}{U_{in}T_s[1+i_2(t_{4-})/i_1(t_{4-})]}+\frac{4U_{in}(C_v+C_L)}{T_sI_p} \tag{16}$$

where T_s is switching period.

From formula (16), increases in the transformer leakage inductance increase the amount of D_{loss} in the converter. Thus, the parallel resonant capacitance C_L cannot be designed so large that it is not conducive to the ZVS of the transistors. Therefore, an appropriate L_{leak} needs to be appreciated.

D. Parameters of the Resonant Network

According to the ZVS realization condition, L_{leak} and C_L can be calculated when the main circuit parameters are determined.

1) Parallel Resonant Capacitor C: Assuming that the clamp capacitor C is large enough, the voltage across C (U_c) is constant (U_c=U_{in}). According to equation (12), the dead time t_d can be obtained by:

$$t_{d\min} \geq -\frac{4U_{in}(C_v + C_L)}{I_p} - \frac{U_{in}(C_v + C_L)^2}{I_p} \quad (17)$$

where t_{dmin}=10%T_s. T_s is the switching period.

The parallel resonant C_L can be calculated from (17) by:

$$C_{L\max} = \frac{C\sqrt{16U_{in}^2 - 4U_{in}t_{d\min}I_p / C}}{2U_{in}} - 2C \quad (18)$$

2) Leakage Inductance L_{leak}: According to C_L and equation (14), the leakage inductance L_{leak} can be expressed as:

$$L_{leak} \geq \frac{(4C_L + 9C_v / 2)\ U_{in}^4 \eta^2 D^2}{P_0^2} \quad (19)$$

As long as L_{leak} meets equation (19), where C_L reaches its maximum, the minimum of L_{leak} is given as:

$$L_{leak\min} = \frac{(4C_{L\max} + 9C_v / 2)\ U_{in}^4 \eta^2 D^2}{P_0^2} \quad (20)$$

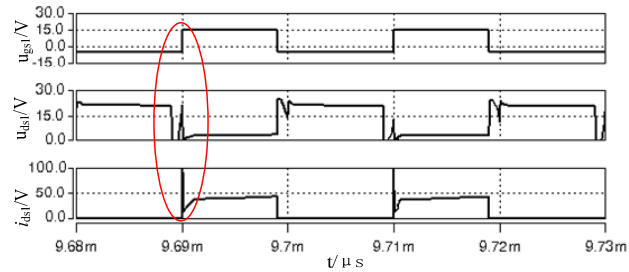
IV. The Simulation and Experimental Results

The conventional push-pull forward topology and the proposed push-pull forward topology have been simulated in Saber. The main specifications are U_{in}=10V to 14V, U_o=90V, P_0=500W and f=50KHz, with a light load output 20%P_0(100W). The main circuit parameters are C=10μF, the output filter capacitor C_f=470μF, the output filter inductor L_f=200μH, the dead time t_{dmin}=10%T_s, C_{Lmax}=2μF (according to formula (18)), and $L_{leak(min)}$=0.26μH (according to formula (19)).

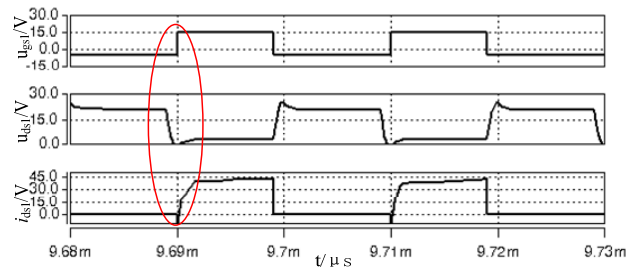
Simulation results are shown in Fig. 4 (a) and (b) to analyze the advantages of the novel push forward topology at P_0=500W. In addition, in order to verify the accuracy of the theoretical analysis and the ZVS conditions, simulations are implemented in various parallel resonant capacitors, leakage inductances and various loads. The simulation results are shown in Fig. 5 (a)-(e), and they include the drive signal u_{gs1}, the voltage u_{ds1} across Q_1 and the current through Q_1.

As shown in Fig. 4(a), at the moment of turning on the switch Q_1, u_{ds1} rises to U_{in}, and the conventional PPFC cannot achieve soft-switching. Furthermore, due to the existence of a parasitic capacitor, the high current spike of i_{ds1} is generated at the moment of turning on Q_1. However, as shown in Fig. 4(b), u_{ds1} decreased to zero before turning on Q_1 in the proposed ZVS PPFC. Thus, it can achieve zero voltage turning-on. When Q_1 turns off, due to the existence of a parallel resonant capacitance and a parasitic capacitor, u_{ds1} rises slowly from zero. Therefore, it can also achieve zero voltage turning-off, and the current through Q_1 has no spikes.

With a variety of parallel resonant capacitors but the same simulation parameters, simulation results are shown in Fig.



(a) u_{gs1},u_{ds1},i_{ds1} waveforms for conventional PPFC.



(b) u_{gs1},u_{ds1},i_{ds1} waveforms for the proposed novel ZVS PPFC.

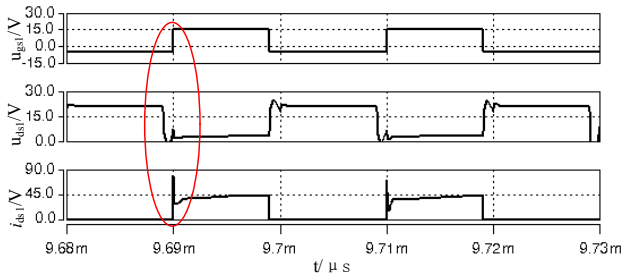
Fig. 4. Contrast simulation waveforms between conventional PPFC and the proposed novel ZVS PPFC at P_0=500W.

5(a) and (b). In Fig. 5(a), when C_L=0.1μF, the novel ZVS PPFC cannot achieve ZVS. This is because C_L is too small to satisfy formula (12). When C_L=0.5μF <C_{Lmax}, the voltage across C_{L1} reaches U_{in} before turning on Q_1. Thus, u_{ds1} can be clamped to zero, and it can achieve ZVS as shown in Fig. 5 (b). The simulation results show good agreement with the theoretical analysis.

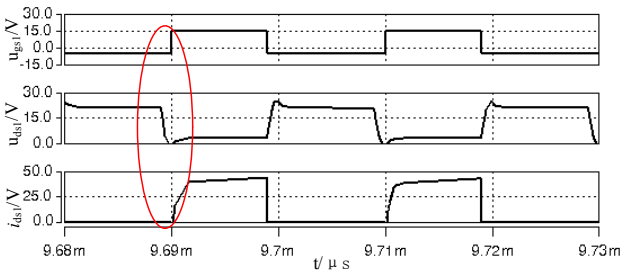
Simulation results with various leakage inductances are shown in Fig. 5(c) and (d). The greater the leakage inductance L_{Leak}, the more easily the ZVS can be achieved. However, when L_{leak}=0.1μH<$L_{leak(min)}$, the zero voltage turning-on cannot be achieved. This is consistent with formula (14). Furthermore, simulation results under the light load condition are given in Fig. 5(e). u_{ds1} decreases to zero at the moment of turning on Q_1. This is consistent with formula (15). Greater values of P_0 and L_{Leak} result in more energy being stored in the transformer leakage inductor. Energy charges the parallel resonate capacitor C_L until the voltage across C_L reaches U_{in}. As a result, the voltage u_{ds1} is clamped to zero. Therefore, under the load condition, the effect of ZVS is non-ideal compared with the full load condition.

The principal parameters and components are listed in Table I. A 500W experimental converter prototype has been built based on the above theoretical analysis and preliminary simulations, as shown in Fig. 6.

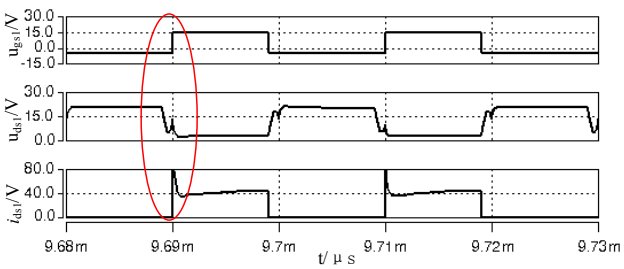
Experimental tests are performed prior to comparing the measured waveforms of the conventional push-pull forward converter and the novel push-pull forward converter under various load conditions to evaluate the advantages and disadvantages of the novel ZVS PPFC. The conventional push-pull forward converter experimental waveforms are shown in Fig. 7(a). It can be seen that the turn-off voltage



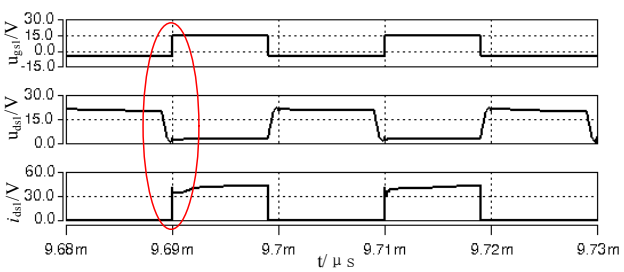
(a) C_L=0.1μF at P_0=500W.



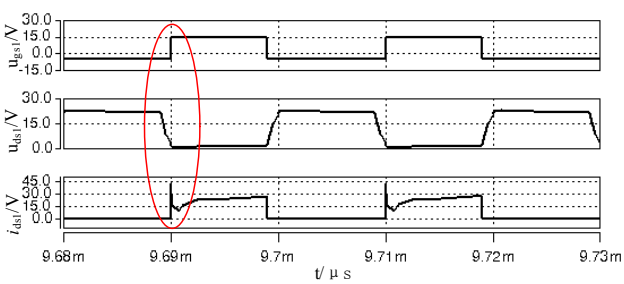
(b) C_L=0.5μF at P_0=500W.



(c) L_{Leak}=0.1μH at P_0=500W.



(d) L_{Leak}=0.2μH at P_0=500W.

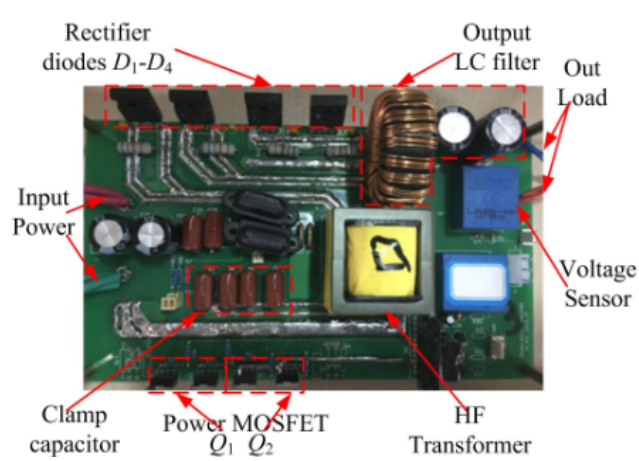


(e) C_L=0.5μF, L_{Leak}=0.1μH at P_0=100W.

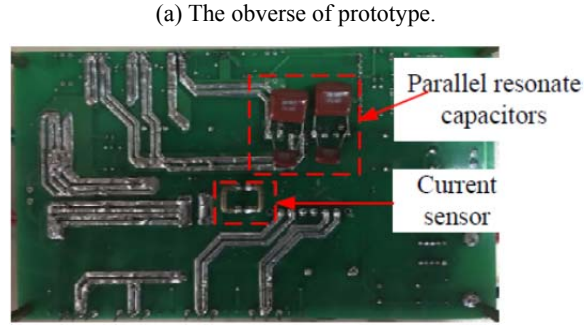
Fig. 5. u_{gs1},u_{ds1},i_{ds1} waveforms under different parameters conditions for the proposed novel ZVS PPFC.

TABLE I
PARAMETERS OF THE LABORATORY PROTOTYPE

Components	Parameters
Power Mosfets Q_1,Q_2	IRFB3607Pbf
Clamp capacitor C	10μF, 100V CBB capacitor,4 capacitors in parallels
Parallel resonate capacitor C_{L1}, C_{L2}	0.47μF and 0.1μF CBB capacitors in parallel
HF Transformer	EE4220/818/H ferrite core, Primary windings turns:n_1=n_2=2; secondary turns n_3=23;Leakge inductance referred to the primary L_{leak}=0.4μH
Rectifier diodes	MUR1005FCT
Output filter inductor L_f	200μH, 10A
Output filter inductor C_f	Two 470μF,200V electrolytic capacitors and 0.1μF 250V CBB capacitors



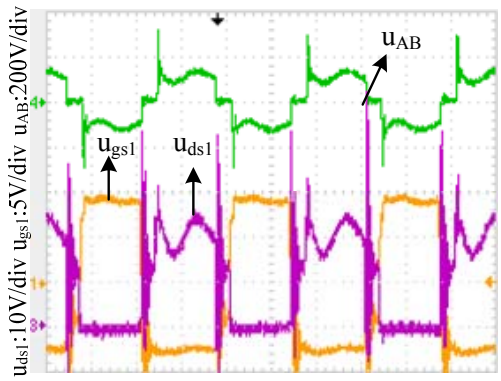
(a) The obverse of prototype.



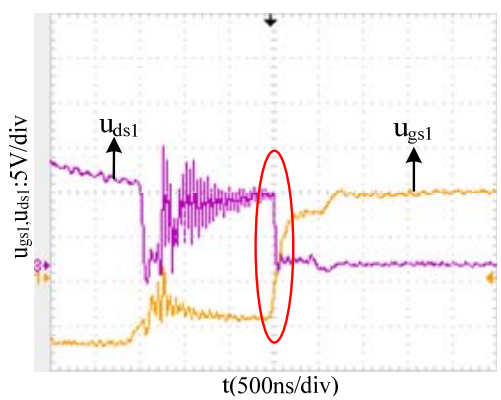
(b) The reverse side of prototype.

Fig. 6. 500W prototype of the proposed novel ZVS PPFC.

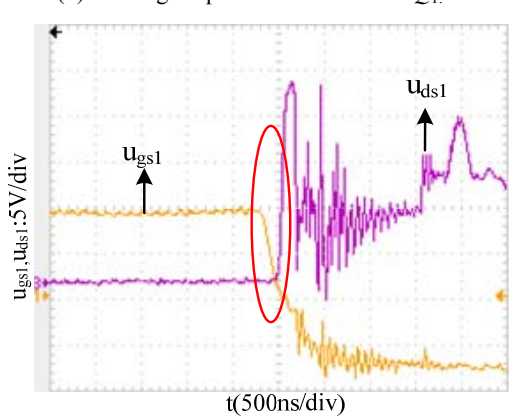
spike of Q_1 reaches 46V under the full load condition, which is more than twice $2U_{in}$. The voltage across the transformer secondary side u_{AB} exhibits high spikes (320V), which increase the requirements for the rectifier diodes. The switching loss also increases. Accordingly, high voltage



(a) u_{gs1},u_{ds1},u_{AB} waveforms for conventional PPFC.

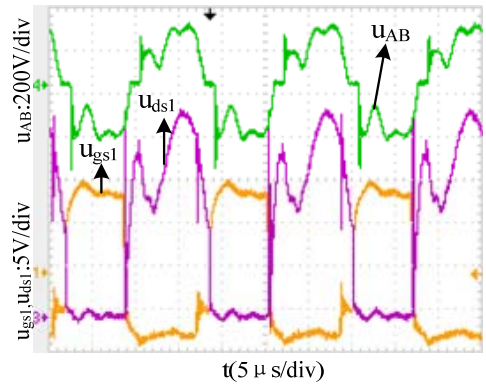


(b) Turning-on process for transistor Q_1.

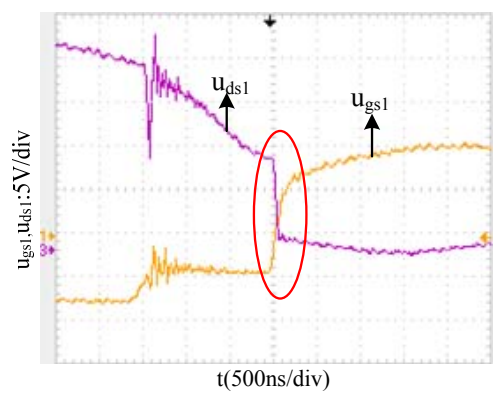


(c) Turning-off process for transistor Q_1.

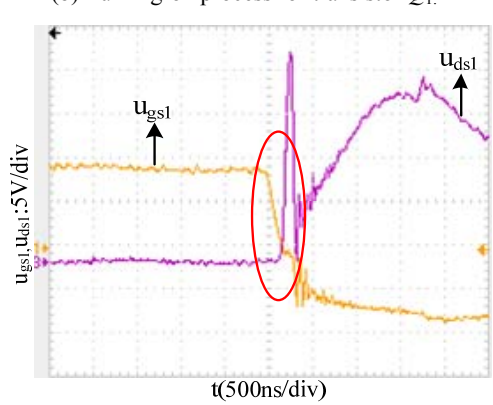
Fig. 7. Experimental waveforms for conventional PPFC at P_0=500W.



(a) u_{gs1},u_{ds1},u_{AB} waveforms at P_0=500W for the proposed novel ZVS PPFC.



(b) Turning-on process for transistor Q_1.



(c) Turning-off process for transistor Q_1.

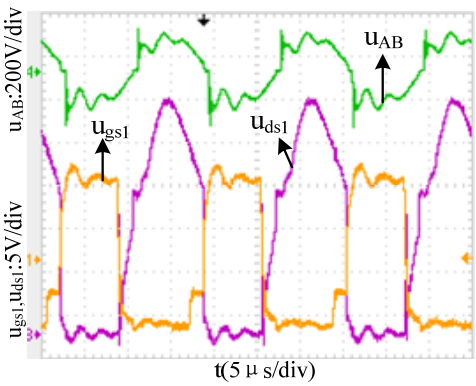
Fig. 8. Experimental waveforms for the proposed novel ZVS PPFC at L_{leak}=0.1μH (P_0=500W).

spikes damage the switching elements easily. The turning-on and turning-off processes for transistor Q_1 are shown in Fig. 7(b) and (c). The EMI is severe at the moment of turning on and turning off. Obviously, the turning-off voltage spike of transistor Q_1 approaches 46V because of the existence of leakage inductance.

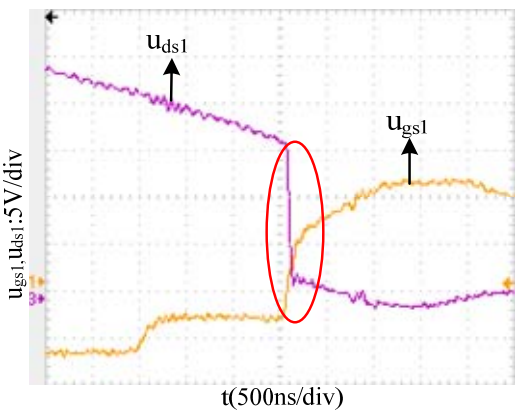
At the moment of turning off (Q_1), back electromotive force can be generated across the leakage inductance of the transformer. Therefore, the voltage u_{ds1} is higher than $2U_{in}$. A larger leakage inductance results in a higher turning-off voltage spike is for the conventional PPFC. Thus, ZVS for the transistor Q_1 cannot be achieved.

Fig. 8(a) presents the novel push-pull forward converter experiment results at L_{leak}=0.1μH and P_0=500W. It can be seen that the maximum value of the voltage across u_{ds1} is $2U_{in}$=24V under the full load condition.

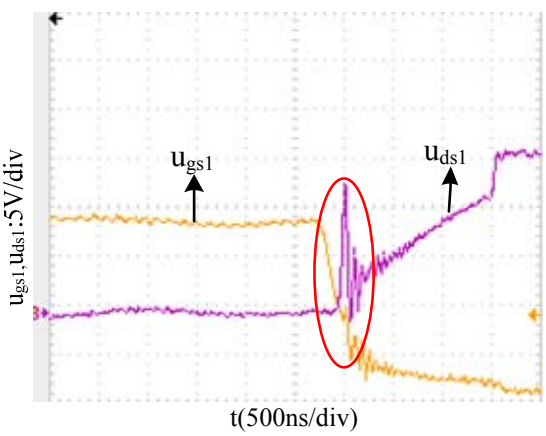
This demonstrates that the novel push-pull forward converter can eliminate the turn-off voltage spikes. Meanwhile, the maximum value of the secondary winding voltage u_{AB} is 250V. The voltage stress of the rectifier diodes



(a) u_{gs1},u_{ds1},u_{AB} waveforms at P_0=100W for the proposed novel ZVS PPFC.

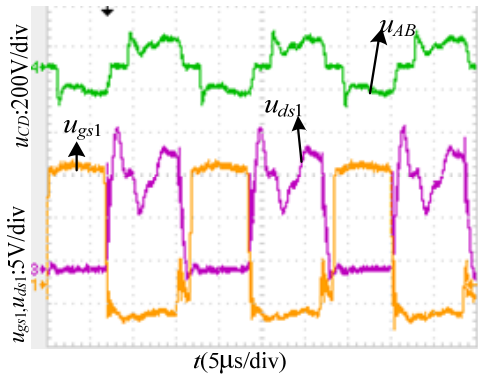


(b) turning-on process for transistor Q_1.

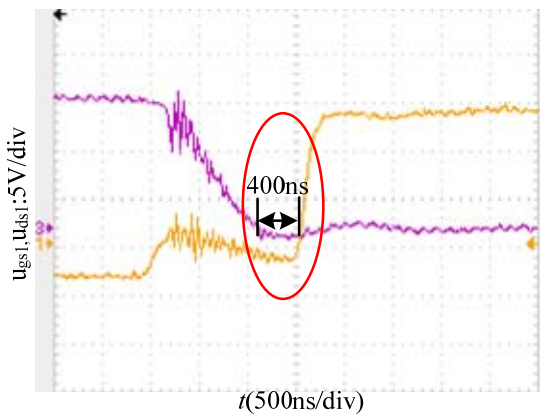


(c) turning-off process for transistor Q_1.

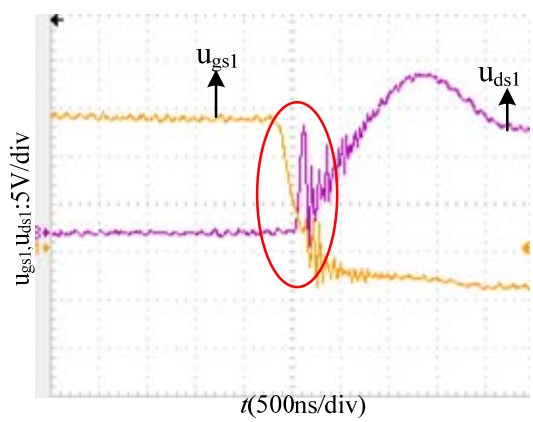
Fig. 9. Experimental waveforms for the proposed novel ZVS PPFC at P_0=100W.



(a) u_{gs1},u_{ds1},u_{AB} waveforms at L_{leak}=0.4μH for the proposed novel ZVS PPFC.



(b) Turning-on process for transistor Q_1.



(c) Turning-off process for transistor Q_1.

Fig. 10. Experimental waveforms for the proposed novel ZVS PPFC at L_{leak}=0.4μH (P_0=500W).

can be reduced. The EMI at the moment of turning-on and turning-off in Fig.8(b) and (c) are much smaller than those in Fig. 7(b) and (c) due to the introduction of the parallel capacitor C_L. Moreover, the voltage u_{ds1} decreases to zero before turning on Q_1. Similarly, the voltage u_{ds1} is kept at zero until the turning on of Q_1. Thereby, ZVS can be achieved.

The novel push-pull forward converter experiment results under the light load condition are shown in Fig. 9. As shown in Fig. 9(a), the maximum value of the voltage across u_{ds1} is $2U_{in}$=24V. Meanwhile, the maximum value of the transformer secondary voltage u_{AB} is 240V with lower voltage spikes. The duty cycle loss is reduced under the light load condition when compared with the full load condition. This meets formula (16). A smaller value of I_{Lfmin} results in a smaller D_{loss}. The processes of turning-on and turning-off are shown in Fig. 9 (b) and (c). It is still possible to achieve ZVS. Obviously, the novel push-pull forward converter can achieve ZVS over a wide load range.

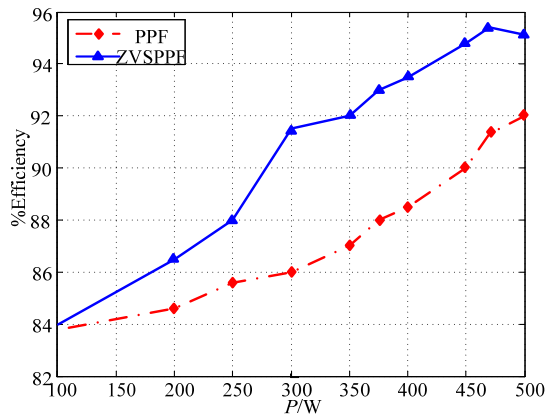


Fig. 11. Efficiency curve for conventional PPFC and the proposed novel ZVS PPFC.

Fig. 10(a) shows experimental results of the novel PPFC at L_{leak}=0.4μH and P_0=500W. There is no turn-off voltage spike for the transistor Q_1. The effect of the ZVS is remarkable. Nevertheless, the maximum voltage across the transistor Q_1 reaches 30V, which is higher than the theoretical value $2U_{in}$. This is because the clamp capacitor C is kept as a constant voltage source in the theoretical analyses (U_c=U_{in}). However, the voltage across C (U_c) is not a constant in practice, as depicted in formula (6). U_c is proportional to the transformer leakage inductance L_{leak}. Therefore, U_c increases with an increase of L_{leak}. u_{ds1}=U_{in}+U_c > 24V at L_{leak}=0.4μH. The turn-on and turn-off processes of the transistor Q_1 are shown in Fig. 10 (b) and (c), respectively.

Obviously, u_{ds1} decreases to zero at 400ns before turning on Q_1. In addition, the turn-off voltage spike of Q_1 is eliminated. Compared with Fig. 8(a), the dead time of the voltage u_{CD} across the secondary wingding is longer in Fig. 10(a). Correspondingly, D_{loss} increases and the voltage gain of the converter decreases. This results in a trade off in terms of the efficiency improvement. Therefore, a compromise is needed between ZVS and high efficiency.

The novel PPFC efficiency curve is shown in Fig.11. Compared with the conventional PPFC, the efficiency of the proposed novel push-pull forward converter is 2 percent higher than that of the conventional push-pull forward converter. The maximum efficiency of the novel PPFC approaches 95.4% at P=470W. The efficiency is 94.8% at P=500W. From 400W to 500W, the converter efficiency is always over 93%. Therefore, the novel push-pull forward converter can achieve a high efficiency over a wide load range.

V. Conclusion

A novel zero voltage switching (ZVS) push-pull forward converter is proposed in this paper. It exhibits a simple topology that only needs to parallel two parallel capacitors across each of the primary windings. In addition, its control strategy is the same as that in the conventional push-pull forward converter. A 500W experimental converter prototype has been built and the conclusions are drawn as follows:

1) The novel zero voltage switching (ZVS) push-pull forward converter has the advantages of the conventional push-pull forward converter, along with the ability to reduce or even eliminate the cut-off voltage spikes.
2) The proposed converter topology can operate in the ZVS mode over a wide load range. It is conducive to improving the efficiency and increasing the switching frequency.
3) The converter proposed in this paper can reduce the duty cycle loss and improve the voltage gain.

Acknowledgment

This work was supported in part by the Scientific and technological project of Shandong Province (2013GGX10502), by China Postdoctoral Science Foundation (2014M560259), by Innovation Foundation of Harbin institute of technology (HIT.NSRIF.2016097).

References

[1] X. Zhou, B. Yang, L. Amoroso, F. C. Lee, and P. Wong, “A novel high input voltage, high efficiency and fast transient voltage regulator module-push-pull forward converter,” *IEEE Applied Power Electronics Conference (APEC)*, Vol. 1, pp.279-283, Mar. 1999.

[2] P. Xu, M. Ye, P. Wong, and F. C. Lee, “Design of 48 V voltage regulator modules with a novel integrated magnetics,” *IEEE Trans. Power Electron.,* Vol. 17, No. 6, pp. 990-998, Nov. 2002.

[3] J. Cruz, M. Castilla, J. Mire, J. Matas, and J. M. Guerrero, “Averaged large-signal model of single magnetic push-pull forward converter with built-in input filter,” *IEEE International Symposium on Industrial Electronics (ISIE)*, Vol. 2, pp. 1023-1028, May 2004.

[4] Y.B. Xia, H.F. Wu, W. Liu, Y. Xing, and X. D. Ma, “A novel push-pull forward converter for high reliability and high input voltage applications,” *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2506-2511, Sep. 2011.

[5] X. B. Ruan, B. Li, Q. H. Chen, S. C. Tan, and C. K. Tse, “Fundamental considerations of three-level DC–DC converters: Topologies, analyses, and control,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 55, No. 11, pp. 3733-3743, Dec. 2008.

[6] Z. L. Yao and L. Xiao, “Push-pull forward three-level DC/DC converter with reduced rectifier voltage stress,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol.57, No. 10, pp. 2815-2821, Oct. 2010.

[7] Z. L. Yao, G. W. Hu, and J. R. Kan, “Improved push-pull forward three-level converter,” *Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, pp. 1-4, Mar. 2012.

[8] R. Ayyanar and N. Mohan, “Novel soft-switching DC-DC converter with full ZVS-range and reduced filter

requirement. I. Regulated-output applications," *IEEE Trans. Power Electron.*, Vol. 16, No. 2, pp. 184-192, Mar. 2001.

[9] S. Hamada and M. Nakaoka, "A novel zero-voltage and zero-current switching PWM DC-DC converter with reduced conduction losses," *IEEE Trans. Power Electron.*, Vol. 17, No. 3, pp. 413-419, May 2002.

[10] M. J. Ryan, W. E. Brumsickle, D. M. Divan, and R. D. Lorenz, "A new ZVS LCL-resonant push-pull DC-DC converter topology," *IEEE Trans. Power Electron.,* Vol. 34, No. 5, pp. 1164-1174, Sep. 1998.

[11] C.-L. Chu and C.-H. Li, "Analysis and design of a current-fed zero-voltage-switching and zero-current-switching CL-resonant push-pull dc-dc converter," *IET Power Electron.*, Vol. 2, No. 4, pp. 456-465, Jul. 2009.

[12] T. F. Wu, J. C. Hung, J. T. Tsai, and C. T. Tsai, "An active-clamp push–pull converter for battery sourcing applications," *IEEE Trans. Ind. Appl.*, Vol. 44, No.1, pp. 196-204, Jan./Feb. 2008.

[13] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 3, pp. 881-891, Mar. 2010.

[14] S. Yu, M. Q. Nguyen, and W. Choi, "A novel soft-switching battery charge/discharge converter with the zero voltage discharge function," *IEEE Trans. Power Electron.,* Vol.31 No.7, pp. 5067-5078, Jul. 2016.

[15] D. S. Sha, Q. W. Lin, F. L. You, X. Wang, and G. Xu, "A ZVS bidirectional three-level DC–DC converter with direct current slew rate control of leakage inductance current," *IEEE Trans. Ind. Appl.*, Vol. 52, No.3, pp. 2368-2377, May/Jun. 2016.

[16] Z. Zhang, O. C. Thomsen, and M. A. E. Andersen, "Optimal design of a push-pull-forward half-bridge (PPFHB) bidirectional DC-DC converter with variable input voltage," *IEEE Trans. Ind. Elec.*, Vol. 59, No. 7, pp. 2761-2770, Jul. 2012.

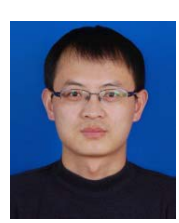
[17] Z. L. Yao and L. Xiao, "Family of zero-voltage-switching unregulated isolated step-up DC-DC converters," *IET Power Electron.* , Vol. 6, No. 5, pp. 862-868, May 2013.

Chunwei Cai was born in Shandong, China, in 1977. He received his B.S. and M.S. degrees in Control Theory and Control Engineering from Shan Dong University, Jinan, China, in 2001 and 2004, respectively; and his Ph.D. degree in Electrical Engineering from Harbin Institute of Technology, Harbin, China, in 2013. In 2006, he became a Lecturer in Harbin Institute of Technology, Weihai, China. Since 2014, he has been working as an Assistant Professor in the Harbin Institute of Technology at Weihai. His current research interests include power converters, inverters and wireless power transfer systems.

Chunyu Shi was born in Heilongjiang, China, in 1991. She received her B.S. degree in Electrical Engineering and Automation from the Changchun University of Science and Technology, Changchun, China, in 2014; and her M.S. degree in Electrical Engineering from Harbin Institute of Technology, Weihai, China, in 2016. She is presently working as a Research Engineer of ultra-capacitor energy storage systems in the CRRC Qingdao Sifang Rolling Stock Research Institute Co., Ltd., Qingdao, China. Her current research interests include DC-DC converters.

Yuxing Guo was born in China, in 1993. He received his B.S. degree in Electrical Engineering and Automation from Harbin University of Science and Technology, Harbin, China, in 2015. He is presently working toward his M.S. degree in Electrical Engineering in the Academy of Information and Electrical Engineering, Harbin Institute of Technology, Weihai, China. His current research interests include power electronics, electric drives and the control of power systems.

Zi Yang was born in China, in 1995. He received his B.S. degree in Electrical Engineering and Automation from Harbin Institute of Technology, Weihai, China, in 2016. He is presently working toward his M.S. degree in the Institute of Power Electronics and Power Drives, Harbin Institute of Technology. His current research interests include power electronics, electric drives and wireless power transmission.



Fangang Meng was born in Shandong, China, in 1982. He received his B.S. degree in Thermal Energy and Power Engineering, and his M.S. and Ph.D. degrees in Electrical Engineering from Harbin Institute of Technology, Harbin, China, in 2005, 2007 and 2011, respectively. His current research interests include harmonic detection, the stability analysis of converters and high power rectification.