JPE 17-1-26

Performance Analysis of Three-Phase Phase-Locked Loops for Distorted and Unbalanced Grids

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Abstract

This paper studies the performances of five typical Phase-locked Loops (PLLs) for distorted and unbalanced grid, which are the Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL), Double Second-Order Generalized Integrator PLL (DSOGI-PLL), Double Second-Order Generalized Integrator Frequency-Lock Loop (DSOGI-FLL), Double Inverse Park Transformation PLL (DIPT-PLL) and Complex Coefficient Filter based PLL (CCF-PLL). Firstly, the principles of each method are meticulously analyzed and their unified small-signal models are proposed to reveal their interior relations and design control parameters. Then the performances are compared by simulations and experiments to investigate their dynamic and steady-state performances under the conditions of a grid voltage with a negative sequence component, a voltage drop and a frequency step. Finally, the merits and drawbacks of each PLL are given. The compared results provide a guide for the application of current control, low voltage ride through (LVRT), and unintentional islanding detection.

Key words: Distorted grid, Small-signal model, Three-phase phase-locked loop, Unbalanced grid

I. INTRODUCTION

Inverters always play an important role as an interface for integrating renewable energy sources into utility grid [1], [2]. Inverters need to quickly and precisely measure the amplitude, frequency and phase of the grid's voltage in complex situations. The three-phase phase-locked loop is an effective method for obtaining information about grid voltage. The conventional three-phase PLL is based on the single synchronous reference frame phase-locked loop (SSRF-PLL) [3], [4]. This method can efficiently extract grid voltage information regarding the amplitude, phase and frequency of voltage when the grid is balanced. However, when the grid voltage is distorted, the phase detected by a SRF-PLL is greatly influenced by the negative sequence component. Although reducing the system bandwidth can attenuate the second orders harmonic, the system response performance is deteriorated [5]-[8]. Therefore, it is essential to develop and research methods to implement a

PLL for distorted grid.

Many studies have been conducted on three-phase PLL methods for distorted grid operating conditions. [8] and [9] proposed a Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL). The DDSRF-PLL is based on positive and negative sequence double synchronous reference frames and can effectively eliminate the adverse effects of 2nd-orders harmonic. Double Second-Order Generalized Integrator PLL (DSOGI-PLL) is proposed in [10], which implements harmonic filters and an orthogonal signal generation by using an adaptive filter with the Double Second-Order Generalized Integrator (DSOGI) based Quadrature Signal Generator (QSG). In this method, the positive and negative sequence components are obtained by applying the instantaneous symmetrical components method. Hence, the grid's voltage amplitude, phase and frequency can be acquired by the conventional SRF-PLL from the obtained positive sequence component. However, the interlaced frequency and phase feedbacks in the DSOGI-PLL lead to a relatively large overshot and a long settling time. In order to overcome these drawbacks, a Double Second-Order Generalized Integrator Frequency-Lock Loop (DSOGI-FLL) method is presented in [11]. A Double Inverse Park Transformation PLL (DIPT-PLL) method was proposed in [12] and [13]. In this method, inverse Park transformation

Manuscript received Apr. 19, 2016; accepted Sep. 7, 2016. Recommended for publication by Associate Editor Jae-Do Park.

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based quadrature signal generation is applied to obtain the orthogonal signal of the input signal. Meanwhile, the symmetrical component method is implemented to extract the positive and negative sequence components of the three-phase voltage. A Complex Coefficient Filter based PLL (CCF-PLL) is proposed in [14], which uses the relationship among the grid's components to implement a complex coefficient filter and to obtain the final positive sequence component in the fundamental frequency. The methods mentioned above are five typical PLLs for distorted and unbalanced grids. There are also many modified or improved PLLs based on these five typical PLLs, for example, the DSOGI-PLL with frequency-tracking [15], Multiple-SOGI-FLL (MSOGIFLL) [16], [17] and so on. However, these five PLLs are fundamental and typical. Their structures are different and their performances also differ. Thus, it is essential to analyze and compare their performances. Furthermore, different applications have different requirements for PLLs. The current control of an inverter requires the precise and steadily phase angle of the grid voltage. For Low Voltage Ride Through (LVRT) applications, the positive sequence D-component has to be detected quickly. In applications for unintentional islanding detection, frequency detection needs to be accurate and smooth. Hence, it is critical to find out how to determine the scenario in practical applications.

This paper studies the performances of the five above mentioned typical three-phase PLL methods in different distorted grid conditions. A unified small-signal model is analyzed and its parameters are designed. Its performance in steady and dynamic states are compared in simulations and experiments. Finally, a guide line is given in the conclusion.

II. THREE-PHASE PHASE-LOCK LOOP SYNCHRONIZATION TECHNIQUE

A. Decoupled Double Synchronous Reference Frame PLL

The scheme of the DDSRF-PLL is shown in Fig.1. The DDSRF-PLL is based on two synchronous reference frames that rotate with positive and negative sequence synchronous speeds, respectively. The 2nd-order harmonic in the positive sequence component caused by the negative sequence component can be eliminated by cross decoupling. The decoupling network can eliminate harmonics from both the positive and negative sequence components [18]. Compared with the SRF-PLL, the DDSRF-PLL does not have to reduce the bandwidth in order to eliminate the influence of negative sequence components. However, this decoupling network is mainly aimed at positive and negative sequence components at the fundamental frequency. Thus, extra filters are needed when the grid voltage is disturbed by higher-order harmonics.

The transfer function of the low pass filters is given by:

$$LPF(s) = \frac{\omega_f}{s + \omega_f} \tag{1}$$



Fig. 1. The scheme of DDSRF-PLL.

where, *s* is the Laplace operator, and ω_f is the cutoff frequency of the low pass filter.

According to Fig.1, the following equations can be obtained.

$$\overset{-+}{v_{dq}} = LPF(t) \times \left(\overset{+}{v_{dq}} - T_{dq^{+2}} \times \overset{--}{v_{dq}} \right)$$
(2)

$$\overline{v_{dq}} = LPF(t) \times \left(\widetilde{v_{dq}} - T_{dq^{-2}} \times \overline{v_{dq}}\right)$$
(3)

where, the symbols d and q refer to the dq components in the D-Q synchronous reference frames, the symbols + and – refer to the positive and negative components, and the upper symbols – and ~ refer to the DC and AC components, respectively.

The result can be simplified into the $\alpha\beta$ stationary reference frame.

$$v_{\alpha\beta}^{+} = T_{dq^{-1}} \times LPF(t) \times T_{dq^{+1}} \left(v_{\alpha\beta} - v_{\alpha\beta}^{-} \right) \tag{4}$$

$$v_{\alpha\beta}^{-} = T_{dq^{+1}} \times LPF(t) \times T_{dq^{-1}} \left(v_{\alpha\beta} - v_{\alpha\beta}^{+} \right)$$
(5)

$$T_{dq^{+n}} = T_{dq^{-n}}^{T} = \begin{bmatrix} \cos(n\omega t) & \sin(n\omega t) \\ -\sin(n\omega t) & \cos(n\omega t) \end{bmatrix}$$
(6)

where, the symbol α and β refer to the $\alpha\beta$ components in the α - β stationary reference frames, respectively.

The following equations can be obtained by adopting Laplace transformation to (4) and (5):

$$v_{\alpha\beta}^{+}(s) = H(s) \left(v_{\alpha\beta}(s) - \bar{v_{\alpha\beta}}(s) \right)$$
(7)

$$v_{\alpha\beta}^{-}(s) = H(s) \Big(v_{\alpha\beta}(s) - v_{\alpha\beta}^{+}(s) \Big)$$
(8)

$$[H(s)] = \frac{\omega_f}{(s+\omega_f)^2 + {\omega'}^2} \begin{bmatrix} s+\omega_f & -\omega' \\ \omega' & s+\omega_f \end{bmatrix}$$
(9)

where, ω ' is the frequency of the positive sequence component.

By substituting (8) and (9) into (7), the relationship between the positive sequence component and input voltage in the $\alpha\beta$ stationary reference frame can be obtained as follows:

$$v_{\alpha\beta^{+}} = \frac{\omega_{f}}{s^{2} + 2\omega_{f}s + \omega^{\prime 2}} \begin{bmatrix} s & -\omega^{\prime} \\ \omega^{\prime} & s \end{bmatrix} v_{\alpha\beta}$$
(10)



Fig. 2. The scheme of DSOGI-PLL.

B. Double Second-Order Generalized Integrator PLL and FLL

The scheme of the DSOGI-PLL is shown in Fig.2. The DSOGI-PLL is based on an instantaneous symmetrical component method. In this method, the Second-Order Generalized Integrator (SOGI) based Quadrature Signal Generator (SOGI-QSG) module can filter the harmonics first. Then, the decoupled positive and negative sequence components at the fundamental frequency can be obtained after the Positive and Negative Calculation (PNSC) [19]-[20]. The phase and frequency of the positive sequence component at the fundamental frequency can be obtained by the SRF-PLL.

The transfer function of the SOGI-QSG can be obtained from Fig.2.

$$D(s) = \frac{v'_{\alpha\beta}}{v_{\alpha\beta}}(s) = \frac{k\omega's}{s^2 + k\omega's + {\omega'}^2}$$
(11)

$$Q(s) = \frac{qv'_{\alpha\beta}}{v_{\alpha\beta}}(s) = \frac{k\omega'^2}{s^2 + k\omega's + \omega'^2}$$
(12)

where, k is the gain of the error signal.

The SOGI-PLL is based on the frequency feedback ω ' and phase feedback θ . Because of the interleaved frequency and phase feedback loops, there is a relatively large overshot and a long settling time in the dynamic response. Therefore, a Frequency-Locked Loop (FLL) is used to instead of PLL in detecting the frequency [21]. The SOGI-FLL scheme is shown in Fig.3.

The gain $-\Gamma$ is utilized to normalize the positive sequence component's square of the input signal. Compared to the DSOGI-PLL, the DSOGI-FLL relies solely on the frequency feedback. Thus, the adaptability of the input signal's frequency can be achieved.

The transfer function of the DSOGI-PLL can also be obtained. The process of the calculation is shown in the appendix. In the two-phase $\alpha\beta$ stationary reference frame, the



Fig. 3. The scheme of DSOGI-FLL.

relationship between the positive sequence component and input voltage can be obtained as follows:

$$v_{\alpha\beta}^{+} = \begin{bmatrix} T_{\alpha\beta+} \end{bmatrix} v_{\alpha\beta} = \frac{1}{2} \begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix} v_{\alpha\beta}$$
$$= \frac{1}{2} \frac{k\omega'}{s^{2} + k\omega's + \omega'^{2}} \begin{bmatrix} s & -\omega' \\ \omega' & s \end{bmatrix} v_{\alpha\beta}$$
(13)

C. Double Inverse Park Transformation PLL

The scheme of the DIPT-PLL is shown in Fig.4. The DIPT-PLL uses two Inverse Park Transformation based Quadrature Signal Generator (IPT-QSG) modules to remove the negative affection caused by harmonics. Additionally, the obtained component at the fundamental frequency and its orthogonal component can be processed by the PNSC module to acquire the positive and negative sequence components at the fundamental frequency. Similarly, the phase and frequency of the positive sequence component at the fundamental frequency can be obtained by the SRF-PLL.

The transfer function of the low pass filter is given by:

$$LPF(s) = \frac{\omega_f'}{s + \omega_f'} \tag{14}$$

where, ω_f is the cutoff frequency of the low pass filter.

The transfer function of the IPT-QSG can be obtained from Fig.4.

$$D(s) = \frac{V_{\alpha}'}{V_{\alpha}}(s) = \frac{n\omega's}{s^2 + n\omega's + {\omega'}^2}; \ n = \frac{\omega_f'}{\omega'}$$
(15)

$$Q(s) = \frac{V_{\beta}}{V_{\alpha}}(s) = \frac{n\omega'^2}{s^2 + n\omega's + \omega'^2}; \ n = \frac{\omega_f'}{\omega'}$$
(16)

As shown in Fig.4, the DIPT-PLL is based on the phase feedback and can accurately detect the phase and frequency information of distorted grid.

Similarly, the relationship between the positive sequence component and the input component in the two-phase stationary reference frame is given by:



Fig. 4. The scheme of DIPT-FLL.



Fig. 5. The scheme of CCF-PLL.

$$v_{\alpha\beta}^{+} = \begin{bmatrix} T_{\alpha\beta+} \end{bmatrix} v_{\alpha\beta} = \frac{1}{2} \begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix} v_{\alpha\beta}$$
$$= \frac{1}{2} \frac{n\omega'}{s^{2} + n\omega's + \omega'^{2}} \begin{bmatrix} s & -\omega' \\ \omega' & s \end{bmatrix} v_{\alpha\beta} .$$
(17)

D. Complex Coefficient-Filter-Based PLL

The scheme of the CCF-PLL is shown in Fig.5. The CCF-PLL consists of a CCF module and a SRF-PLL module. The implementation structure of the CCF module is shown in Fig.6.

From Fig.5 and Fig.6, the transfer function of the positive sequence component extracted by the CCF-PLL can be obtained as follows:

$$v_{\alpha}^{+}(s) = \frac{\omega_{c}}{s + \omega_{c}} \left(v_{\alpha}(s) - v_{\alpha}^{-}(s) \right) - \frac{\omega'}{s + \omega_{c}} v_{\beta}^{+}(s)$$
(18)

$$v_{\beta}^{+}(s) = \frac{\omega_{c}}{s+\omega_{c}} \left(v_{\beta}(s) - \overline{v_{\beta}}(s) \right) - \frac{\omega'}{s+\omega_{c}} v_{\alpha}^{+}(s)$$
(19)

where, ω_c is a constant, and ω is the band-pass frequency.

From (18) and (19), the following equations can be obtained.

$$\begin{bmatrix} v_{\alpha}^{+}(s) \\ v_{\beta}^{+}(s) \end{bmatrix} = \frac{\omega_{c}}{(s+\omega_{c})^{2}+\omega^{\prime^{2}}} \begin{bmatrix} s+\omega_{c} & -\omega^{\prime} \\ \omega^{\prime} & s+\omega_{c} \end{bmatrix} \begin{bmatrix} v_{\alpha}(s)-v_{\alpha}^{-}(s) \\ v_{\beta}(s)-v_{\beta}^{-}(s) \end{bmatrix}$$
(20)



 $\begin{bmatrix} v_{\alpha}^{-}(s) \\ v_{\beta}^{-}(s) \end{bmatrix} = \frac{\omega_{c}}{(s+\omega_{c})^{2}+{\omega'}^{2}} \begin{bmatrix} s+\omega_{c} & \omega' \\ -\omega' & s+\omega_{c} \end{bmatrix} \begin{bmatrix} v_{\alpha}(s)-v_{\alpha}^{+}(s) \\ v_{\beta}(s)-v_{\beta}^{+}(s) \end{bmatrix}$ (21)

According equations (20) and (21), the relationship between the positive sequence component and the input voltage can be obtained as follows:

$$v_{\alpha\beta}^{+}(s) = \frac{\omega_{c}}{s^{2} + 2\omega_{c}s + {\omega'}^{2}} \begin{bmatrix} s & -\omega' \\ \omega' & s \end{bmatrix} v_{\alpha\beta}(s)$$
(22)

III. PARAMETER DESIGN AND ANALYSIS

A. Equivalence Analysis

According to the analysis in Section II, the five typical PLL methods can acquire the grid information regarding the amplitude, phase and frequency of the voltage when the grid is unbalance. From the transfer functions (10), (13), (17) and (22), the relationships between positive sequence component and input voltage have the same form but with different structures. Equation (23) is considered to be the general transfer function of the module extracting the positive sequence component:

$$v_{\alpha\beta}^{+} = \frac{1}{2} \frac{g\omega'}{s^{2} + g\omega's + {\omega'}^{2}} \begin{bmatrix} s & -\omega' \\ \omega' & s \end{bmatrix} v_{\alpha\beta}$$
(23)

where, g is the normalized factor for various PLLs.

In order to analyze the frequency response, Equation (24) is obtained by substituting $s = j\omega$ into (23):

$$\begin{bmatrix} v_{\alpha}^{+} \\ v_{\beta}^{+} \end{bmatrix} = \frac{1}{2} \frac{g\omega'}{(\omega'^{2} - \omega^{2}) + jg\omega'\omega} \begin{bmatrix} j\omega & -\omega' \\ \omega' & j\omega \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix}$$
(24)

It is known that the following equations can be obtained in the frequency domain:

$$v_{\alpha}(j\omega) = jv_{\beta}(j\omega); v_{\beta}(j\omega) = -jv_{\alpha}(j\omega)$$
(25)

Thus, according to (24) and (25), (26) can be obtained as:

$$\begin{bmatrix} v_{\alpha}^{+} \\ v_{\beta}^{+} \end{bmatrix} = \frac{1}{2} \frac{g\omega'(\omega' + \omega)}{j(\omega^{2} - \omega'^{2}) + g\omega'\omega} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix}$$
(26)

From (26), the relationship between the amplitude of the measured positive sequence component and the actual amplitude of the input voltage can be acquired as follows:



g. 7. Frequency response of $P(j\omega)$ and $N(j\omega)$.

$$P(j\omega) = \left| v_{\alpha\beta}^{+} \right| / \left| v_{\alpha\beta} \right| = \frac{1}{2} \frac{g\omega'(\omega' + \omega)}{j(\omega^{2} - \omega'^{2}) + g\omega'\omega}$$
(27)

The relationship between the amplitude of the measured negative sequence component and the actual amplitude of the input voltage is given as follows:

$$N(j\omega) = \left| v_{\alpha\beta}^{-} \right| / \left| v_{\alpha\beta} \right| = \frac{1}{2} \frac{g\omega'(\omega' - \omega)}{j(\omega^{2} - \omega'^{2}) - g\omega'\omega}$$
(28)

The magnitude-frequency characteristic of (27) and (28) are shown in Fig.7. (Note that $g=\sqrt{2}$)

As shown in Fig.7, $P(j\omega)$ functions as a low pass filter. The cutoff frequency is the fundamental frequency ($\omega/\omega' = 1$). $N(j\omega)$ functions as a notch filter. The center frequency is the fundamental frequency ($\omega/\omega' = 1$).

B. Small-Signal Model Analysis

Three-phase voltage can be converted into DQ components in the synchronous rotational reference frame by a Park transformation. When the PLL locks the phase of the input signal, the DQ components can be seen as the sum of the DC component and the AC disturbance component under distorted grid conditions, as shown in (29).

$$\begin{bmatrix} v_{d}(t) \\ v_{q}(t) \end{bmatrix} \cong \begin{bmatrix} \overline{v}_{d} \\ \overline{v}_{q} \end{bmatrix} + \begin{bmatrix} \widetilde{v}_{d}(t) \\ \widetilde{v}_{q}(t) \end{bmatrix}$$
DC component AC disturbance component (29)

where, \overline{v}_d and \overline{v}_q are the DC components, \tilde{v}_d and \tilde{v}_q are the AC component.

According to the analysis above, a unified small signal model of the five methods can be obtain as shown in Fig. 8. where, k_n and k_i are the PI parameters.

In general, the harmonics of grid voltage mainly consist of the odd harmonics of non-THG (three-times harmonic generation) harmonic sequences, such as the 5th, 7th, 9th and 11th order harmonics. In the synchronous rotational reference frame, the harmonics turn into even harmonics, such as the 6th and 10th order harmonics. For the sake of a convenient analysis, only the harmonics mentioned above will be taken into account during the analysis. The PLL linearization model of the input disturbance can be described as follows:



Fig. 8. The unified small-signal model.

$$\tilde{v}_q(s) = L[f(2\omega, 4\omega, 6\omega, 8\omega...)]$$
(30)

where, L denotes the Laplace transformation.

In the synchronous rotational reference frame, the negative sequence component at the fundamental frequency will be the 2^{nd} order harmonic. The five PLL methods analyzed above can thoroughly eliminate the influences of the negative sequence component at the fundamental frequency by a direct decouple module or PNSC module. Therefore, 2^{nd} order harmonic disturbances can be eliminated. However, the consequent problem regarding limitations in the dynamic response provided by the notch filter cannot be ignored. Thus, the bandwidth of the open-loop system must be less than 2ω to achieve good robustness for the PLL.

C. Parameter Design

According to the equivalent analysis above, the relationship between the transfer functions of each PLL method (equations: (10), (13), (17) and (22)) and the equivalent transfer function (23) can be obtained.

For the DDSRF-PLL, $\omega_f = g\omega'/2$. For the DSOGI-PLL/FLL, k = g. For the DIPT-PLL, n = g and $\omega_f' = n\omega' = g\omega'$. For the CCF-PLL, $\omega_c = g\omega'/2$.

The characteristic function $G(s) = s^2 + g\omega' s + \omega'^2$ of the general transfer function is considered. In order to achieve an objective comparison among the five methods, the damping ratio of the characteristic functions are designed to be 0.7 (approximately $\sqrt{2}$). The resonant frequency of the characteristic functions are set to be the fundamental frequency. Thus, g is equal to 1.4 and the resonant frequency ω' is equal to $2\pi \times 50$ rad/s. The selections of k_p and k_i are based on the small-signal analysis reported in [22]. In this paper, the settling time, measured from the starting time to the time in which the system stays within 1% of the steady-state response, is set to 100ms. Therefore, the parameters for the PI control in the RSF-PLL are: $k_p=92$ and $k_i=4225$.

According to the parameters design and the equivalent relationship, the parameters for each of the PLL methods are as follows. For the DDSRF-PLL, the cutoff frequency of the LPF ω_f is 220rad/s. For the DSOGI-PLL/FLL, the gain coefficient *k* is 1.4, and the gain of the error signal Γ is -46. For the DIPT-PLL, the cutoff frequency of the LPF ω_f is 440rad/s. For the CCF-PLL, the constant ω_c is 220rad/s.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results obtained with the

DDSRF-PLL, DSOGI-FLL, DSOGI-PLL, DIPT-PLL and CCF-PLL are compared under the following conditions. Comparisons and analyses of the steady-state and dynamic characteristics are also included in this section.

1. Unbalanced grid: 0.3pu of the negative sequence component at the fundamental frequency is added to ideal grid.

2. Low-order harmonic: 0.05pu of the 5th-order positive sequence harmonic.

3. Voltage drop: the grid voltage amplitude falls to 0.5pu.

4. Frequency jump: The frequency of the grid voltage step changes to 55Hz.

A. Simulation Results:

Simulation I: the test condition is an unbalanced grid at 0 to 0.5s. At 0.5s, a low-order harmonic is added to the unbalanced grid. The performances of the discussed PLLs in Simulation I are shown in Fig.9.

As shown in Fig.9, the DDSRF-PLL and DIPT-PLL perform best under an unbalanced grid in terms of the responses of the grid voltage phase, positive sequence D-component and grid frequency. When the low-order harmonic is added, the responses for all of the PLLs begin to oscillate. The peaks of the oscillation are summarized in Table I.

Simulation II: the test condition is an unbalanced grid at 0 to 0.5s. At 0.5s, a voltage drop is added to the unbalanced grid. The performances of the discussed PLLs in Simulation II are shown in Fig.10.

When the voltage drop is added, the different PLLs perform differently. Based on the simulation results in Fig. 10, the dynamic responses for each of the PLLs are summarized in Table II.

Simulation III: the test condition is an unbalanced grid at 0 to 0.5s. At 0.5s, a frequency jump is added to the unbalanced grid. The performances of the discussed PLLs in Simulation III are shown in Fig.11.

When the frequency jump is added, the different PLLs perform differently. Based on the simulation results in Fig. 11, the dynamic responses for each of the PLLs are summarized in Table III.

B. Experimental Results:

The experimental platform is shown in Fig.12. A standard AC signal source (Type: JW-0301A) is used to generate a distorted and unbalance grid voltage. The PLLs are implemented by a TMS320F28335 DSP board. The performances for each of the PLLs are evaluated by Matlab/Simulink.

Experiments under the conditions of unbalanced voltages, voltage drops and frequency jumps are all tested. The experiments are divided into two parts.

Experiment I: at the beginning, 0.3pu of the negative sequence component at the fundamental frequency is added to an ideal grid. Then, the voltage drops to 80% of the original





(c) Frequency output.

Fig. 9. Waveform of five PLLs in unbalanced grid with low-order harmonic.

TABLEI
SIMULATION RESULT OF FIVE PLLS UNDER UNBALANCED GRID
WITH LOW-ORDER HARMONIC

	DDSR F-PLL	DSOG I -FLL	DSOG I -PLL	DIPT- PLL	CCF- PLL
Phase (rad)	0	0.01	0.01	0	0.01
V _d + (pu)	0.03	0.03	0.04	0.03	0.03
Frequency (Hz)	0.2	0.08	0.07	0.15	0.06



(c) Frequency output.

Fig. 10. Waveform of five PLLs under unbalanced grid and voltage drop.

TABLE II SIMULATION DATA OF FIVE PLLS UNDER UNBALANCED GRID AND VOLTAGE DROP

VOLTAGE DIGI					
	DDSR F-PLL	DSOG I -FLL	DSOG I -PLL	DIPT- PLL	CCF- PLL
Max. Phase error (rad)	0.05	0.08	0.04	0.05	0.04
Overshoot of V _d + (%)	40	0	0	40	0
Max. Frequency error(Hz)	1.7	1.1	0.5	1.7	0.5





(c) Frequency value.

Fig. 11. Waveform of five PLLs in unbalanced grid and frequency jump.

TABLE III
SIMULATION DATA OF FIVE PLLS UNDER UNBALANCED GRID AND
FREOUENCY JUMP

The generation					
	DDSR F-PLL	DSOG I -FLL	DSOG I -PLL	DIPT- PLL	CCF- PLL
Phase error (rad)	0.53	0.35	0.6	0.54	0.6
Ud+ error (V)	0.17	0.05	0.16	0.15	0.16
Frequency Overshoot(%)	30	0	32	32	38



Fig.12. Experimental platform.



Fig. 13. Experimental waveform of five PLLs under voltage drop.

voltage. The responses of the positive sequence D-component are shown in Fig.13.

Experiment II: at the beginning, 0.3pu of the negative sequence component at the fundamental frequency is added to an ideal grid. The grid frequency is set as 50Hz. Then, the frequency jumps to 51Hz. The responses of the frequencies are shown in Fig.14.

Based on the experimental results in Fig.13 and Fig.14, the performances of the discussed PLLs are summarized in Table IV.

From the simulation and experimental results obtained with all five of the PLL methods, the following conclusions can be obtained:

When a negative sequence component at the fundamental frequency exists in the three-phase grid voltage, 2ω oscillations appear in the frequency steady-state waveforms of all five PLLs. This is caused by the negative sequence component. The negative sequence component cannot be totally eliminated.

(2) Under the conditions of an unbalanced grid voltage, voltage drops (sag) and frequency steps (jump), it can be seen from Tables I and Table II that all five of the PLLs can effectively extract phase information in the steady state.

(3) When the grid voltage amplitude experiences sudden drops, the amplitude waveforms in Fig.10 and Fig.13 demonstrate that the DDSRF-PLL and DIPT-PLL have extremely prompt responses in detecting the positive sequence D-component V_d^+ . In LVRT applications, this characteristic



Fig. 14. Experimental waveform of five PLLs under frequency jump.

TABLE IV EXPERIMENTAL RESULTS OF FIVE PLLS UNDER VOLTAGE DROP AND FREQUENCY JUMP

	DDSR F-PLL	DSOG I -FLL	DSOG I -PLL	DIPT- PLL	CCF-P LL
Ud+ error(V)	0.6	0.4	0.1	0.8	0.3
Ud+ overshoot (%)	2.8	0	0	1.8	0
Frequency error(Hz)	0.14	0.03	0.03	0.07	0.07
Frequency overshoot (%)	32	0	42	49	48
Running time in DSP(us)	14.1	11.8	10.4	14.4	9.8

can be used to as feed forward in order to eliminate grid shock currents. However, these two PLL methods are not appropriate for phase angle detection in dynamic situations due to the presence of large oscillations in the phase detection. On the other hand, the DSOGI-PLL and CCF-PLL can achieve good performance in terms of phase detection.

(4) Under the frequency jump condition, the frequency response waveforms in Fig.11 and Fig.14 show that the frequency response of the DSOGI-FLL is smooth and steady with a very small overshoot. In the application of unintentional islanding detection, this characteristic for the DSOGI-FLL is very suitable for avoiding misjudgments.

(5) Because the DSOGI-FLL adopts frequency feedback, it has the feature of frequency adaption. The CCF-PLL is a simple method that is suitable for parallel detection of sub-order harmonics. Both of these PLLs are superior when it comes to the applications of Active Power Filters (APF).

V. CONCLUSIONS

This paper surveys five typical PLL methods. Firstly, the transfer functions for each of the PLLs have been analyzed. Then, a unified small-signal model has been proposed to reveal their interior relations and to design the control parameters.

Finally, Matlab simulations and experiments have been carried out to compare and analyze the steady-state characteristics and dynamic responses for the discussed PLL methods. The merits and drawbacks for each of the method are analyzed. Furthermore, their advantages and applicability in terms of current control, low voltage through ride (LVRT) and unintentional islanding detection are given.

ACKNOWLEDGMENT

This work was supported in part by the Sichuan Science and technology support program (No. 2016GZ0027) and in part by the Fundamental Research Funds for the Central Universities (No. ZYGX2015J075, No. ZYGX2014J069).

APPENDIX

The unbalanced three-phase voltage v_{abc} can be decompose into the sum of the instantaneous positive sequence component, negative sequence component and zero sequence component. The relationships are shown in (31) to (34).

$$v_{abc} = v_{abc}^{+} + v_{abc}^{-} + v_{abc}^{0}$$
(31)

$$v_{abc}^{+} = \begin{bmatrix} T_{+} \end{bmatrix} v_{abc}; \qquad \begin{bmatrix} v_{a}^{+} \\ v_{b}^{+} \\ v_{c}^{+} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^{2} \\ a^{2} & 1 & a \\ a & a^{2} & 1 \end{bmatrix} \begin{bmatrix} v_{a} \\ v_{b} \\ v_{c} \end{bmatrix}$$
(32)

$$v_{abc}^{-} = \begin{bmatrix} T_{-} \end{bmatrix} v_{abc}; \quad \begin{bmatrix} v_{a}^{-} \\ v_{b}^{-} \\ v_{c}^{-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a^{2} & a \\ a & 1 & a^{2} \\ a^{2} & a & 1 \end{bmatrix} \begin{bmatrix} v_{a} \\ v_{b} \\ v_{c} \end{bmatrix}$$
(33)

$$v_{abc}^{0} = \begin{bmatrix} T_{0} \end{bmatrix} v_{abc}; \quad \begin{bmatrix} v_{a}^{0} \\ v_{b}^{0} \\ v_{c}^{0} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_{a} \\ v_{b} \\ v_{c} \end{bmatrix}$$
(34)

where, $a=e^{-i2\pi/3}$ refers to a 120° phase shift.

In a three phase system, the zero sequence components do not exist. Therefore, the positive and negative sequence components can be transformed into the $\alpha\beta$ stationary reference frame as follows:

$$v_{\alpha\beta}^{+} = T_{\alpha\beta} v_{abc}^{+} \tag{35}$$

$$v_{\alpha\beta}^{-} = T_{\alpha\beta} v_{abc}^{-} \tag{36}$$

The following equations can be obtained by applying inverse Clarke transformations:

$$\mathbf{v}_{\alpha\beta}^{+} = \begin{bmatrix} T_{\alpha\beta+} \end{bmatrix} \mathbf{v}_{\alpha\beta}; \begin{bmatrix} T_{\alpha\beta+} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix}$$
(39)

$$v_{\alpha\beta}^{-} = \begin{bmatrix} T_{\alpha\beta} \end{bmatrix} v_{\alpha\beta}; \begin{bmatrix} T_{\alpha\beta} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix}$$
(40)

where, $q=e^{-i\pi/2}$ is the operation of a -90° phase shift.

REFERENCES

- Q. Wang, M. Cheng, and Y. Jiang, "A novel controller of electric springs based on bode diagram optimization," *Journal of Power Electronics*, Vol. 16, No. 4, pp. 1396–1406, Jul. 2016.
- [2] W. Wang, L. Yan, X. Zeng, B. Fan, and J. M. Guerrero, "Principle and design of a single-phase inverter based grounding system for neutral-to-ground voltage compensation in distribution networks," *IEEE Trans. Ind. Electron.*, Vol. PP, No. 99, pp. 1-1, Sep. 2016.
- [3] V. Kaura and V. Blasco, "Operation of a phase locked loop system under distorted utility conditions," in 11th Annual Applied Power Electronics Conference and Exposition (APEC), Mar. 1996.
- [4] K. Young and R. A. Dougal, "SRF-PLL with dynamic center frequency for improved phase detection," in 2009 IEEE International Conference on Clean Electrical Power, pp. 212-216, Jun. 2009.
- [5] U. S. Seong and S. H. Hwang "Analysis of phase error effects due to grid frequency variation of SRF-PLL based on APF," *Journal of Power Electronics*, Vol. 16, No. 1, pp.18-26, Jan. 2016.
- [6] S. K. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Trans Power Electron.*, Vol. 15, No. 3, pp. 431-438, May 2000.
- [7] H. Awad, J. Svensson, and M. J. Bollen, "Tuning software phase-Locked loop for series-connected converters," *IEEE Trans. Power Del.*, Vol. 20, No. 1, pp. 300-308, Jan. 2005.
- [8] B. Sen, D. Sharma, and B. C. Babu, "DSRF and SOGI based PLL-two viable scheme for grid synchronization of DG systems during grid abnormalities," in 2012 Students Conference on Engineering and Systems (SCES), pp.1-6, Mar. 2012.
- [9] S. Gao and M. Barnes, "Phase-locked loop for AC systems: analyses and comparisons," in 6th IET International Conference on Power Electronics, Machines and Drives (PEMD), pp. 1-6, Mar. 2012.
- [10] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, Vol. 22, No. 2, pp. 584-592, Mar. 2007.
- [11] A. Nicastri and A. Nagliero, "Comparison and evaluation of the PLL techniques for the design of the grid-connected inverter systems," in 2010 IEEE International Symposium on Industrial Electronics (ISIE), pp. 3865-3870, Jul. 2010.
- [12] K. Li, A type of three phase lock loop base on reverse park transformer, China patent. 201310179102, 2013.
- [13] Z. Xing and Z. Chongwei, *PWM rectifier and its control*, China Machine PRESS, 2012.
- [14] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1194-1204, Apr. 2011.
- [15] P. Tan, H. He, and X. Gao. "A frequency-tracking method based on SOGI-PLL for wireless power transfer system to assure operation in resonant state," *Journal of Power Electronics*, Vol.16, No.3, pp.1056-1066, May 2016.
- [16] P. Rodriguez, A. Luna, I. Etxeberria, J. R. Hermoso, and R. Teodorescu, "Multiple second order generalized integrators for harmonic synchronization of power converters," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2239-2246, Sep. 2009.

- [17] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multi-resonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 1, pp. 127-138, Jan. 2011.
- [18] P. Rodríguez, A. Luna, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Advanced grid synchronization system for power converters under unbalanced and distorted operating conditions," in 32nd Annual Conference of IEEE Industrial Electronics(IECON), pp. 5173-5178, Nov. 2006.
- [19] P. Rodirguez, A. Luna, I. Candela, R. Teodorescu, and F. Blaabjerg, "Grid synchronization of power converters using multiple second order generalized integrators," in 34th Annual Conference of IEEE Industrial Electronics (IECON), pp.755-760, Nov. 2008.
- [20] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in 37th IEEE Power Electronics Specialists Conference (PESC), pp.1-6, 2006.
- [21] X. Zhao, X. Jin, and F. Zhou, "A frequency-locked loop technology of grid-connected inverters based on the reduced order resonant controller," in *Proceedings of the CSEE*, Vol. 33, No. 15, pp. 38-44, May 2013.
- [22] R. Teodorescu, M. Liserre, and P. Rodriguez, Grid converters for photovoltaic and wind power systems, John Wiley & Sons, 2011.



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