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Model-based Optimal Control Algorithm for the Clamp Switch of Zero-Voltage Switching DC–DC Converter

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Abstract

This paper proposes a model-based optimal control algorithm for the clamp switch of a zero-voltage switching (ZVS) bidirectional DC–DC converter. The bidirectional DC–DC converter (BDC) can accomplish the ZVS operation using the clamp switch. The minimum current for the ZVS operation is maintained, and the inductor current is separated from the input and output voltages by the clamp switch in this topology. The clamp switch can decrease the inductor current ripple, switching loss, and conduction loss of the system. Therefore, the optimal control of the clamp switch is significant to improve the efficiency of the system. This paper proposes a model-based optimal control algorithm using phase shift in a micro-controller unit. The proposed control algorithm is demonstrated by the results of PSIM simulations and an experiment conducted in a 1-kW ZVS BDC system.

Key words: Bidirectional DC–DC converter, Clamp switch, Inductor current ripple, Zero-voltage switching

I. INTRODUCTION

The rapidly increasing economy and the enormous demand for energy have resulted in global energy crisis. Therefore, the demand for renewable energy sources, such as sunlight, wind power, and hydrogen energy, has increased. Power conversion systems (PCSs) and energy storage systems for electric vehicles are used to utilize renewable energy efficiently, along with distributed generation and DC distribution systems. PCSs are necessary when using bidirectional DC–DC converters (BDCs) with high reliability, stability, and efficiency [1]-[3].

BDCs can be categorized into isolated converters [4]-[7] and non-isolated converters [8]-[10]. An advantage of an isolated converter is its electrical isolation. The isolated converter system is protected by separating its input and output stages. An isolated converter is also commonly used in applications requiring a large capacity, whereas a non-isolated converter is used for those requiring a small capacity. Most non-isolated BDCs are based on a boost/buck converter structure. The switching frequency must be increased to minimize the size of a non-isolated BDC. However, increasing the switching frequency results in high switching losses. Numerous soft switching methods that employ resonant networks are extensively used in BDCs to solve the problem of high switching losses.

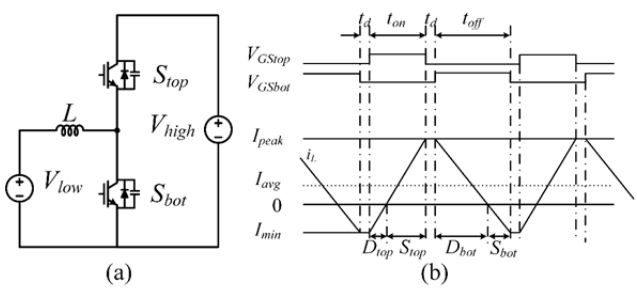

Fig. 1. (a) BDC structure and (b) synchronous conduction mode (SCM) operation.

In general, a conventional BDC is a half-bridge buck-boost converter for a non-isolated converter, as shown in Fig. 1(a). This converter has advantages, such as a simple structure, a simple design method, and an easy control technique. However, the converter also has weaknesses, which include a limited switching frequency and a large switching loss caused by the hard switching of the power semiconductor [11]-[13].

Fig. 1(b) shows the SCM. A BDC that applies SCM is proposed to improve the hard switching of a conventional BDC

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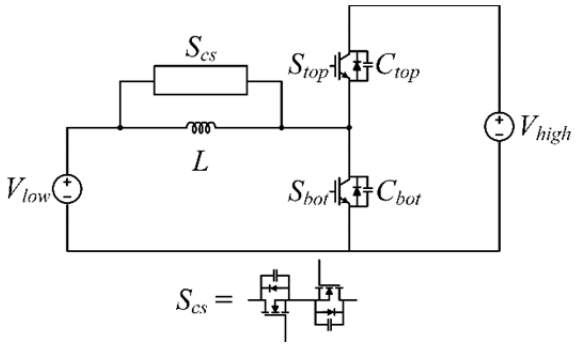


Fig. 2. Zero-voltage switching (ZVS) BDC and clamp switch.

[14]. Performing ZVS with an inductor current obtained from the optimal inductor design without applying additional circuits is possible. When a smaller inductance is used in the conventional converter, the inductor current flows to the low- and high-side directions during each switching period. The negative current can charge and discharge the top and bottom output capacitors of a device to create the resonance. However, a large inductor current ripple causes a large voltage ripple and shortens the lifetime of low-voltage sources, such as batteries and fuel cells.

This paper discusses a ZVS BDC that applies a bidirectional switch (clamp switch). The clamp switch is connected parallel with the inductor of a conventional BDC. The inductor current is separated by the clamp switch from the input and output voltages. Moreover, the clamp switch maintains the minimum inductor current to operate the ZVS operation. Separating the inductor current can decrease the inductor current ripple and power loss of power devices. Therefore, the optimal control of the clamp switch is important to improve system efficiency [15].

A model-based optimal control algorithm for the clamp switch is proposed in this paper. The ZVS BDC discussed in this paper is significant in maintaining a minimum current through the optimal clamp switching for the ZVS operation. Therefore, this paper proposes a model-based optimal control algorithm for the clamp switch using a microcontroller unit (MCU). The proposed algorithm is validated by the results of a PSIM simulation and an experiment.

II. Description of Converter Topology

A. Topology Structure

The ZVS BDC structure with the clamp switch is shown in Fig. 2. Constructing the BDC by connecting the clamp switch to the inductor is possible. The clamp switch comprises two MOSFETS, which perform complementary switching. The inductor is isolated by the clamp switch from the input and output stages. The ZVS BDC achieves the ZVS operation by maintaining the minimum current. Therefore, this topology can reduce the inductor current ripple (I_{ripple}) and the current stress of power devices. However, the clamp switch does not operate ZVS, and the current flowing through the clamp switches is small. MOSFET is applied to the clamp switch to reduce the power loss because it has less switching loss than that of IGBT. Therefore, MOSFET is more suitable for the BDC used in this paper. The ZVS BDC performs a buck and boost operation. The buck operation transfers power from V_{high} to V_{low}, and the boost operation transfers power from V_{low} to V_{high}.

B. Buck Operation

The key waveform of the ZVS BDC during one switching period of the buck operation is shown in Fig. 3. The waveform is divided into seven modes according to the switching state. The switches S_{top}, S_{bot}, and S_{cs} are the main switch, auxiliary switch, and clamp switch, respectively. Fig. 4 shows the equivalent circuits for the ZVS BDC during the buck operation.

1) Mode 1 [t_0–t_1]: Mode 1 is started when the gate signal of S_{top} (V_{GStop}) is turned on. The current flow through inductor V_{high} to V_{low} and the inductor current (I_L) linearly increases. In Mode 1, the ZVS BDC transfers the power from V_{high} to V_{low}. At the end of Mode 1, I_L obtains its maximum value (I_{peak}).

2) Mode 2 [t_1–t_2]: Mode 2 is activated when V_{GStop} is turned off. This mode operates during the dead time between V_{GStop} and the gate signal of S_{bot} (V_{GSbot}), which is a relatively short time. In Mode 2, the energy stored in the inductor charges the parasitic capacitor of S_{top} (C_{top}) and discharges the parasitic capacitor of S_{bot} (C_{bot}). Therefore, the voltage of S_{bot} (V_{Sbot}) reaches zero within the dead time, and S_{bot} can perform the ZVS. After V_{Sbot} reaches zero, I_L flows through the anti-parallel diode of S_{bot}.

3) Mode 3 [t_2–t_3]: Mode 3 is started when V_{GSbot} is turned on. The ZVS operation of S_{bot} is possible, because V_{Sbot} is already at zero in Mode 2. I_L decreases linearly, because the direction of the inductor voltage is opposite to that of I_L. At the end of Mode 3, the direction of I_L changes from positive to negative.

4) Mode 4 [t_3–t_4]: Mode 4 is activated when the direction of I_L changes. I_L flows through S_{bot} and increases (decreases) linearly to negative. V_{GSbot} is turned off when the minimum energy for the ZVS of S_{top} is stored in the inductor. Performing ZVS when the energy of the inductor is larger than the energy of C_{top} and C_{bot} is possible. Equation (1) expresses the relationship between the energies of the inductor and the parasitic capacitor for the ZVS operation.

$$\frac{1}{2}LI_L^2 \geq \frac{1}{2}(C_{top}+C_{bot})V^2 \quad (1)$$

5) Mode 5 [t_4–t_5]: Mode 5 is activated when V_{GSbot} is turned off, and the gate signal of S_{cs} (V_{GScs}) is turned on. The current flows through S_{cs} and the inductor when V_{GScs} is turned on. S_{cs} isolates the inductor from the input and output stages, and power is not transferred to the output in this mode. The ZVS operation of S_{top} can be achieved by maintaining a minimum current of the inductor (I_{min}) because of I_L isolation. Therefore, The turn-on of S_{cs} is important to store the minimum energy in the inductor for

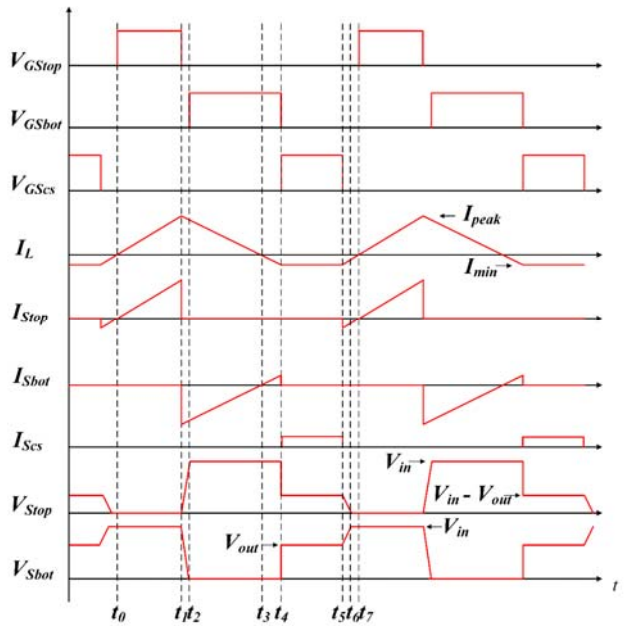


Fig. 3. Key waveform of the buck operation.

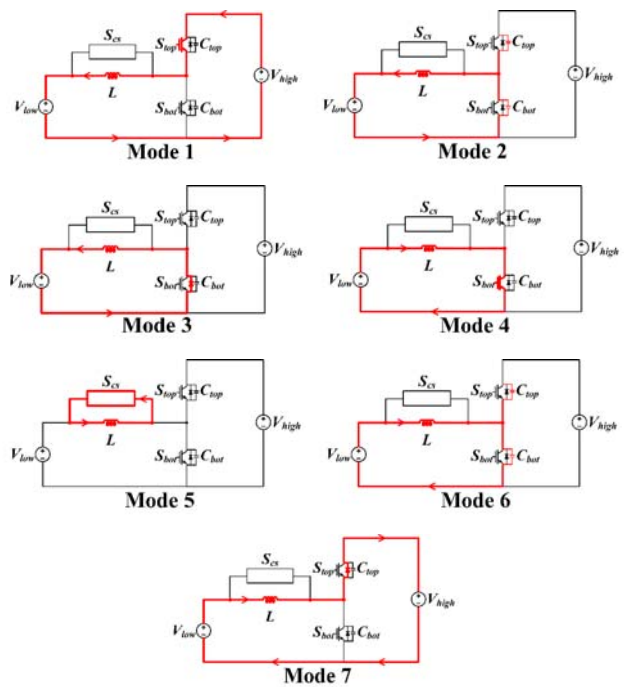


Fig. 4. Equivalent circuits of ZVS BDC during buck operation.

the ZVS of S_{top}.

6) Mode 6 [t_5–t_6]: Mode 6 is started when V_{GScs} is turned off. This mode is operated during the dead time between V_{GScs} and V_{GStop}. The energy stored in the inductor charges C_{bot} and discharges C_{top}. Therefore, V_{Stop} reaches zero before S_{top} is turned on. Thus, performing the ZVS of S_{top} is possible.

7) Mode 7 [t_6–t_7]: Mode 7 is operated when the current flows through the anti-parallel diode of S_{top}. This mode is operated during the dead time between V_{GScs} and V_{GStop}. S_{top} is turned on, and the current flows through S_{top} after Mode 7.

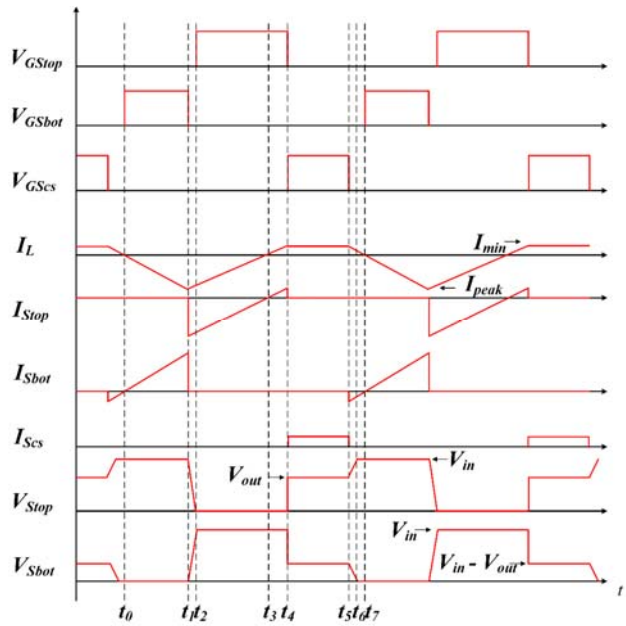


Fig. 5. Key waveform of boost operation.

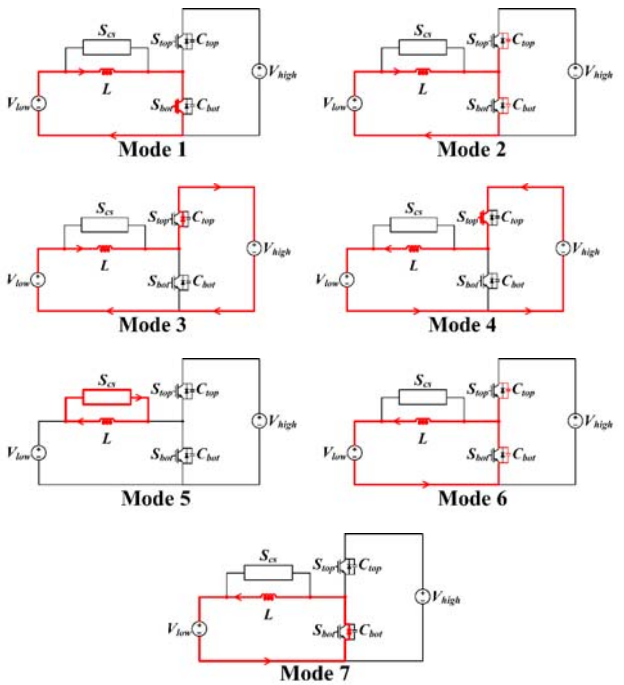


Fig. 6. Equivalent circuits of the ZVS converter in boost mode.

C. Boost Operation

The boost operation can be classified into seven modes similar to the buck operation. However, the switches perform different roles. In the boost operation, S_{bot} and S_{top} are performed as the main switch and auxiliary switch, respectively. The direction of the current is fixed because of an accuracy analysis of the waveform to compare the boost operation with the buck operation. Therefore, I_L has a value of less than zero. Fig. 5 shows the key waveform of the ZVS BDC during one switching period of the boost operation. The

equivalent circuits of the ZVS BDC during the boost operation is shown in Fig. 6.

III. Proposed Model-Based Control Algorithm

S_{cs} is connected parallel with the inductor. When turned on, S_{cs} isolates the inductor from the input and output stages, and maintains I_{min} for the ZVS operation. S_{bot} is turned off and S_{cs} is turned on simultaneously to operate S_{cs}.

The flow of I_L is affected by the timing of the switching operations, as shown in Fig. 7. T_{Stop}, T_{Sbot}, and T_{Scs} are the turn-on times of S_{top}, S_{bot}, and S_{cs}, respectively. D_{Stop}, D_{Sbot}, and D_{Scs} are the duty times of S_{top}, S_{bot}, and S_{cs}, respectively.

In the buck operation, obtaining the average of the inductor current (I_{avg}) is necessary to determine T_{Stop}, because D_{Stop}, which chooses T_{Stop}, is determined by the current control. I_{avg} is controlled, and the output voltage is generated by the current controller. D_{Stop} is determined by the voltage-transfer ratio.

$$D_{Stop} = \frac{V_{out}^*}{V_{in}} \tag{2}$$

The I_L value sensed at the MCU (I_{sen}) is identical to the average inductor current (I_{avg}) in the continuous conduction mode. However, I_{sen} and I_{avg} are different in the discontinuous conduction mode (DCM) during one switching period. Therefore, I_{avg} is calculated in the DCM. Using S_{cs} reveals that I_L has a form similar to the DCM current. Calculating I_{avg} is necessary to control the BDC used in this paper. I_{avg} is determined by calculating the area of I_L. Power is not delivered in T_{Scs}. Therefore, the area of I_L can only be determined by the colored part in Fig. 7. I_{peak} and I_{min} are necessary to calculate the area of I_L. Calculating I_{avg} from D_{Stop} and D_{Sbot} is possible. I_{avg} is expressed as follows:

$$\begin{aligned} I_{avg,k} = & \frac{(I_{peak,k} + |I_{min,k}|)}{2} \cdot (D_{Stop,k} + D_{Sbot,k}) \\ & - |I_{min,k}| \cdot (D_{Stop,k} + D_{Sbot,k}). \end{aligned} \tag{3}$$

$D_{Stop,k+1}$ is decided by Equ. (3) and the reference of I_{avg} (I^*_{avg}). A proportional integral (PI) controller is used to determine $D_{Stop,k+1}$. Fig. 8 shows the block diagram of the PI controller. The transfer function of the inductor current system can be expressed as follows:

$$H(s) = \frac{i(s)}{d(s)} = \frac{V_o}{DLC_o} \cdot \frac{1}{s^2 + \frac{1}{R_L C_o} s + \frac{1}{LC_o}} \tag{4}$$

where L is the inductance of the ZVS BDC, C_o is the output capacitance, and R_L is the load resistor [16]. The transfer function of the PI controller is expressed as follows:

$$K(s) = K_P + K_i / s \tag{5}$$

where K_p is the proportional gain, and K_i is the integral gain of the PI controller. The closed-loop transfer function, which considers the PI controller, is expressed as follows:

$$G(s) = \frac{K(s) \cdot H(s)}{1 + K(s) \cdot H(S)} \tag{6}$$

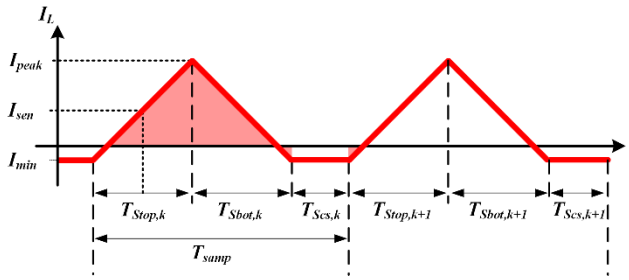


Fig. 7. Inductor current according to switching time.

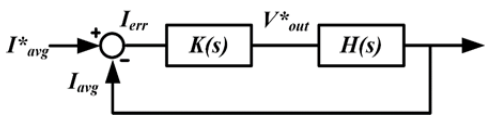


Fig. 8. Block diagram of PI the controller and system.

The bandwidth and gain of the PI current controller are selected by the stability criterion using the transfer function of the closed-loop current controller and Bode plot to stabilize the system.

D_{Stop} can be obtained by substituting V^*_{out} into Equ. (1). Therefore, $T_{Stop,k+1}$ is shown as follows:

$$T_{Stop,k+1} = D_{Stop,k+1} \cdot T_{samp} \tag{7}$$

where T_{samp} is the sampling period.

Solving $T_{Sbot,k+1}$ using the voltage equation of I_L is possible. T_{Sbot} is expressed as follows:

$$T_{Sbot} = (I_{peak} - I_{min}) \frac{L}{V_{out}}. \tag{8}$$

First, obtaining I_{peak} is necessary. I_{peak} can be estimated from I_{sen} and the voltage equation of the inductor. I_{peak} is shown as follows:

$$I_{peak,k+1} = I_{sen,k+1} + \frac{(V_{in} - V_{out})}{L} \frac{1}{2} T_{Stop,k+1}. \tag{9}$$

I_{min} depends on $T_{Sbot,k+1}$, because $T_{Sbot,k+1}$ is the time when I_L changes from I_{peak} to I_{min}. Therefore, based on Equ. (9) and the current variety from I_{peak} to the reference of I_{min} (I^*_{min}), $T_{Sbot,k+1}$ is calculated as follows:

$$T_{Sbot,k+1} = \left(I_{peak,k+1} - I^*_{\min}\right) \frac{L}{V_{out}}. \tag{10}$$

Using Equ. (10), $D_{Sbot,k+1}$ is expressed as follows:

$$D_{Sbot,k+1} = \frac{T_{Sbot,k+1}}{T_{samp}}. \tag{11}$$

Determining D_{Scs} from D_{Stop} and D_{Sbot} is possible. $D_{Scs,k+1}$ is shown as follows:

$$D_{Scs,k+1} = 1 - (D_{Stop,k+1} + D_{Sbot,k+1}). \tag{12}$$

Fig. 9 shows the block diagram of the proposed control algorithm. Each duty is generated by each controller. The generated duty is compared with each pulse width modulation (PWM) carrier to operate switching. The phase shift method is applied to the PWM carrier. Therefore, three PWM carriers are necessary.

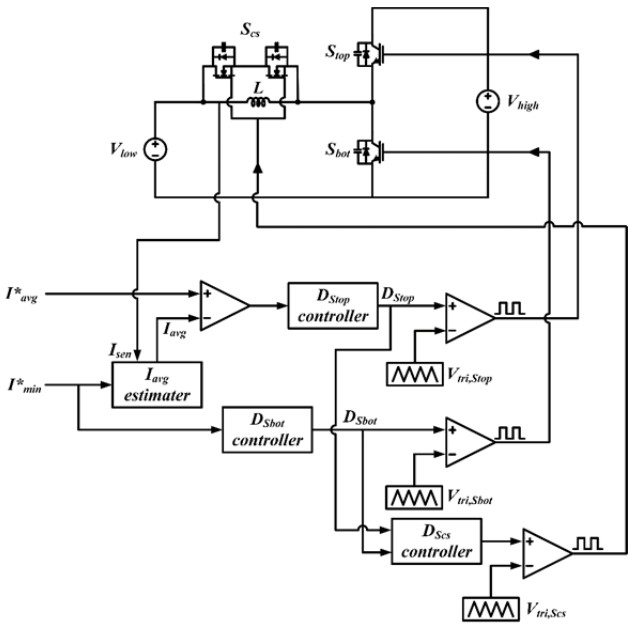


Fig. 9. Block diagram of the proposed control algorithm.

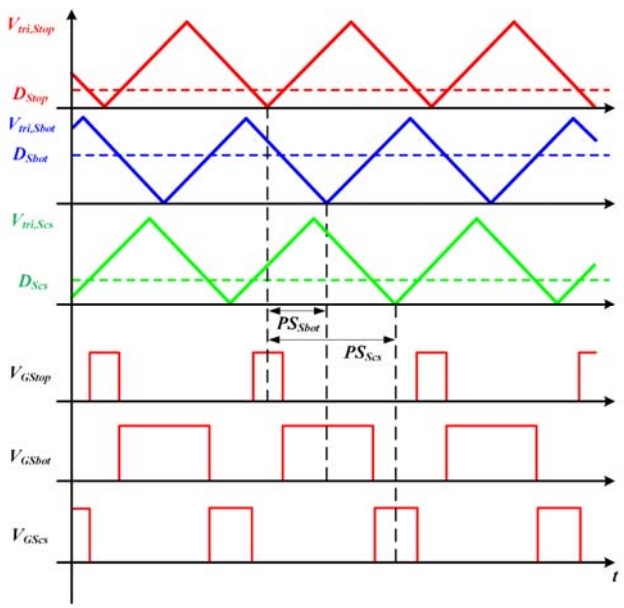


Fig. 10. Phase shift method of ZVS BDC.

In the boost operation, the main switch changes from S_{top} to S_{bot}. Equs. (2), (3), (7), (11), and (12) are similar to those used in the buck operation. However, reorganizing these equations is necessary because Equs. (8)–(10) are different. T_{Stop} is expressed as follows:

$$T_{Stop} = (I_{min} - I_{peak})\frac{L}{(V_{in} - V_{out})}. \quad (13)$$

The denominator is different in Equ. (13), because the voltage of the inductor is $V_{out}-V_{in}$ while the S_{bot} is turned off.

I_{peak} of the boost operation is expressed as follows:

$$I_{peak,k+1} = I_{sen,k+1} - \frac{V_{in}}{2L}T_{Sbot,k+1}. \quad (14)$$

TABLE I
PARAMETERS FOR THE SIMULATION

ZVS BDC	
Rated power	1 kW
High-side voltage	350 V
Low-side voltage	200 V
Switching frequency	10 kHz
Inductance	250 μH
Parasitic capacitance	0.2 nF
Control period	100 μs

I_{min} depends on $T_{Stop,k+1}$, which is determined as follows:

$$T_{Stop,k+1} = \left(I^*_{min} - I_{peak,k+1}\right)\frac{L}{(V_{in} - V_{out})}. \quad (15)$$

The phase shift method of the ZVS BDC is shown in Fig. 10. The switching is not complementary because of the use of S_{cs} in the ZVS BDC. This paper outlines the use of the phase shift algorithm to control S_{cs} optimally. The phase shift algorithm is used for the sequential switching of S_{top}, S_{bot}, and S_{cs}. The phase of $V_{tri,Sbot}$ and $V_{tri,Scs}$ is shifted based on $V_{tri,Stop}$.

The phase of S_{bot} (PS_{Sbot}) is expressed as follows:

$$PS_{Sbot} = \frac{(D_{Stop} + D_{Sbot})}{2} \cdot 360^{\circ}. \quad (16)$$

Similar to Equ. (12), the phase of S_{cs} (PS_{Scs}) is shown as follows:

$$PS_{Scs} = PS_{Sbot} + \frac{(D_{Sbot} + D_{Scs})}{2} \cdot 360^{\circ}. \quad (17)$$

Using Equs. (16) and (17), shifting the phase of the PWM carrier and the sequential switching S_{top}, S_{bot}, and S_{cs} is achievable.

IV. SIMULATION RESULTS

The proposed control algorithm is validated based on the results of PSIM simulation. Table I lists the simulation parameters. The ZVS BDC waveform that applies the proposed algorithm during the buck operation is shown Fig. 11. The phase shift algorithm is used in this study to make the sequential switching of S_{top}, S_{bot}, and S_{cs}. The turn-on time of each switch is acquired using Equs. (7), (10), and (12). The phases of $V_{tri,Sbot}$ and $V_{tri,Scs}$ are shifted based on $V_{tri,Stop}$ for the optimal S_{cs} switching. Therefore, the gate signal is generated sequentially, and the current flows as the DCM.

A. Simulation Results of the Buck Operation

Fig. 12 shows the performance of the proposed optimal control algorithm for the ZVS BDC during the buck operation. I^*_{avg} is 5 A, and I^*_{min} is −1 A. A value of −1 A is selected for I^*_{min} because of the minimum energy required to perform ZVS. Equ. (1) and the parasitic capacitor of the IGBT is used to select I^*_{min}. The parasitic capacitance is obtained using the datasheet of IGBT used in the experiment

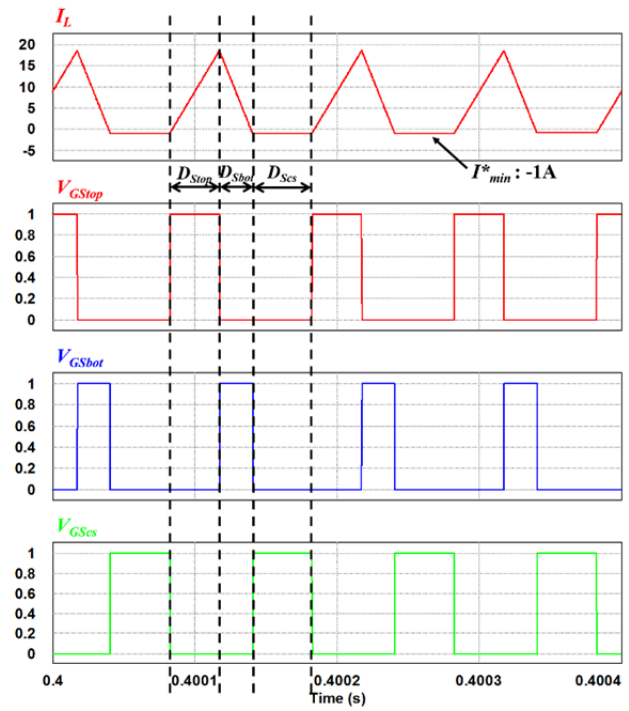
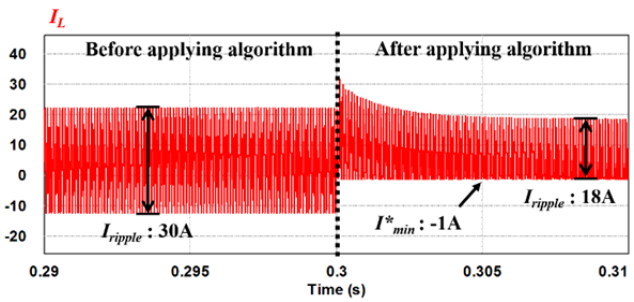
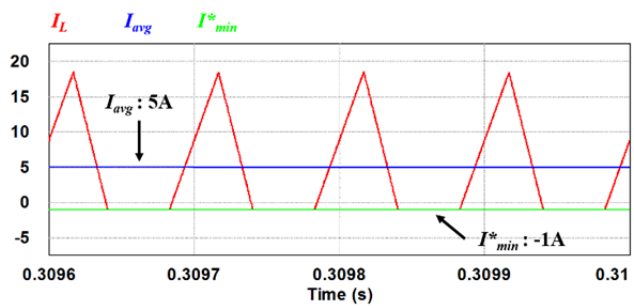


Fig. 11. Inductor current and gate signal of ZVS BDC.



(a) Before and after the inductor current is applied to the algorithm.



(b) Inductor current is applied to the proposed control algorithm.

Fig. 12. Waveform of the proposed control algorithm in buck operation (I^*_{avg}: 5 A, I^*_{min}: −1 A).

set. The equation for selecting I^*_{min} is expressed as follows:

$$I^*_{min} \geq \sqrt{\frac{(C_{top}+C_{bot})\times V^2_{high}}{L}}. \quad (18)$$

When calculating the given value from Equ. (18), I^*_{min} is larger than 0.44 A, which provides a margin. Fig. 12(a) shows I_L with the proposed control algorithm at 0.3 s. I_{min} is

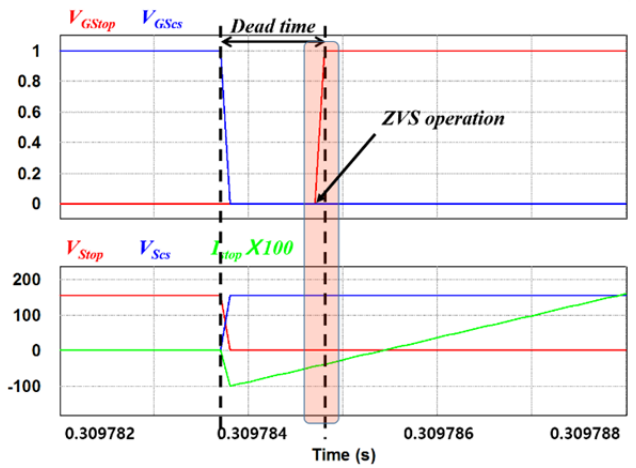


Fig. 13. ZVS of S_{top} within dead time (buck operation).

controlled at −1 A. I_{ripple} is decreased from 30 A to 18 A. The I_L value applied to the proposed control algorithm is shown in Fig. 12(b). I_{avg} is determined by Equ. (3), and I_{avg} is controlled at 5 A in the rated power condition. In the system used in this paper, the low voltage is 200 V, and the rated power is 1 kW. Therefore, 5 A is the rated current. When S_{cs} is turned on, I_{min} is limited to −1 A, which is the I^*_{min} value under this simulation condition.

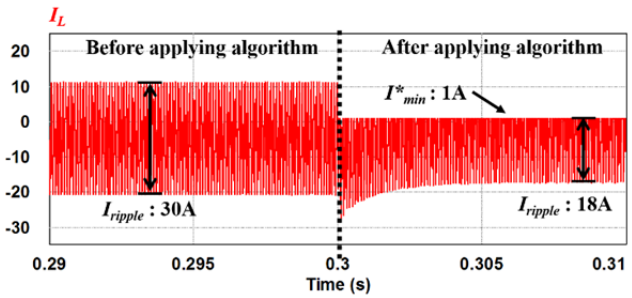
The ZVS of S_{top} within the dead time is shown in Fig. 13. The energy stored in the inductor discharges C_{top} and charges C_{bot}. V_{Stop} reaches zero before V_{GStop}. Therefore, when applying the proposed control algorithm, performing the ZVS from I_{min} is achievable. If the BDC operates under the ZVS condition, then the switching loss of the main switch can be decreased. In addition, I_{ripple} and the conduction loss can be decreased by maintaining I_{min}.

B. Simulation Results of the Boost Operation

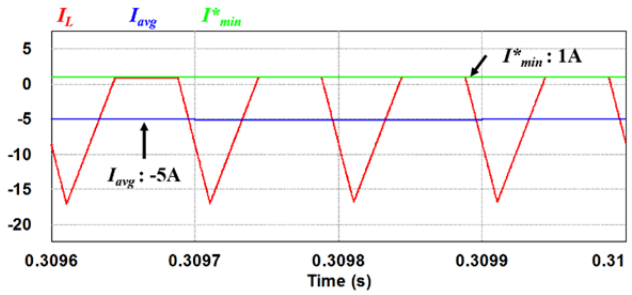
Fig. 14 presents the performance of the proposed optimal control algorithm for the ZVS BDC during the boost operation. The direction of the current is fixed to compare the boost operation with the buck operation. Therefore, I_L flows continuously, and the current flows in the opposite direction compared with that of the buck operation. Fig. 14(a) shows that I_L is controlled by the algorithm at 0.3 s, and I_{min} is controlled at 1 A. Similar to the buck operation, I_{ripple} is reduced. I_{avg} is determined by Equ. (3), and I_{avg} is controlled at −5 A during the rated power condition. A value of −5 A is the rated current under the same condition as Fig. 13. I_{min} is limited to 1 A, as shown in Fig. 14(b). The ZVS of S_{bot} within the dead time is presented in Fig. 15. Although the roles of S_{top} and S_{bot} are changed, the waveform is similar to that of Fig. 13. V_{Sbot} reaches zero using I_{min} before V_{GSbot} is turned on. Therefore, this operation satisfies the ZVS operation.

V. EXPERIMENTAL RESULTS

The experimental parameters are similar with the



(a) Before and after the inductor current is applied to the algorithm.



(b) Inductor current is applied to the proposed control algorithm.

Fig. 14. Waveform of the proposed control algorithm in boost operation (I^*_{avg}: 5 A, I^*_{min}: −1 A).

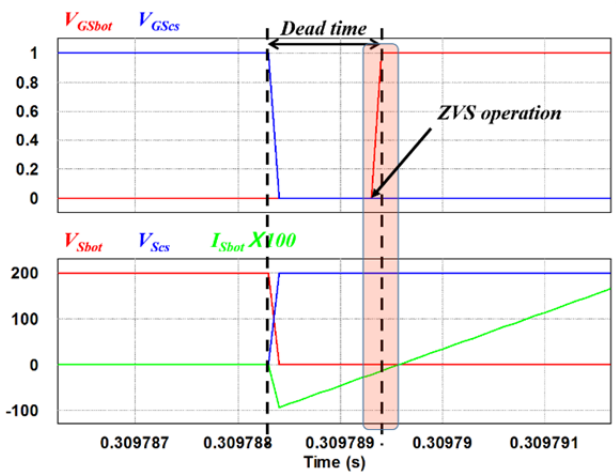


Fig. 15. ZVS of S_{bot} within dead time (boost operation).

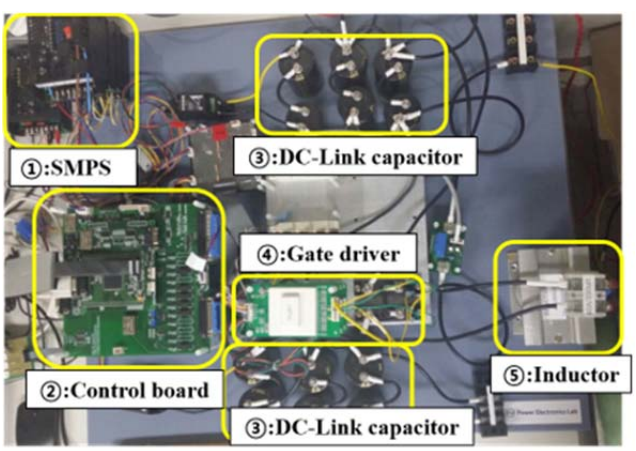
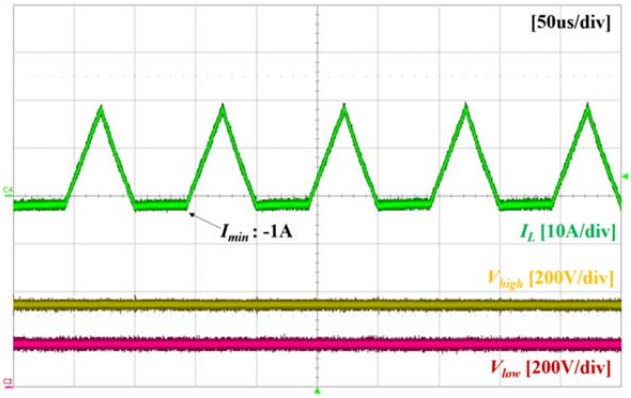
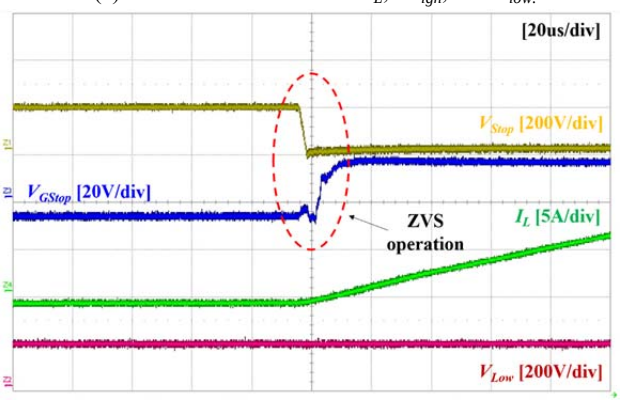


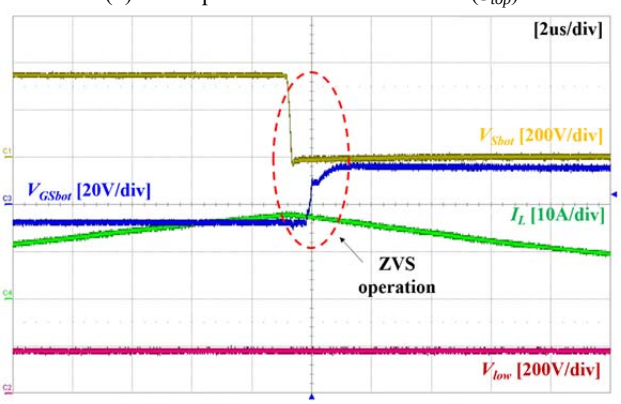
Fig. 16. Experimental configuration of ZVS BDC.



(a) Measured waveforms of I_L, Vh_{igh}, and V_{low}.



(b) ZVS operation of the main switch (S_{top}).



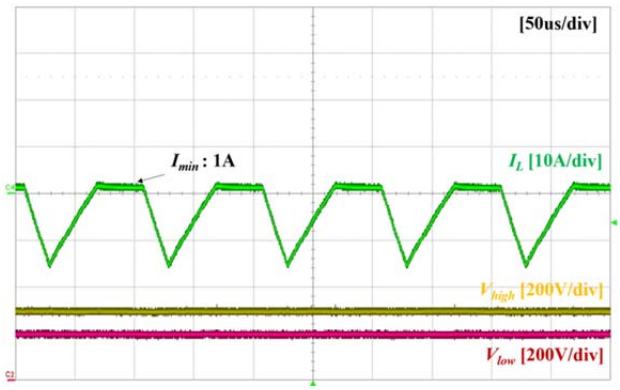
(c) ZVS operation of the auxiliary switch (S_{bot}).

Fig. 17. Experimental results during buck operation.

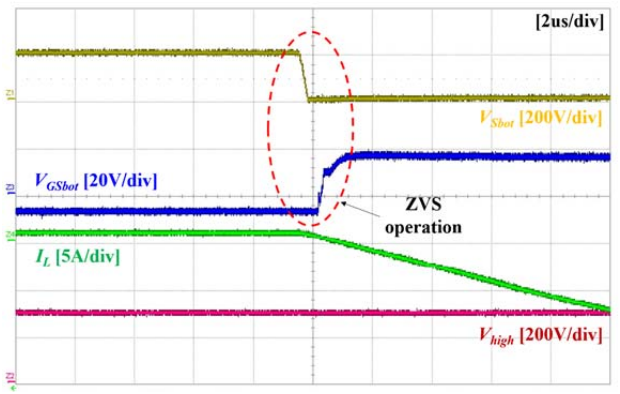
simulation parameters. The ZVS BDC is used for the buck and the boost operations. Fig. 16 shows the experimental setup of the ZVS BDC, which comprises the inductor, SMPS, control board, and DC link capacitors. An SKM75GB063D made by SEMIKRON is used for the main switch, and VMO60-05F made by IXYS is used for the S_{cs}. Each operation is compared using the fixed voltage polarity and current direction based on the buck operation experiment.

Fig. 17 shows the waveforms of the ZVS BDC during the buck operation, and Fig. 18 shows the voltage and current of the ZVS BDC during the boost operation.

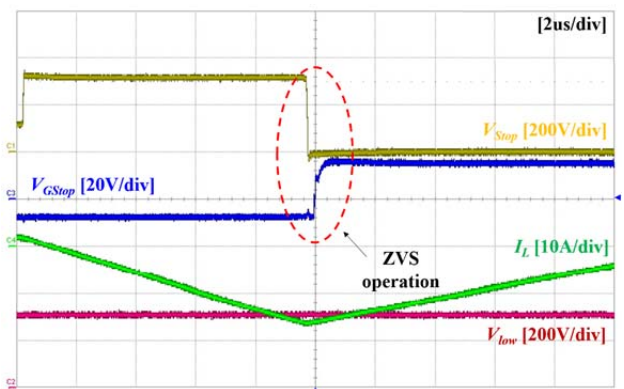
The I_L value used for the proposed control algorithm, which shows the experimental results when V_{high} is 350 V, is shown in Fig. 17(a). I_{min} is maintained at −1 A by S_{cs}. Fig. 17(b) shows



(a) Measured waveforms of I_L, Vh_{igh}, and V_{low}.



(b) ZVS operation of the main switch (S_{bot}).

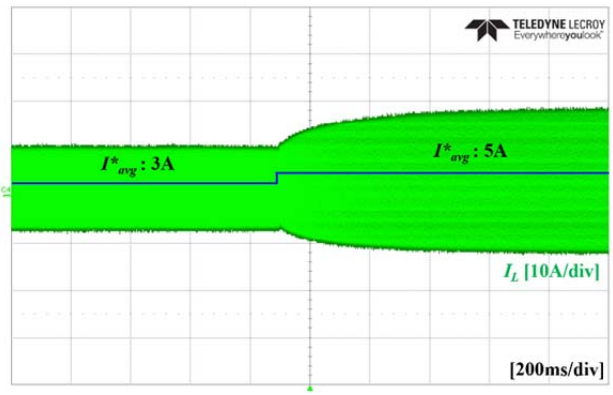


(c) ZVS operation of the auxiliary switch (S_{top}).

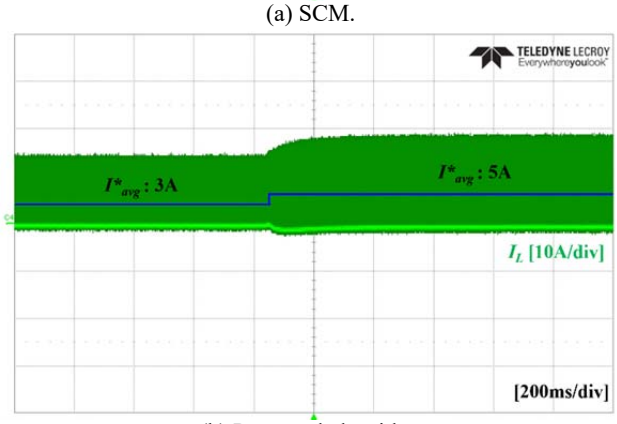
Fig. 18. Experimental results during boost operation.

the ZVS operation of the main switch (S_{top}). Before S_{top} is turned on, V_{Stop} reaches zero, thereby satisfying the ZVS of S_{top}. Fig. 17(c) shows ZVS operation of the auxiliary switch (S_{bot}). S_{bot} is turned on after V_{Sbot} reaches zero. Therefore, all switches operate the ZVS operation.

The waveforms of I_L, V_{high}, and V_{low} during the boost operation are shown in Fig. 18(a). When comparing the buck operation, the current polarity is changed, because I_L is in the opposite direction. Fig 18(b) shows the ZVS operation of the main switch (S_{bot}). Similar to the buck mode, both switches are turned on under the ZVS condition. Although the roles of switches S_{top} and S_{bot} change, the waveform is similar to that shown in Fig. 17(b). The ZVS operation of the auxiliary switch (S_{top}) is shown in Fig. 18(c).

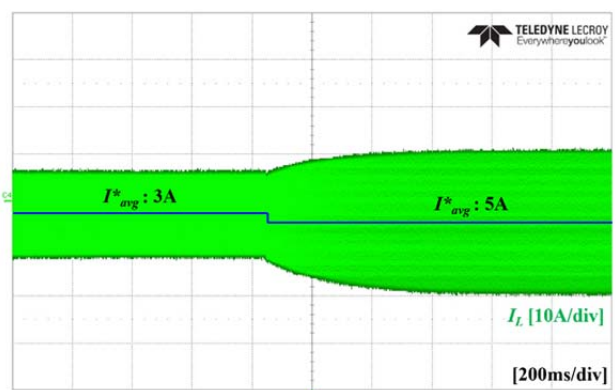


(a) SCM.

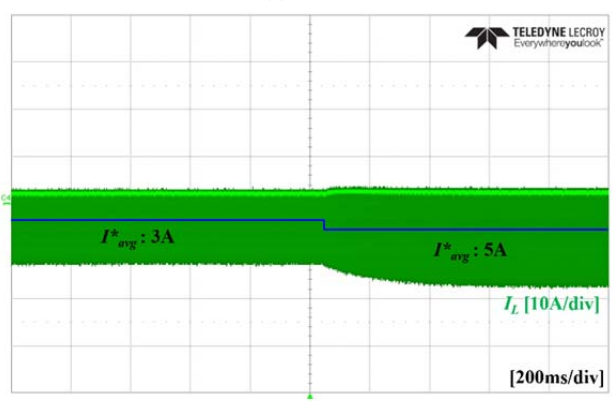


(b) Proposed algorithm

Fig. 19. Dynamic response during buck operation



(a) SCM.

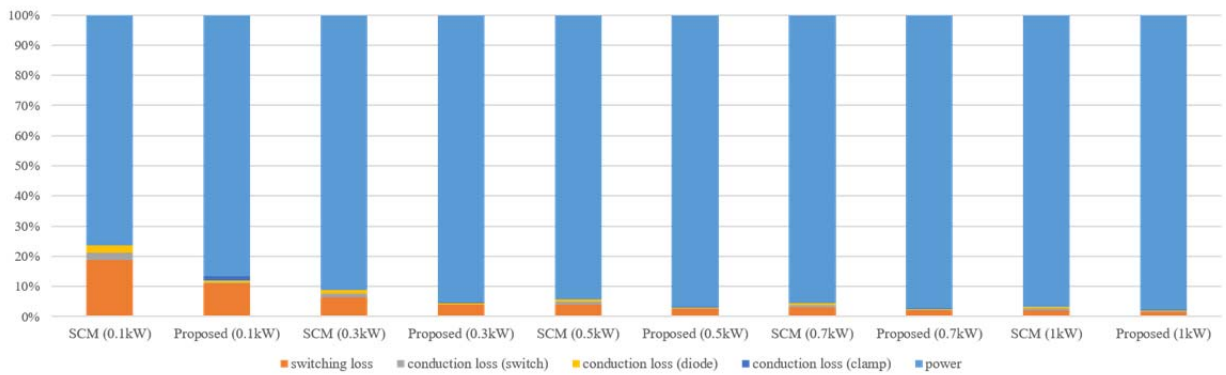


(b) Proposed algorithm.

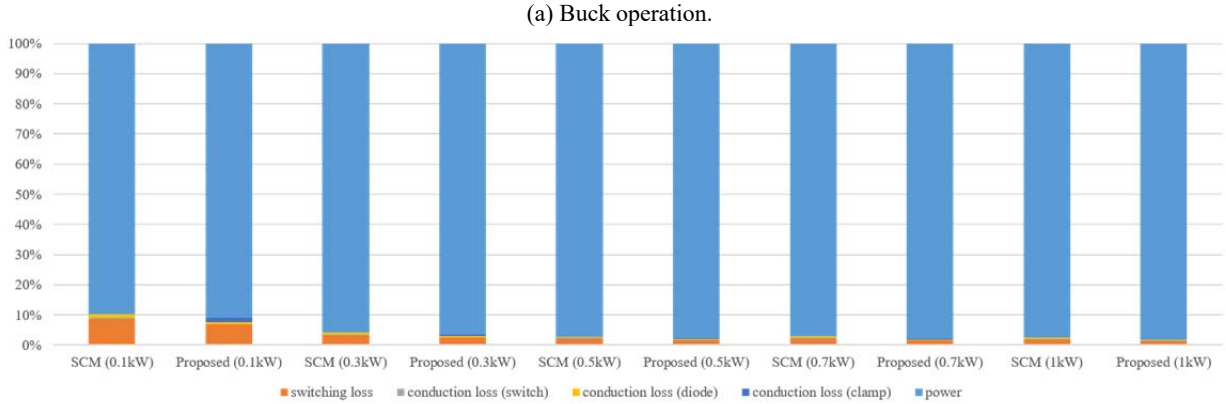
Fig. 20. Dynamic response during boost operation.

TABLE II
LOSS BREAKDOWN OF ZVS METHOD

Mode	P_{out} (W)	Method	Switching Loss (W)	Conduction Loss (switch, W)	Conduction Loss (diode, W)	Conduction Loss (clamp, W)	P_{Loss} (W)	Effi (η)
Buck	100	SCM	30.18	4.18	3.92	0	38.27	61.73
		Proposed	19.82	0.34	1.20	1.33	22.70	77.29
	300	SCM	35.30	6.72	6.32	0	48.33	83.89
		Proposed	22.30	0.90	1.82	1.25	26.26	91.25
	500	SCM	38.16	8.38	7.78	0	54.36	89.13
		Proposed	24.66	1.80	2.50	1.41	30.38	93.92
	700	SCM	40.40	10.66	8.62	0	59.67	91.48
		Proposed	27.98	4.32	3.32	1.47	37.12	94.69
	1000	SCM	40.40	11.78	8.7	0	60.87	93.91
		Proposed	30.08	6.80	4.40	1.59	42.85	95.71
Boost	100	SCM	15.57	1.07	2.08	0	18.72	81.28
		Proposed	12.71	0.22	1.09	1.33	15.35	84.65
	300	SCM	18.53	2.09	3.42	0	24.04	91.98
		Proposed	14.65	0.50	1.73	1.42	18.30	93.89
	500	SCM	20.73	2.84	4.44	0	28.01	94.39
		Proposed	16.14	0.84	2.37	1.42	20.77	95.84
	700	SCM	27.76	5.56	6.78	0	40.09	94.27
		Proposed	20.75	2.02	3.51	1.48	27.77	96.03
	1000	SCM	33.34	7.86	8.65	0	49.85	95.06
		Proposed	25.21	3.89	5.13	1.57	35.81	96.42



(a) Buck operation.



(b) Boost operation.

Fig. 21. Loss breakdown chart.

TABLE III
EFFICIENCY COMPARISON OF ZVS METHOD

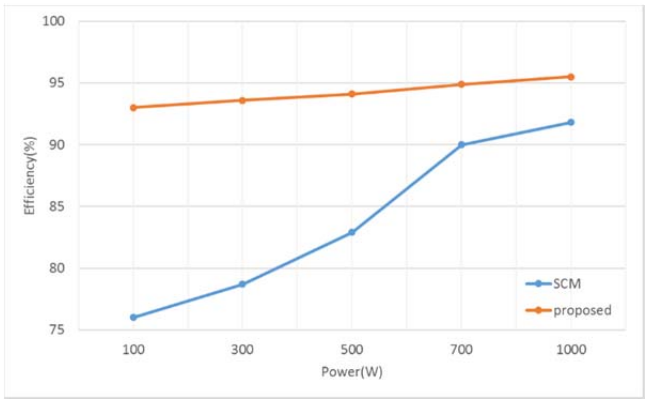
Mode	P_{out} (W)	Method	Effi. (η)
Buck	100	SCM	76.48
		Proposed	85.57
	300	SCM	78.73
		Proposed	93.67
	500	SCM	82.97
		Proposed	94.11
	700	SCM	90.03
		Proposed	94.92
	1000	SCM	91.86
		Proposed	95.55
Boost	100	SCM	75.12
		Proposed	84.20
	300	SCM	81.08
		Proposed	94.30
	500	SCM	86.77
		Proposed	95.18
	700	SCM	90.06
		Proposed	95.31
	1000	SCM	92.65
		Proposed	95.63

The dynamic response in the buck operation is shown in Fig. 19. This experiment progresses in the condition of Figs. 17 and 18. Fig. 19(a) shows that I^*_{avg} is changed from 3 A to 5 A in the SCM. Fig. 19(b) shows that I^*_{avg} is changed to the same reference value in the proposed algorithm; it also shows that I_{min} is maintained even if I^*_{avg} is changed. Compared to SCM and the proposed method, the experimental results of the dynamic response are similar.

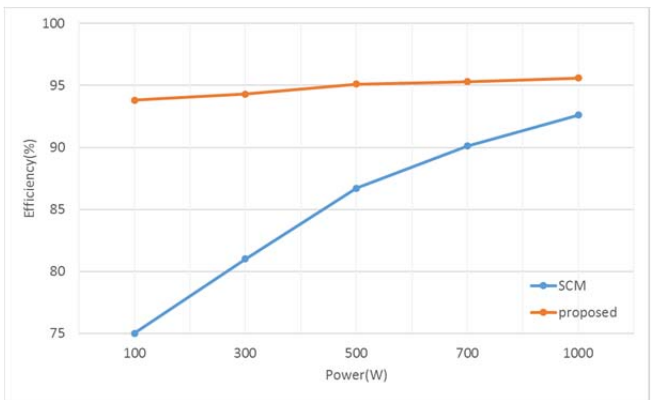
Fig. 20 shows the dynamic response during the boost operation. Fig. 20(a) shows that I^*_{avg} is changed from 3 A to 5 A in the SCM. Fig. 20(b) shows that I^*_{avg} is changed to the same reference value. Similar to the buck operation, if I^*_{avg} is changed, then I_{min} is maintained. SCM and the proposed method do not differ with regard to the dynamic response.

VI. EFFICIENCY COMPARISON

Table II and Fig. 21 show the comparison of loss breakdown between the SCM and the proposed control algorithm. The power loss data is generated and analyzed by the PSIM tool. The proposed method performs a higher efficiency than the results of SCM over the wide-load condition. This result implies that the switching loss can be reduced with the proposed method; two reasons can be considered for this result. First, the conduction loss of the auxiliary switch is decreased, because the clamp switch maintains the minimum inductor current. Current does not flow through the auxiliary switch during on-time of the clamp switch. Therefore, reducing the conduction loss of the auxiliary switch is possible. Second, the turn-off switching loss of the auxiliary switch is reduced, because the magnitude of the current is small at the moment



(a) Buck operation.



(b) Boost operation.

Fig. 22. Experimental efficiency graph

when auxiliary switch is turned off. The power loss is not large even if the switching loss of the clamp switch is generated, because the current is small at the switching, and MOSFET has a low-switching loss characteristic. Particularly the proposed method shows a noticeable benefit in terms of efficiency in the light-load condition, because the I_{ripple} is decreased with the proposed control algorithm. Therefore, the conduction loss and the turn-off switching loss of the auxiliary switch with the proposed control algorithm can also be significantly reduced.

Table III shows the comparison of efficiency between the SCM and the proposed control algorithm through the experiment. The efficiency is measured using a power analyzer WT-3000. Compared with the SCM, the proposed control algorithm has a high efficiency, as shown in Fig. 22. In the buck and boost operations, the maximum efficiency is approximately 95.6%.

VII. CONCLUSION

A model-based optimal control algorithm for the clamp switch of a ZVS BDC was proposed in this paper. ZVS BDC and bidirectional switch were also discussed. In this topology, controlling the clamp switch was significant to maintain the minimum inductor current for the ZVS operation. In addition, the inductor current ripple could be reduced by the clamp

switch. The proposed control algorithm was implemented in the model-based converter and the MCU. The effectiveness of the proposed control algorithm was verified by simulation and experimental results.

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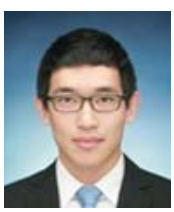

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