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A Fast Sorting Strategy Based on a Two-way Merge Sort for Balancing the Capacitor Voltages in Modular Multilevel Converters

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Abstract

The Modular Multilevel Converter (MMC) is particularly attractive for medium and high power applications such as High-Voltage Direct Current (HVDC) systems. In order to reach a high voltage, the number of cascaded submodules (SMs) is generally very large. Thus, in the applications with hundreds or even thousands of SMs such as MMC-HVDCs, the sorting algorithm of the conventional voltage balancing strategy is extremely slow. This complicates the controller design and increases the hardware cost tremendously. This paper presents a Two-Way Merge Sort (TWMS) strategy based on the prediction of the capacitor voltages under ideal conditions. It also proposes an innovative Insertion Sort Correction for the TWMS (ISC-TWMS) to solve issues in practical engineering under non-ideal conditions. The proposed sorting methods are combined with the features of the MMC-HVDC control strategy, which significantly accelerates the sorting process and reduces the implementation efforts. In comparison with the commonly used quicksort algorithm, it saves at least two-thirds of the sorting execution time in one arm with 100 SMs, and saves more with a higher number of SMs. A 501-level MMC-HVDC simulation model in PSCAD/EMTDC has been built to verify the validity of the proposed strategies. The fast speed and high efficiency of the algorithms are demonstrated by experiments with a DSP controller (TMS320F28335).

Key words: Capacitor voltages balancing, Fast sorting algorithms, Modular multilevel converter, Two-way merge sort

I. INTRODUCTION

In high power High-Voltage Direct Current (HVDC) applications, the power electronics components are constrained and difficult to use due to limitations on the rated voltage. Consequently, with the capability of reaching high voltages, the Modular Multilevel Converter [1] (MMC) has been developed as one of the most attractive topologies in the application of Voltage-Sourced Converter (VSC) based HVDC transmission technology [2]-[4]. The basic structure of the MMC is shown in Fig. 1, where every arm contains N series-connected submodules (SMs) and an inductor L. In this way, the direct series connection of power electronics devices can be avoided, and the devices in one arm do not need to be switched on or off at the same time [5]. Compared with other multilevel topologies, the MMC is able to construct high voltage levels by cascading SMs, with the added advantages of scalability, modularity, high efficiency, better harmonic performance and lower switching frequency [6], [7].

One of the main problems associated with the MMC is its capacitor voltage imbalance among the SMs. According to the existing research on voltage balancing strategies, two distinct groups of methods can be obtained. The first group [8] uses an individual closed-loop controller for each of the SMs to balance the capacitor voltages, which are modulated by the Phase-Shifted Carrier PWM (PSC-PWM) scheme. The second group [2] is based on a sorting algorithm for capacitor voltage balancing. With the help of a closed-loop controller for each of the SMs, the capacitor voltages can be well balanced through PSC-PWM modulation [9]. In [10], a voltages balancing strategy using a PSC-PWM scheme that reduces the number of current sensors is proposed. A predictive PWM strategy based on predefined cost functions shows promising performance in terms of voltages balancing [11]. However, in applications with

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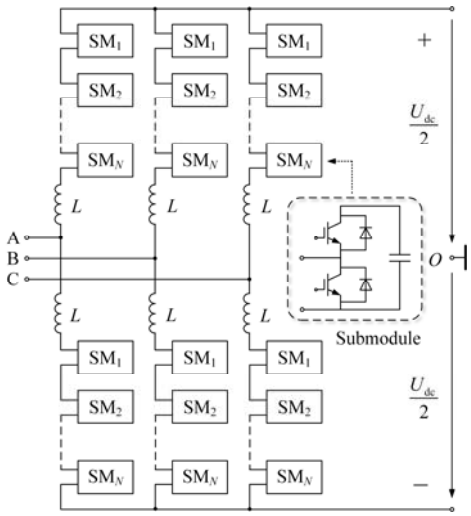


Fig. 1. MMC basic structure.

a very large number of SMs such as HVDC, it is impractical and difficult to use an individual voltage balancing controller for each of the SMs. In this situation, Nearest Level Control (NLC) modulation is a better choice [12]. The most widely applied voltage balancing method is based on the sorting algorithm [13]. With measurements of the direction of the arm current and all of the capacitor voltages, the SMs that have the highest or lowest capacitor voltages are inserted [14]. Thus, a sorting algorithm is required, and it should be executed in every control period. However, when the number of SMs in a HVDC transmission system is very large, the sorting process causes serious implementation issues. It often costs too much time and leaves very little time in a control period for other programs.

As a result, the choice between different sorting algorithms is significant for computational issues. In applications with several SMs, bubble sort, selection sort and odd-even sort are popular choices due to their simplicity. However, they add an enormous computational burden due to their inefficient time complexity $O(N^2)$ on an array of N numbers. To be specific, the O-notation gives an asymptotic upper bound on a function within a constant factor. Hence, it is very common to use the O-notation to describe the running time of an algorithm merely by inspecting the algorithm's overall structure [15]. Obviously, $O(N^2)$ grows rapidly with N numbers. As a result, the sorting method takes too much time, with little left over for other control algorithms, sampling, and so on. Therefore, applications with a large number of SMs such as HVDCs should avoid using them to save implementation efforts. Typically, quicksort is the best practical choice for sorting due to its low expected time complexity $O(N \lg N)$ (use $\lg N$ as $\log_2 N$) and the small constant factors hidden in the $O(N \lg N)$ notation on an input array of N numbers [15]. In comparison with sorting algorithms where the time complexity is $O(N^2)$, such as bubble sort, quicksort is much faster. This makes it a better candidate for sorting in HVDCs. However, when the number of SMs is extremely large, even quicksort is not fast enough to finish sorting in one control period. As a result, more expensive controllers with a higher CPU rate have to be applied. In the practical application of a MMC-HVDC, several advanced FPGA controllers commonly work together to achieve the sorting process. If one normal controller with a faster sorting algorithm can solve it, the hardware cost will decrease, and it will have better stability and simplicity in terms of the control structure.

Combined with the conventional sorting method, many improved capacitor voltage balancing strategies have been proposed [16]-[18]. However, these strategies mainly focused on reducing the switching frequency, and the computational issue is not effectively improved when the number of SMs is very large. Hence, on the basis of the hardware logic design, "The Tortoise and the Hare" sorting algorithm was introduced in [19] to reduce the computational weight. However, its application is limited in terms of its dependence on the hardware structure, and it is not convenient to use when specific values of the capacitor voltages have to be considered. In order to accelerate the MMC simulation process, an efficient sorting algorithm based on a Thévenin's equivalent circuit is proposed in [20]. However, the conclusions demonstrate that this method can only be applied in specific simulations. An optimized FPGA implementation for balancing capacitor voltages has been presented in [21], and it accelerates the sorting process. However, since it has to detect and operate every time the number of required inserted SMs changes, the sampling and controlling systems should be designed with a very high speed. This has the effect of greatly increasing the hardware cost and lowering the stability of MMC systems with a large number of SMs.

This paper presents a new sorting strategy based on Two-Way Merge Sort (TWMS) [22] for balancing capacitor voltages, combined with a capacitor voltage prediction strategy under ideal conditions. This method dramatically accelerates the sorting process and greatly reduces the computational load. In addition, to deal with the non-ideal conditions in practical engineering, an innovative Insertion Sort Correction (ISC) algorithm for the TWMS (ISC-TWMS) is proposed in this paper. This algorithm features a high efficiency and a low computational burden. More importantly, it can be used in real applications, with a much higher speed and efficiency than commonly used sorting algorithms such as quicksort. A 501-level MMC simulations in PSCAD/EMTDC has been built to verify the studies, and experiments are carried out using a DSP controller (TMS320F28335) to measure the practical sorting execution time.

This paper is organized as follows. Section II presents the basic principles of TWMS and proposes a sorting strategy combined with the prediction of capacitor voltages under ideal conditions. Under non-ideal conditions, section III analyzes capacitor voltage variations and proposes an ISC-TWMS

strategy. Simulation and experimental results are presented in Section IV. Finally, some conclusions are drawn in Section V.

II. Proposed TWMS Strategy under Ideal Conditions

A. Basic Principles of TWMS

The core idea of TWMS is to combine two previously ordered arrays into a single ordered array [23]. To be specific, compare the two smallest items in two ordered arrays, output the smallest, repeat the same process until one of the arrays is finished, copy the rest of the items of the other array and finally get one set of ordered results. Assuming the subarrays $A[p..q]$ and $A[q+1..r]$ are in ascending order, to merge them into an ordered array $z[p]\leq z[p+1]\leq\cdots\leq z[r]$, Fig. 2(a) shows flowcharts of the TWMS of the pointers in ascending order.

To be specific, set i, j and k to be the pointers of the two unsorted subarrays and the ordered array z. Then compare A[i] (in the first subarray) and $A[j]$ (in the second subarray). If $A[i]\leq A[j]$, copy $A[i]$ into $z[k]$, and add 1 to the pointers i and k to compare the subarrays next number; if not, copy $A[j]$ into $z[k]$, and add 1 to the pointers j and k. Repeat the loop until one of the subarrays has been completely copied into $z[k]$ ($i>q$ or $j>r$). Then sequentially copy the remaining numbers into the rest of the subarray, and get the two-way merged ordered array z. It should be mentioned that the pointers i, j and k ascend from the beginning of the arrays in Fig. 2(a). Another method where the pointers i, j and k are in descending order is shown in Fig. 2(b).

Clearly, the flowcharts of the TWMS show that the sorting can be finished within one loop and that the computational efforts are directly proportional to the total number of the unsorted array. As a result, the time complexity of the merge process is $O(N)$ in an array of N numbers [23], because it is compared within N steps. Obviously, $O(N)$ is much smaller than $O(N \lg N)$ of quicksort. However, the two subarrays of the TWMS should already be ordered. Otherwise, the merged array using TWMS is not completely ordered. Typically, despite its high efficiency, the TWMS cannot be directly used in practice due to its strong requirement of ordered subarrays.

Examples of the TWMS of pointers in ascending order and descending order are shown in Fig. 3. Two arrays {8, 9, 12} and {7, 10} are sorted and merged by TWMS in ascending order (from left to right) in Fig. 3(a) and by TWMS in descending order (from right to left) in Fig. 3(b). Clearly, with an input of 5 unsorted numbers, as shown in Fig. 3, the TWMS can finish sorting within one loop of 5 steps.

B. Prediction of Capacitor Voltages with Ideal Parameters in One Control Period

Under ideal conditions, the parameters for all of the SMs are identical. In addition, since the "*OFF*" state resistances of the switches in the SMs are very large, it is assumed that they are infinite and that the corresponding branches are completely

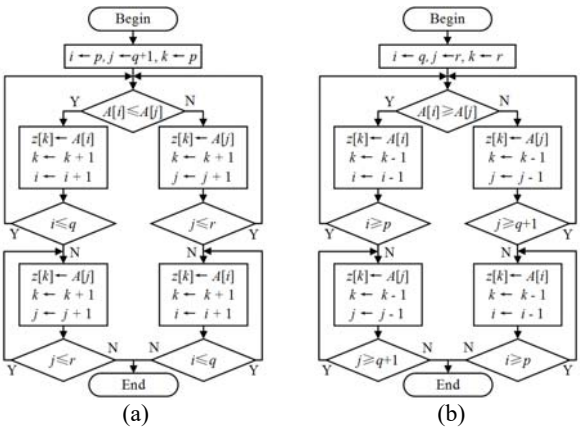


Fig. 2. Flowcharts of TWMS of pointers in (a) ascending and (b) descending order.

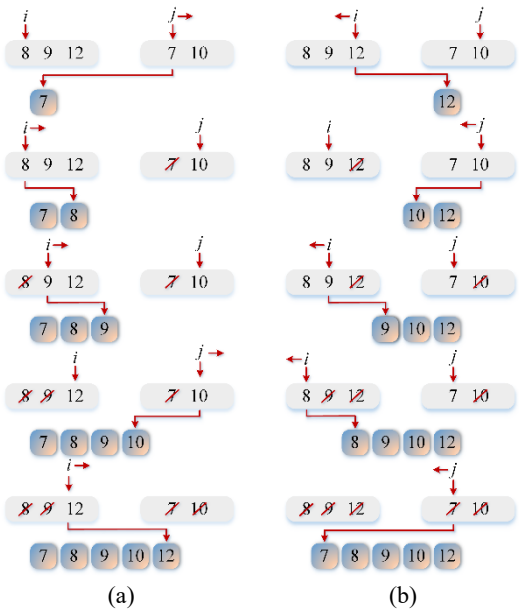


Fig. 3. Examples of TWMS of pointers in (a) ascending and (b) descending order.

open (the leakage current is zero). Hence, the capacitors for all of the inserted SMs in the same arm are directly series-connected. Suppose that the capacitances for all of the SMs are the nominal value C_0. Then when a control period T_s ends, the voltage of the *ith* inserted SM v_i can be obtained by:

$$v_i = v_{i0} + \frac{1}{C_0}\int_{T_s} i_{arm}dt = v_{i0} + \Delta v \tag{1}$$

where v_{i0} denotes the voltage of the *ith* inserted SM when the control period begins, and i_{arm} represents the arm current, which leads to a capacitor voltage variation Δv. Similarly, the voltage of the *jth* inserted SM v_j in the same arm can be expressed as:

$$v_j = v_{j0} + \frac{1}{C_0}\int_{T_s} i_{arm}dt = v_{j0} + \Delta v \tag{2}$$

Equations (1) and (2) show that the voltage variations Δv for different inserted SMs in the same arm are equal in one control

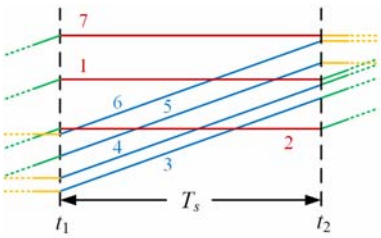


Fig. 4. Capacitor voltage variations of 7 SMs in a control period.

cycle, since the capacitances are equal. As a result, if the SMs are not bypassed, the orders of the capacitor voltages do not change. Therefore, once the order of the capacitor voltages in the last control cycle are recorded, their orders in this control cycle are predicable. As for the capacitor voltages of the bypassed SMs, their voltage variations are obviously the same. As a result, their orders can also be predicted.

An example showing the capacitor voltages variations of 7 SMs in a control period is depicted in Fig. 4, where 3 SMs are bypassed (depicted in red), and the others are inserted (depicted in blue). Obviously, the orders of the inserted (blue lines) and bypassed (red lines) SMs remain unchanged, demonstrating the prediction of the capacitor voltages.

C. TWMS Combined with the Prediction of Capacitor Voltages

In order to use TWMS, the two subarrays should be in order. Considering the predictions of the capacitor voltages, the respectively ordered inserted and bypassed SMs are exactly suitable for the two subarrays, since the orders of the inserted and bypassed SMs can be predicted according to the sorted results in the last control period.

Fig. 5 shows a block diagram of the TWMS strategy combined with the prediction of capacitor voltages. To be specific, according to the records of the sorting results, the number of inserted SMs and the directions of the arm currents in the last control period, divide the SMs into two groups - the inserted group and the bypassed group (the two groups are ordered). Then use TWMS to merge the two groups into one ordered group. Finally, record the results for the next period. When the record of the arm current charges the capacitors, the TWMS of the pointers in ascending order, shown in Fig. 2(a), is used. When the record of the arm current discharges the capacitors, the TWMS of the pointers in the descending order, shown in Fig. 2(b), is used. In this way, the voltages balancing effect will be improved under non-ideal conditions. Detailed proof will be given in Section IV.

Combined with the proposed TWMS strategy, the control scheme of a MMC is shown in Fig. 6. The traditional widely used current vector control based on *dq* coordinates can be adopted in a MMC [18], and v_{j_ref} (j=1, 2, 3 for the three phases) is the output of the control. The Nearest Level Modulation (NLM) is applied because NLM is more practical and suitable than Phase-Shifted Carrier PWM (PSC-PWM) when the number of SMs is very large in a MMC-HVDC

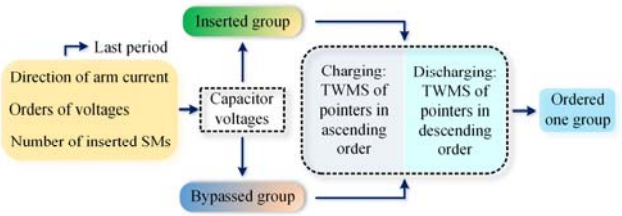


Fig. 5. Block diagram of the TWMS strategy with the prediction of capacitor voltages.

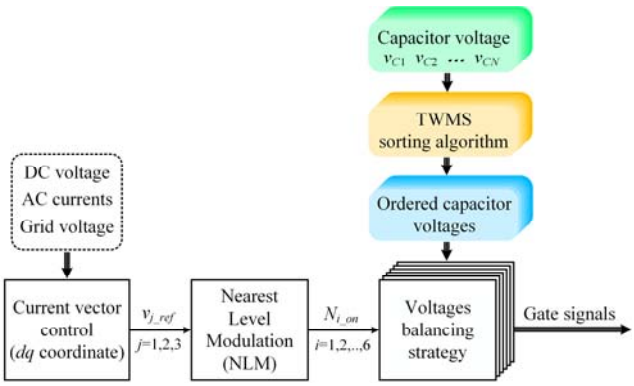


Fig. 6. Block diagram of the control scheme of MMC.

[12]. After the NLM, the number of SMs that should be switched on N_{i_on} (i=1,2,..,6 for six arms) is obtained.

The proposed TWMS sorting method is included in the conventional voltages balancing strategy [2][14]. Depending on N_{i_on}, the traditional strategy balances the capacitor voltages as follows. If the arm current charges the capacitors, the SMs with the lowest capacitor voltages are switched on, and the voltages of the involved charged capacitors increase and conform to the other capacitor voltages. If the arm current discharges the capacitors, the SMs with the highest capacitor voltages are switched on, and the triggered capacitor voltages decrease to conform to the lower ones. As a result, by using the proposed efficient TWMS sorting method in the voltages balancing strategy, the n highest or lowest capacitor voltages can be immediately obtained from the results. This is much faster than traditional sorting algorithms, where n represents the number of SMs that should be inserted in a control period.

III. Proposed ISC-TWMS Strategy under Non-Ideal Conditions

A. Prediction of Capacitor Voltages Analysis under Non-Ideal Conditions

Under non-ideal conditions, there is no guarantee that all of the storage capacitances of SMs are exactly equal to the nominal value. As a result, differences between the storage capacitances cause different voltage variations Δv in (1) and (2). When the voltages of the inserted SMs are close to each other, the orders of the voltages may change in one control period, and the subarrays for the TWMS are no longer strictly ordered.

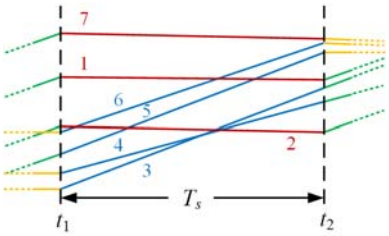


Fig. 7. Capacitor voltages variations of 7 SMs with non-ideal.

Similarly, the losses and different discharge resistances in the bypassed SMs may also cause disorder. However, the chances are a lot less than with the inserted SMs, because the voltage variations of the bypassed SMs are comparatively smaller.

An example showing the capacitor voltage variations of 7 SMs under non-ideal conditions is depicted in Fig. 7. Due to the differences in the storage capacitances, the capacitor voltages of the inserted SMs (depicted in blue) are no longer parallel. Thus, SM3 and SM4 exchange their orders in the control cycle. Therefore, the inserted and bypassed SMs are not ordered under non-ideal conditions. In fact, the TWMS is based on the two subarrays being ordered. However, it is unable to correct disorder within the two subarrays, even if there are not many exchanged orders in a control period. Moreover, the exchanged orders gradually accumulate with the number of control periods, and a correction method should be considered to solve this problems.

In addition to the capacitance error, the "*ON*" and "*OFF*" state resistances of switches are also contributing factors of exchanged orders. However, the capacitance difference has a more significant impact on prediction. Therefore, to analyze the primary non-ideal factor that results in exchanged orders, the *ith* inserted SM in the *N* SMs of the upper arm (or the lower arm) of phase $u = a, b, c$ satisfies the following:

$$\Delta v_i = v_i - v_{i0} = \frac{1}{C_i}\int_{T_s} i_{armu}\,dt \tag{3}$$

where Δv_i is the voltage variation of the *ith* inserted SM in a control period, i_{armu} is the arm current of the upper arm (or the lower arm) of phase $u = a, b, c$, and C_i is the capacitance of the *ith* inserted SM, which can be expressed as:

$$C_i = (1+\varepsilon_i)C_0 \tag{4}$$

where C_0 is the nominal capacitance, and ε_i is ratio of the manufacturing tolerance of the capacitance. Similarly, the *jth* inserted SM also satisfies the corresponding equations (3) and (4) with the subscript *j*. As a result, the difference Δv_{ij} between the voltage variation of the *ith* inserted SM Δv_i and the *jth* inserted SM Δv_j can be obtained by:

$$\begin{aligned}\Delta v_{ij} &= \Delta v_i - \Delta v_j = \left(\frac{1}{C_i} - \frac{1}{C_j}\right)\int_{T_s} i_{armu}\,dt \\ &= \left[\frac{1}{(1+\varepsilon_i)C_0} - \frac{1}{(1+\varepsilon_j)C_0}\right]\int_{T_s} i_{armu}\,dt\end{aligned} \tag{5}$$

When v_i and v_j exchange their orders in a control period, the following relation must be satisfied:

$$\left|v_i - v_j\right| < \left|\Delta v_{ij}\right| \tag{6}$$

Obviously, the possibility of exchanging orders increases with the absolute value of Δv_{ij}. According to equation (5), when the sign of i_{armu} remains unchanged in a control period, the larger T_s is, the larger $|\Delta v_{ij}|$ becomes. Therefore, a longer control period generally leads to a higher possibility of exchanging orders. In addition, a greater difference between ε_i and ε_j also increases $|\Delta v_{ij}|$. This in turn increases the possibility of exchanging orders.

In conclusion, the existence of exchanged orders of the capacitor voltages under non-ideal conditions turns subarrays into disorder. As a result, and the sorted results of the TWMS are not completely ordered. The possibility of exchanging orders increases with the number of control periods and the differences of the capacitances.

B. Voltage Balancing Analysis of the TWMS Strategy under Non-Ideal Conditions

The basis of the TWMS is that the two subarrays are ordered. Even when there are only a few exchanged orders before the accumulation in a control period, the TWMS is unable to correct the disorder in the subarrays. Thus, exchanged orders gradually accumulate over control periods.

However, if the TWMS strategy can balance capacitor voltages under an allowed tolerance under non-ideal conditions, it is still worthy of high speed. In fact, an array of complete ordered voltages does not represent an optimal selection since the switching frequency is unnecessarily high [18]. A voltage balancing analysis of the TWMS strategy under non-ideal conditions is shown in Fig. 8. Suppose the number of SMs per arm is *N* and that *s* SMs are inserted. The sequence $A_1 .. A_s .. A_N$ represent *N* capacitor voltages, and they are sorted in ascending order during the last control period by the TWMS strategy.

Fig. 8(a) shows an analysis of charging capacitors. In the inserted group, assume that A_p represents the capacitor voltage which moves from A_{pi} to the left due to the exchanged orders. When the arm current is positive, the SMs with the highest capacitor voltages (to the right in an ascending sequence) should be bypassed. Therefore, if A_p still moves to the left after the TWMS strategy, it increases the possibility of a mistaken triggering, and should move to the right. According to the flowchart of TWMS in Fig. 2(a), after sorting, the new position of A_p is located at $A'_{p'}$. Clearly, $p \le p'$, which means that A_p is kept still or moves to the right, since at least p-1 of the capacitor voltages in the inserted group are on the left of A_p in the merged array. When the arm current charges the capacitor, the controller chooses the s' SMs with the lowest capacitor voltages. Thus, A_p moves to the right (generally $s'-s \le p'-p$) indicating the decreased possibility of a mistaken triggering. If A_p is not bypassed, the possibility of a mistaken triggering continuously decreases in

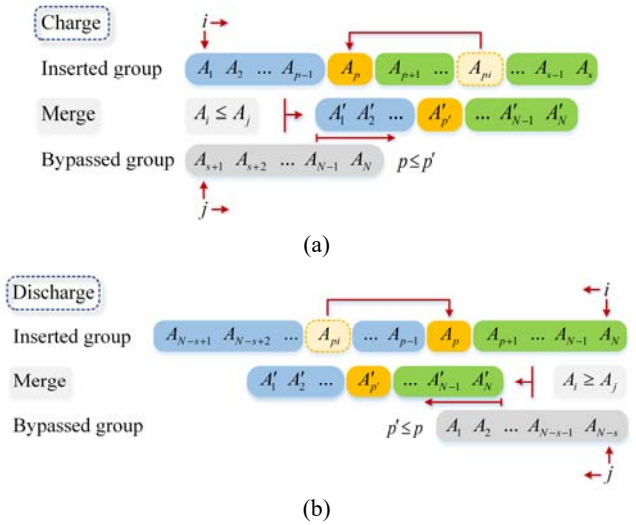


Fig. 8. Voltage balancing analysis of the proposed TWMS strategy in non-ideal conditions (a) of charging and (b) discharging capacitors.

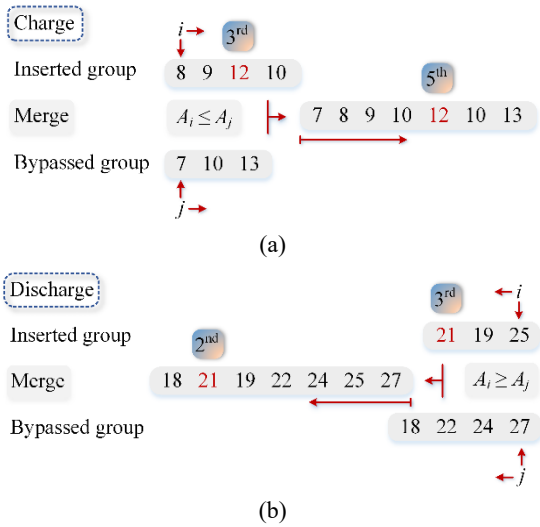


Fig. 9. Examples of the voltages balancing analysis in Fig. 8 of (a) charging and (b) discharging capacitors.

the following control periods until it is bypassed.

Fig. 8(b) shows a similar analysis when the arm current discharges the capacitors. At this time, suppose A_p moves from A_{pi} to the right due to exchanged orders. After using the TWMS of pointers in descending order, as shown in Fig. 2(b), A_p moves to the left, and quickly reduces the possibility of a mistaken triggering in choosing the s' SMs with the highest capacitor voltages. It should be mentioned that when the TWMS of pointers in ascending order is used while discharging, at least p-1 of the voltages are on the left of A_p. Thus, A_p still moves to the right, and the possibility of a mistaken triggering gradually increases. Likewise, the TWMS of pointers in descending order is not suitable for charging capacitors. Thus, the proposed TWMS strategy in Fig. 5 is the most effective way to balance capacitor voltages in the selections of pointers in ascending or descending order.

To give an example of the above analysis above, Fig. 9 shows two arrays sorted by the proposed TWMS strategy under non-ideal conditions. While charging, the number in disorder that is shown in red (also represented as A_p in Fig. 8(a)) moves to the right of the array after the TWMS (from 3rd to 5th). Therefore, the possibility of a mistaken triggering decreases, because the inserted SMs for the next control period are chosen from left to right when charging. A similar process can be obtained while discharging the capacitors. The number in disorder moves to the left in this situation. This also helps reduce the possibility of a mistaken triggering, since the inserted SMs for the next control period are chosen from right to left during discharging.

In conclusion, although the SMs with the highest or lowest voltages can be inserted with a lag of a few control periods, leading to larger voltage variations, the TWMS strategy can still balance the capacitor voltages under non-ideal conditions.

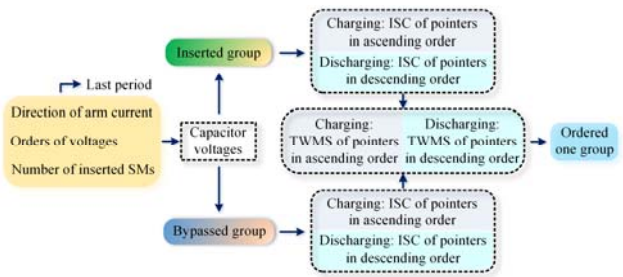


Fig. 10. Block diagram of the ISC-TWMS strategy in non-ideal conditions.

C. Proposed ISC-TWMS Strategy

To reduce the capacitor variations caused by exchanged orders, it is necessary to correct the orders in each control cycle to prevent accumulation. Considering that there are not many exchanged orders before accumulation, this paper proposes an ISC-TWMS strategy to reduce exchanged orders with a small computational burden. Specifically, insertion sort is applied to correct the inserted and bypassed groups before the TWMS. A block diagram of the ISC-TWMS under non-ideal conditions is shown in Fig. 10.

The core idea of the insertion sort is to insert a number into an already ordered array and to keep the order [15]. To be specific, the number to be inserted (called a *key*) is compared sequentially with the values in an ordered (assume ascending order) array. When the *key* is larger, the *key* is copied to the next position of the compared value. If the *key* is not larger, the compared value moves to the next position. After the *key* is inserted, choose the next number to be inserted as a new *key* and repeat these operations until all of the numbers are inserted. An example of insertion sort on the array={5,2,4,6,1,3,7,8,9} is shown in Fig. 11, in which the *key* is held in the orange rectangle.

The insertion sort has a significant advantage since it can be executed at a high speed on a basically ordered array. This

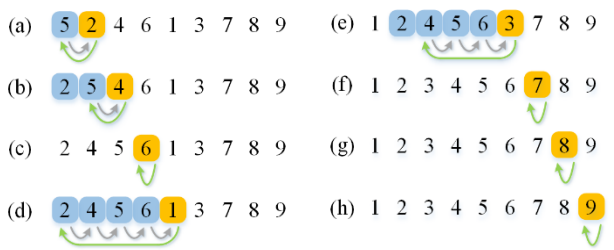


Fig. 11. Operations (a)-(h) of insertion sort on the array= {5,2,4,6,1,3,7,8,9}.

is due to the fact that a lot of moving operations are avoided, as shown in Fig. 11(c), (f), (g) and (h). Therefore, when an array of N numbers is basically ordered, the time complexity of the ISC is nearly linear $O(N)$ [15], and the speed is very close to the TWMS. Considering that there are relatively few exchanged orders before accumulation, and the capacitor voltages are basically ordered, the insertion sort can correct them very quickly with low computational efforts.

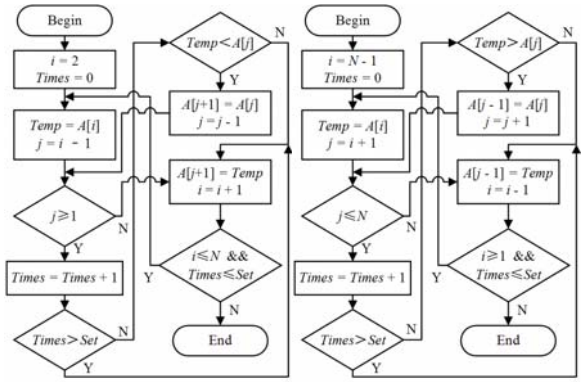
In addition, taking the allowed tolerances and the different applications of capacitance variations into consideration, it is unnecessary to correct the entire sequence of the capacitor voltages using ISC. Therefore, to reduce the excessive computational burden of the correction, this paper introduces limited steps into the ISC. One comparison counts as one step. If the operation steps are over a default value, the ISC will be immediately stopped. In fact, fewer limited steps will be required if the differences between the capacitances are small. Flowcharts of the ISC with limited steps are shown in Fig. 12, where $A[1..N]$ is the sequence, *Times* denotes the counter of the operation steps, and *Set* represents the default value for the limited steps.

Furthermore, ISC also can be divided into two types: pointers i in ascending and in descending order. Like the proposed TWMS strategy, when arm current charges the capacitors, the ISC of the pointers in ascending order, shown in Fig. 12(a), is used; when arm current discharges the capacitors, the ISC of the pointers in descending order, shown in Fig. 12(b), is applied. Thus, the correction operates much more effectively with limited steps, and the variations of the capacitor voltages are lower.

As a result, ISC is very suitable for correcting the inserted group and bypassed group under non-ideal conditions, and its time complexity is nearly $O(N)$ under this condition. Consequently, the time complexity of the ISC-TWMS is also nearly $O(N)$. The proposed ISC-TWMS strategy ensures the order of the capacitor voltages while maintaining a high speed.

IV. Simulation and Experimental Results

In order to verify the proposed strategies under both ideal and non-ideal conditions, a 501-level MMC-HVDC simulation has been established in PSCAD/EMTDC. The



(a) (b)

Fig. 12. Flowcharts of insertion sort with limited steps of pointers in (a) ascending and (b) descending order.

TABLE I
Parameters of the MMC Simulation

Parameter	Value
AC system voltage U_S	500 kV (L-L rms)
Transformer ratio U_S/U_V	500 kV/350 kV
DC bus voltage U_{DC}	±300 kV
Output Power P_{DC}	800 MW
Number of SMs per arm N	500
SM capacitance C_0	10 mF
SM capacitor voltage U_C	1.2 kV
Arm inductance L_0	100 mH
Control period T_s	200μs

main parameters of the MMC model are listed in Table I. Since the number of SMs is very large, the simulation uses a Thévenin equivalent circuit for the SM [6] and a NLC [12] is applied.

A. Verification of the Proposed TWMS Strategy under Ideal Conditions

The capacitances for all of the SMs are 10mF (Table I) under ideal conditions. Therefore, the TWMS strategy can precisely predict the orders of the capacitor voltages, and the TWMS can be applied without correction.

The capacitor voltages using the TWMS strategy and quicksort are shown in Fig. 13. It is obvious that the performances for balancing the capacitor voltages of the two algorithms are identical, which means that the sorted results of the TWMS are the same as those of quicksort. Thus, the prediction of the capacitor voltages and the TWMS strategy under ideal conditions are verified.

B. Verification of the ISC-TWMS Sorting Method under Non-Ideal Conditions

Considering the capacitance error and variation under ideal conditions, suppose that the capacitance variation is ±20%, where the capacitances of a randomly chosen 250 SMs are +20% (12mF) greater than the nominal value (10mF in Table I), and the capacitances of the rest of the SMs are -20% (8mF). Compared with a real MMC-HVDC system, the

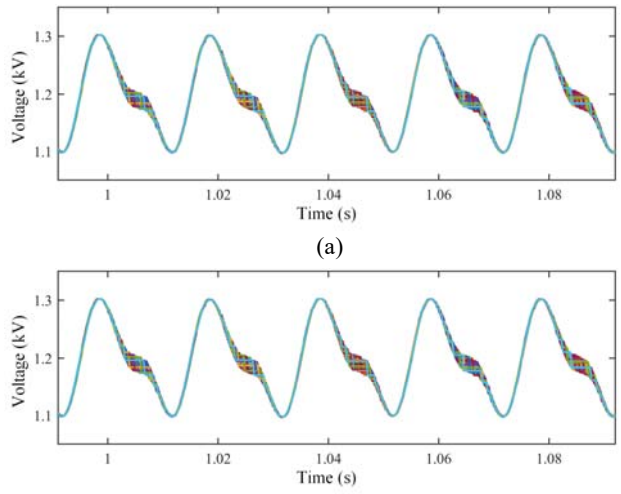


Fig. 13. Capacitor voltages of using (a) quicksort and (b) TWMS strategy in ideal conditions.

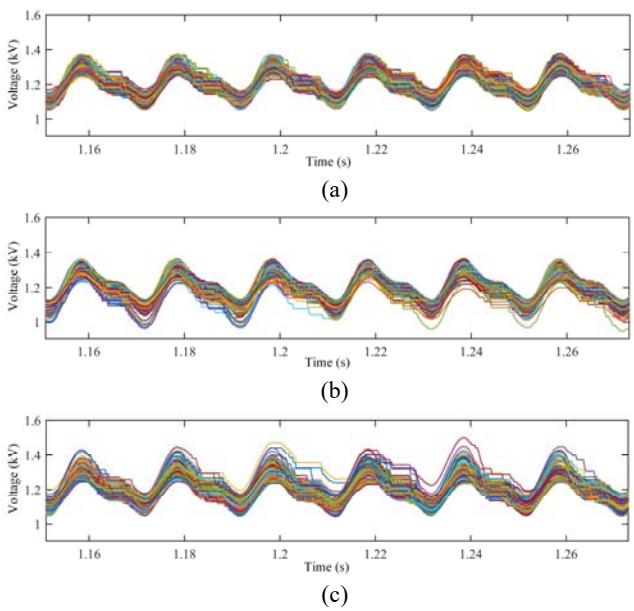


Fig. 14. Capacitor voltages of using (a) proposed TWMS strategy in Fig. 5, TWMS of pointers in (b) ascending and (c) descending order both in charging and discharging processes.

condition for balancing the capacitor voltages is much worse. However, it is able to verify the effectiveness of the proposed ISC-TWMS strategy.

The capacitor voltages using the TWMS strategy under non-ideal conditions are shown Fig. 14(a). Obviously, the variations of the capacitor voltages are larger due to exchanged orders. However, the voltages are still stabilized and balanced.

To verify the effectiveness of balancing the capacitor voltages of the proposed TWMS strategy, comparisons of the capacitor voltages using different TWMS strategies in terms of the orders of the pointers are shown in Fig. 14. When the TWMS of the pointers in ascending order is used in both the charging and discharging processes, as shown in Fig. 14(b),

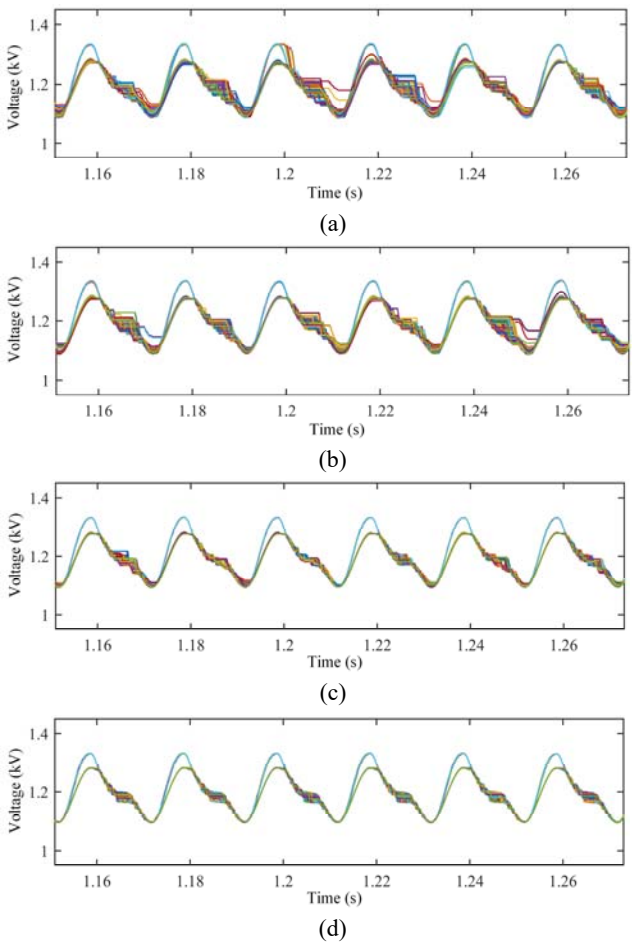


Fig. 15. Capacitor voltages of using ISC-TWMS with (a) limited 250 steps, (b) limited 500 steps, (c) limited 1000 steps and (d) quicksort in non-ideal conditions.

the capacitor voltage variations increase by 31.5% during discharging. Similarly, Fig. 14(c) shows the capacitor voltages balancing waveforms when the TWMS of the pointers in descending order is used in both the charging and discharging processes. It can be seen that the variations of the voltages greatly increase by 39.8% during charging. Therefore, the proposed TWMS strategy in Fig. 5 shows the best performance in terms of balancing voltages in the selections of pointers in ascending or descending order.

The capacitor voltages under non-ideal conditions using the ISC-TWMS strategy with different limited steps are shown in Fig. 15. The capacitor voltages of the proposed ISC-TWMS limited to 250 ($N/2$, N=500) steps are shown in Fig. 15(a). Compared with the TWMS strategy without the ISC in Fig. 14(a), the voltage variations are evidently decreased although there are not many limited steps, indicating the effectiveness of the ISC. The voltages with the limited 500 (N) steps are shown in Fig. 15(b), and the variations decrease further. In addition, the limited 1000 ($2N$) steps in Fig. 15(c) show a better voltage balancing effect. The larger the number of limited steps, the lower the variations of the capacitor voltages become. In comparison with quicksort,

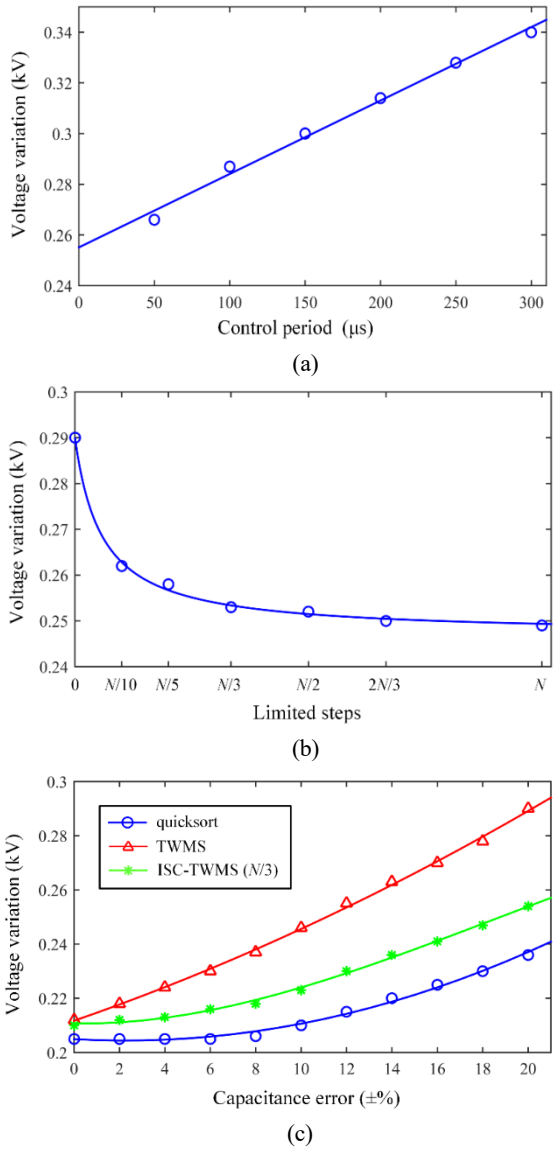


Fig. 16. Capacitor voltage variation under different conditions: (a) Capacitor voltage variation of using TWMS with different control periods, (b) Capacitor voltage variation of using ISC-TWMS with different limited steps and (c) Capacitor voltage variation of using quicksort, TWMS and ISC-TWMS (*N*/3) with different capacitance errors.

shown in Fig. 15(d), the variations of Fig. 15(c) are almost the same.

As a result, it is unnecessary to completely correct the array, and the required limited steps are different for different situations. To analyse the primary influence factors of the capacitor voltage variation, Fig. 16 shows the capacitor voltage variations with different control periods, limited steps and capacitance errors.

It should be mentioned that the transient performances of a MMC-HVDC transmission system using the proposed TWMS and ISC-TWMS under non-ideal conditions are satisfying. Fig. 17 shows the transient performances of the proposed TWMS strategy under non-ideal conditions. It can

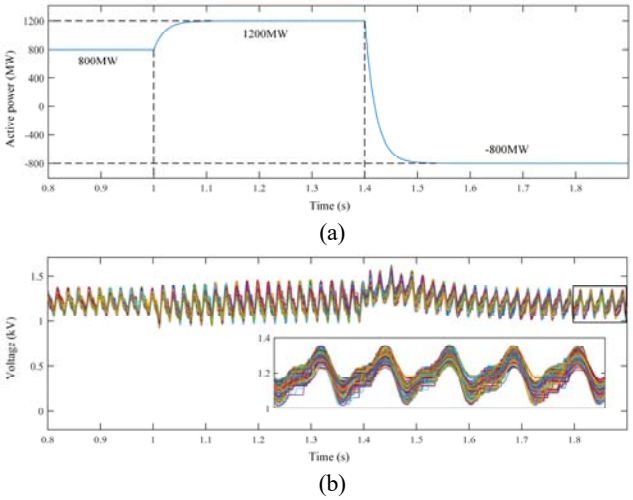


Fig. 17. Transient performances of the proposed TWMS strategy: (a) active power and (b) capacitor voltages.

be seen that the active power reference changes from 800MW to 1200MW at 1.0s and from 1200MW to -800MW at 1.4s. It can be seen from Fig. 17(a) that the active power responds quickly without steady-state error, and that the capacitor voltages 17(b) also reach the steady-state very quickly. As a result, although the capacitor voltage variation of the TWMS is larger under non-ideal conditions, it still shows satisfactory transient performance even in the event of a power reversal. In addition, the transient performance is similar when using the ISC-TWMS strategy, since the capacitor voltage variation is lower due to the correction of the exchanged orders.

C. Experimental Results

To verify the high speed of the proposed sorting methods, experiments with a DSP controller TMS320F28335 (the highest CPU rate is 150MHz) have been carried out. By using the DSP to sort *N* numbers, the execution times of quicksort, TWMS and ISC-TWMS (*N*/3 limited steps) are measured. The *N* numbers to be sorted are the capacitor voltages generated from corresponding MMC simulations at a certain instant in PSCAD. The procedures to measure the execution time are as follows. Set an output channel in the DSP (for instance GPIO0) to be the high-level. Then start the sorting method. When the sorting process ends, set the output channel GPIO0 to the low-level. Finally, use an oscilloscope to capture the voltage level of the output channel GPIO0 and measure the time of the high-level, which is equal to the execution time of the sorting process.

The proposed sorting methods show their advantages with a large number of SMs (over 100 SMs per arm). Therefore, to verify the main advantages of high speed and high efficiency of the TWMS and ISC-TWMS, it is necessary to sort a huge amount of data in a controller. A photo of the controller experimental setup for testing the execution time of sorting to verify the high speed is shown in Fig. 18, and an example waveform for measuring the execution time is shown in Fig.

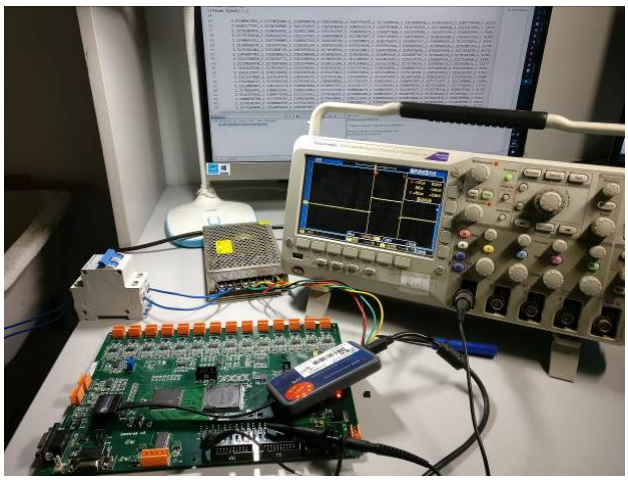


Fig. 18. Photo of controller experimental platform of testing the execution time of sorting.

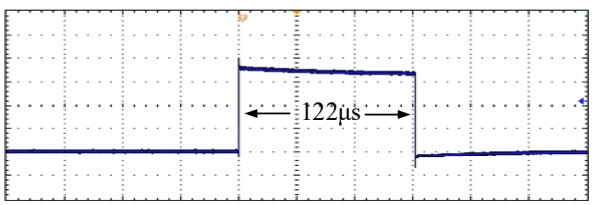
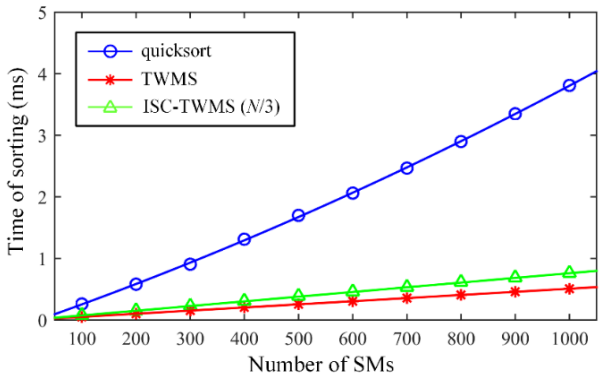


Fig. 19. Waveform of the output port GIPO0 to measure the execution time.

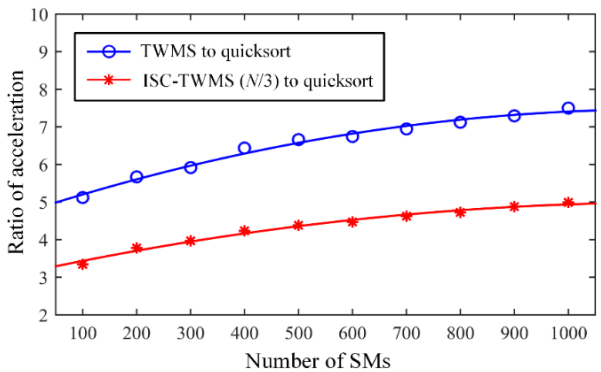
19.

Fig. 20 shows the results of the experiments. The measured times of the quicksort and TWMS with different numbers of SMs are shown in Fig. 20(a), and the ratios of the accelerations of TWMS and ISC-TWMS with limited $N/3$ steps to quicksort are shown in Fig. 20(b). Obviously, the fitted curve of quicksort in Fig. 20(a) satisfies $O(N \lg N)$. This demonstrates the low efficiency and enormous implementation weight of quicksort. For TWMS, the fitted curve in Fig. 20(a) clearly satisfies $O(N)$. This indicates good linearity, and its speed is much higher than that of quicksort, which results in great savings in terms of execution time. The ISC-TWMS with limited $N/3$ steps also satisfies linear $O(N)$. Although the speed of ISC-TWMS is a little slower than that of TWMS, it is still higher than quicksort, which reduces the computation efforts.

When the number of SMs is larger than 100, it can be observed from Fig. 20(b) that the ISC-TWMS strategy is at least 3 times faster than quicksort, and that the ratio increases with more SMs. More advanced controllers with higher CPU rates are able to execute the quicksort process in less time. However, the curves of the ratio of the acceleration shown in Fig. 20(b) can still be satisfied. Consequently, the proposed TWMS and ISC-TWMS strategies are much faster than the traditionally used quicksort. This greatly reduces the implementation efforts and accelerates the sorting process. With the decreased time cost of the proposed control strategy, a less complicated and less expensive controller structure can be applied.



(a)



(b)

Fig. 20. Results of experiments: (a) measured time of quicksort, TWMS and ISC-TWMS with limited $N/3$ steps and (b) ratios of acceleration of TWMS and ISC-TWMS (limited $N/3$ steps) to quicksort.

V. CONCLUSIONS

This paper proposes a TWMS and ISC-TWMS with limited steps for efficiently sorting the capacitor voltages in MMC-HVDC systems. Combined with the features of the MMC control strategy, the proposed sorting methods are extremely fast, which greatly reduces the computational burden of controllers. Thus, the time costs for sorting are decreased by the proposed methods, which helps to lower the designing difficulties and hardware costs of controllers. In addition, the accelerating ratios of the proposed sorting methods grow with the number of SMs. Hence, the TWMS and ISC-TWMS become more efficient with an increasing number of SMs. 501-level MMC time-domain simulation results in PSCAD/EMTDC demonstrate the satisfactory performance of the proposed sorting methods. Experimental results with a DSP controller (TMS320F28335) verify the extremely high speed of the proposed sorting algorithms. In conclusion, the proposed sorting algorithms are highly suitable and strongly recommended for applications of MMC-HVDCs that require thousands of SMs.

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