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An Accurate Modeling Approach to Compute Noise Transfer Gain in Complex Low Power Plane Geometries of Power Converters

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Abstract

An approach based on a 2D lumped model is presented to quantify the voltage transfer gain (VTG) in power converter low power planes. The advantage of the modeling approach is the ease with which typical noise reduction devices such as decoupling capacitors or ferrite beads can be integrated into the model. This feature is enforced by a new modular approach based on effective matrix partitioning, which is presented in the paper. This partitioning is used to decouple power plane equations from external device impedance, which avoids the need for rewriting of a whole set of equation at every change. The model is quickly solved in the frequency domain, which is well suited for an automated layout optimization algorithm. Using frequency domain modeling also allows the integration of frequency-dependent devices such inductors and capacitors, which are required for realistic computation results. In order to check the precision of the modeling approach, VTGs for several layout configurations are computed and compared with experimental measurements based on scattering parameters.

Key words: Electromagnetic interference, Lumped model, Noise, Power converter, Power plane, Printed circuit layout

I. INTRODUCTION

EMI control and computation for power converters has been a topic of extensive research over the last ten years. Although EMI issues are mainly related to meeting standards in terms of conducted and radiated noise, it is still a wide topic that can be divided in two main areas. The first area deals with noise that affects external devices mostly in the conducted frequency range. This topic has been covered in many publications. Passive and active EMI filters are the key components used to meet conducted EMI standards and they have been improved in terms of their frequency response [1]-[4] and density [5], [6]. In addition, several efforts have been made to model the whole power converter in terms of EMI prediction [7]-[13]. These studies provide the EMI model of a particular power converters such as a direct matrix converter [7], buck converter [8] or DC-DC converter considering parametric uncertainties [9]. EMI prediction for a general power converter is developed in [10] based on the experimental impedance extraction of each part of the power converter. This approach is useful once a prototype is developed to solve the EMI issues. Conducted EMI prediction for a power inverter in the early design stage based on PEEC modeling is presented in [11]-[12]. The authors of [13] divide a power converter into active, ground and passive blocks. The impedance matrices of the passive blocks are deployed to predict the EMI current.

The second area is related to the noise propagation inside the power converter PCB which affects measurement precision and low power circuit supplies, such as embedded controllers and sensing amplifiers. As shown schematically in Fig. 1, the problem is mainly due to high power transistor switching, which creates perturbations in low power circuit supplies that affect their logic and analog measurements. These perturbations can easily drive the power converter into erratic control behavior resulting in poor power converter reliability. Although no standard exists in terms of an acceptable noise margin, all of the components have strong

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requirements for their supply variation. A typical DSP sustains a small variation of 5% in its supply. Operational amplifiers offer very poor rejection of noise in the EMI frequency range. Consequently, the supply voltage must be tightly controlled by the designers. As shown in Fig. 1, the inherent low impedance of the low power plane provides suitable and complex propagation paths for noise (dashed lines) since this plane connects all the noise sources together (i.e. power transistors) through the parasitic mutual inductance and capacitance. This is especially true for the recently developed multiport converters [14] and modular multilevel converters [15], where the low power plane areas are critical for supplying the numerous devices attached to them. The complexity of these power planes provides several propagation paths for noise.

In laboratory research, it is possible to use a high cost commercial DC source to supply each gate driver, so that the low power plane does not exist. However, there is always a common point connecting all of the DC sources, which creates paths for noise propagation. The resulting noise is unpredictable due to unknown propagating paths inside the DC sources. Conversely, in industry, to ensure low cost products with a high density, manufacturability and high reliability, all of the parts of the converter must be placed compactly together. In this case, the low power plane is essentially required.

The main purpose of this paper is to provide a modeling approach that helps power converter designers to compute the VTG between each of the port pairs of the low power plane and to analyze the effect of EMI attenuators on the VTG. This knowledge is mandatory for optimizing the immunity of the low power plane. Based on this knowledge, it is easier to select proper noise attenuators and to determine the effect of their spatial distribution on noise performance. The method employs an established 2D lumped model for power planes. When compared with other methods, the lumped model requires less computational resources while being precise for the power plane model [19]. The current boundary conditions are utilized to deal with the complex geometry of the power plane without extra computation. In addition, the real impedance of external devices placed on the power plane is taken into account in the model as an additional matrix. This additional matrix allows fast computation and optimization capability of the model. Furthermore, the VTG, which represents the noise propagation, is computed and compared with experimental measurements to validate the computational model. Based on the VTG results, the effect of each external device on the VTG is analyzed in detail, providing insight into the optimal design of the EMI attenuation.

This paper is organized as follows. Section II presents the noise propagation issues in the low power planes of power converters in detail. In section III, the modeling approach is

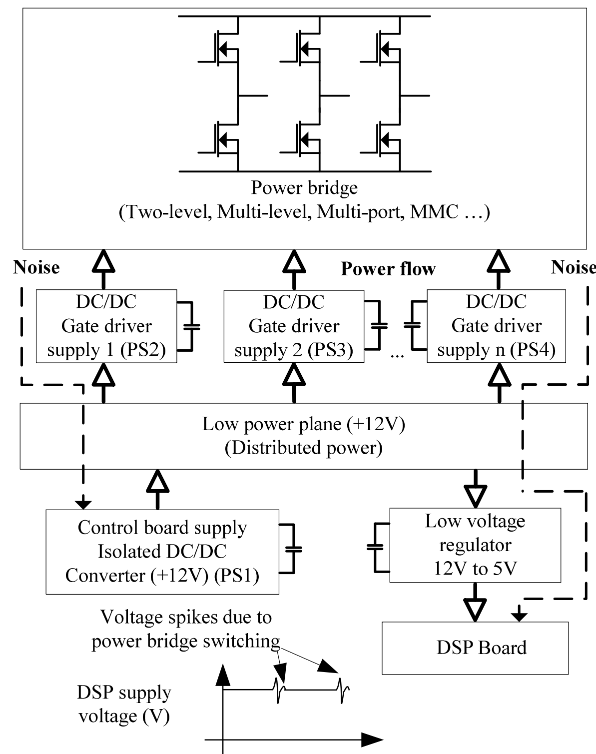


Fig. 1. Noise propagation in low power part of converter.

introduced. Section IV gives computational and experimental results of several low power plane configurations. Some conclusions are presented in section V.

II. NOISE PROPAGATION IN LOW POWER PLANE

Fig. 1 illustrates a typical power converter structure. An isolated DC/DC converter (PS1) regulates a +12V voltage from a power source. The output of this DC/DC converter is connected to a power plane distributing power for other DC/DC converters. These isolated DC/DC converters provide positive and negative rails to supply gate drivers and micro-controllers. During the power converter operation, a very high $\partial V/\partial t$ appears across the power transistors, generating noise through the numerous stray inductances in the converter structure. This noise travels along the connecting traces, passes through the parasitic elements of the gate drivers and distributed DC/DC converters before reaching the low power plane. The isolated capacitance between the input and output sides of the DC/DC converter is in the range of a few *nF*, which provides an easy way for noise to propagate. Once in the low power plane, the noise propagates in a complex way to the other DC/DC converters and other low-voltage devices, resulting in voltage spikes in their supplies. These voltage spikes can cause inaccurate voltage and current measurements, and malfunction of DSP and gate drivers. In order to attenuate the noise propagation, EMI attenuators such as ferrite beads, decoupling capacitors

and EMI filters can be placed on the power plane. However, since the noise propagation path is not well determined due to complex 2D geometry, the noise performance is unpredictable, which further complicates the design process. This issue is solved by the proposed modeling approach. The obtained results are mandatory knowledge for optimizing the immunity of the low power plane.

A. Low Power Plane Modeling

In recent years, low power plane structures have been widely investigated by microwave researchers. The rectangular power plane, which features the simplest geometry, has been efficiently modeled by the cavity - lumped model [16] – [18]. The decoupling capacitor is taken into account by the transmission line elements method [19] – [20]. The above approaches are fast and accurate. However, they are unable to analyze the power plane in the complex geometry which is typical in power electronic board designs.

Several approaches have been developed for irregular power plane geometries. The 2D contour integral equation method is introduced in [21] – [22], which separates arbitrary shape into small segments with the assumption of a uniformly distributed voltage. A FEM - SPICE method is introduced in [23] – [25]. In this approach, the impedance of each part of the power plane is calculated by the finite element method. Then the complete circuit is solved by SPICE software. This method is efficient for modeling the arbitrary geometry power plane due to the FEM. However, the computational burden is increased with the PCB structure complexity. The arbitrary power plane is modeled accurately in the time-domain by the discontinuous Galerkin method [26]. However, the time-domain model is not effective for integration with the models of the other parts of the power converter. A multi-conductor transmission line based on a lumped model is presented in [27] – [28]. This method represents irregular geometry by a combination of several rectangular cells which are presented by the established lumped model in the transmission matrix form. The complete model is created by multiplying the cascaded cells' matrix. The segmentation and treatment for each cell's matrix become complicated with the power plane geometry complexity. In addition, several modifications in the transmission matrices must be done once the power plane geometry changes, which limits the method being applied in the design stage. The authors of [28] take the decoupling capacitor into account as a multiplied matrix, where its impedance is placed on a diagonal line with an assumption of the device's small dimensions. This limits the approach in terms of modeling large dimension devices which are usually placed in the power plane. In addition, the optimization for decoupling capacitor selection and placement is difficult since its matrix interacts with the whole set of equations.

There are several parasitic extraction tools for PCBs, such as FastHenry, FastCap (free), Q3D Ansoft, StarRC and QRC

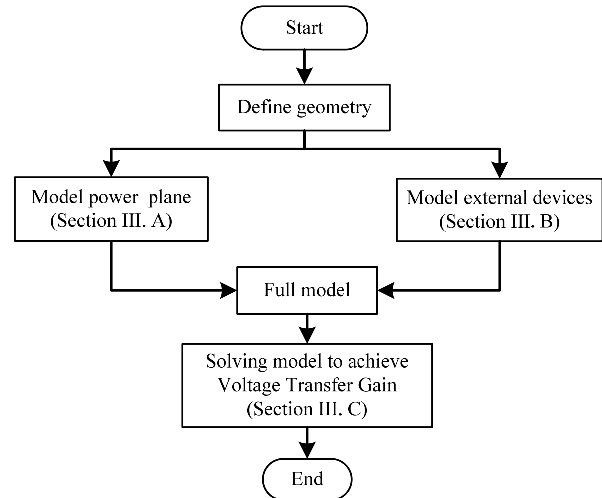


Fig. 2. Modeling approach.

(commercial), using complex methods such as FEM, PEEC and Method-of-Moment. Even though software provides many advantages, engineers must have knowledge of the problem's physics and the limits of the software's method which may be more complicated than the problem itself [29]. Therefore, the developed 2D lumped model which is simple, accurate and can be employed as a part of the whole converter model, is very useful for researchers.

B. Near Field Coupling in Power Converters

Another source of noise resulting from power converters is the near field coupling from external sources (cables), which has been analyzed for EMC applications in several publications [32] - [35]. The near field is created by the large area of a strong current slope circuit [32] - [33], which is a high power circuit or other circuit outside the enclosure of a power converter. However, low power circuits are always located at some distance from the power parts of the convert to avoid electrical arcs or PCB insulation failure. In addition, the converter cannot be placed much closer to the enclosure for safe packaging purposes. According to Biot and Savart's law shown in [34], the magnetic flux densities decay with cubic distance. Therefore, the aforementioned distances are very efficient for removing near field coupling. In addition, the ground plane with vias closed to the power converter circuit, which is a more general case of the low power plane, can further attenuate the field by 10-15dB [35]. Consequently, effect of near-field coupling on a power converter circuit is negligible and not considered in this paper.

III. MODELING APPROACH

An approach is developed to obtain a full model of the low-power plane with all of the external devices placed on it. The main idea of this approach is to model the power plane and the external devices separately, as summarized in Fig. 2.

First, the power plane geometry is separated into a number

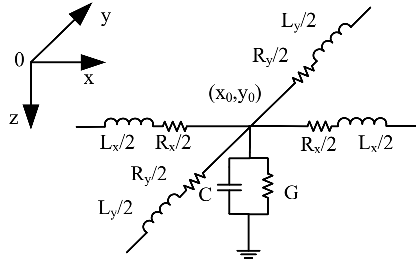


Fig. 3. Lumped model of one cell.

of small parts (hereafter called a 'cell') with dimensions $dx \times dy$. Based on several numerical investigations, cell dimensions 10 times smaller than the signal wavelength must be chosen to guarantee a constant current and voltage over the cell. Without losing generality, the power plane is assumed to be separated into n cells for the rest of this paper. Second, the power plane and the external devices are modeled independently before combining them into a full model. Considering the fact that these parasitic components may be different from those introduced in the datasheet, experimentally measuring the impedance of the external devices is suggested to guarantee the accuracy of the computational results. Third, the model is solved to obtain both the voltage distribution and the VTG. These steps are introduced in details in the following sections.

A. 2D Lumped Model for Complex Power Plane Geometry

The 2D lumped model is used to model each cell of the power plane [28]. As shown in Fig. 3, each cell is connected to 4 surrounding cells by serial resistances (R_x, R_y) and serial inductance (L_x, L_y). In addition, the impedance between the power and ground planes is represented by a shunt conductance (G) and a shunt capacitance (C). In the event that parts of the power plane have a small dimension, the cell parameters can be extracted using the finite element method. On the other hand, if the conduction width is very large compared to the PCB thickness, the border effect can be neglected resulting in a uniform field distribution between the planes. In this case, the parallel plane approximation is valid and the cell parameters are computed by the following equations [30]:

$$L_x = \frac{\mu h dx}{dy}; L_y = \frac{\mu h dy}{dx};$$
$$R_x = \frac{2R_s dx}{dy}; R_y = \frac{2R_s dy}{dx}; \quad (1)$$
$$C = \frac{\varepsilon dx dy}{h}; G = \omega \delta C;$$

where ω is the considered frequency, h is the height of the dielectric, μ is the permeability, δ is the loss tangent, ε is the permittivity, and R_s is the surface resistivity of the material.

To obtain the voltage and current distributions over the plane, Kirchhoff equations are developed in the remaining part of this section. In order to keep things simple, closed form equations are presented for a simple plane, making the extension to the complex plane geometry straightforward.

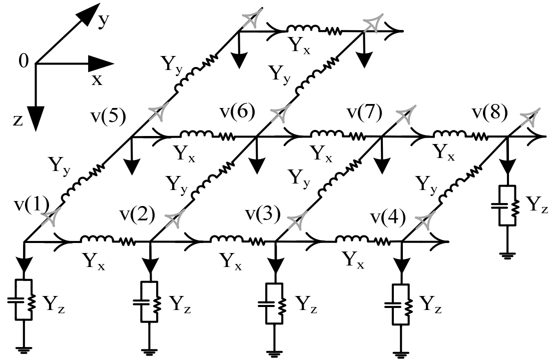


Fig. 4. Example for a 2D model of power plane.

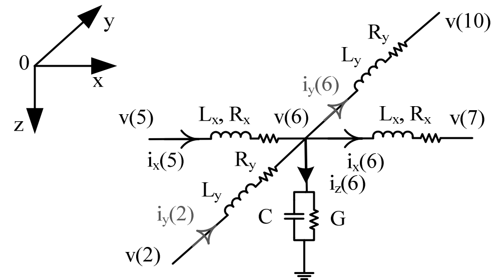


Fig. 5. Voltage and current definition at cell 6.

Fig. 4 shows a typical L-shape geometry power plane discretized into 10 cells corresponding to the node voltage (V(1), V(2)... V(10).) Of course, Kirchhoff's equations must be applied to all of the cells. However, due to limited space, only equations for cell number 6 are presented. The current and voltage definition of cell 6 are shown in Fig. 5. Applying Kirchhoff's voltage law in the $x-$ and $y-$ directions yields (2) and (3), respectively:

$$i_x(6) = [v(6) - v(7)](R_x + j\omega L_x)^{-1} \quad (2)$$

$$i_y(6) = [v(6) - v(10)](R_y + j\omega L_y)^{-1} \quad (3)$$

The Kirchhoff's current law yields:

$$i_z(6) = v(6)\left(G + \frac{1}{j\omega C}\right)^{-1} = i_x(5) - i_x(6) + i_y(2) - i_y(6) \quad (4)$$

The current of each cell is linked to that of the *neighbor cell*. Cell m is defined as the $x-$ *neighbor* or $y-$ *neighbor* of cell k if (5) or (6) is satisfied, respectively.

$$\begin{cases} X(m) - X(k) = dx \\ Y(m) - Y(k) = 0 \end{cases} \quad (5)$$

$$\begin{cases} X(m) - X(k) = 0 \\ Y(m) - Y(k) = dy \end{cases} \quad (6)$$

The vectors Q_x and Q_y are defined as the $x-$ *neighbor* and $y-$ *neighbor* vectors, respectively:

$$Q_x(k) = \begin{cases} m & if \quad \exists m \; satisfies \; (5) \\ 0 & if \quad \nexists m \; satisfies \; (5) \end{cases} \quad (7)$$

$$Q_y(k)=\begin{cases} m & if \quad \exists m \; satisfies \; (6) \\ 0 & if \quad \nexists m \; satisfies \; (6) \end{cases} \tag{8}$$

For instance, in Fig. 4, these vectors are:
$Q_x=[2\,3\,4\,0\,6\,7\,8\,0\,10\,0]^T; Q_y=[5\,6\,7\,8\,9\,10\,0\,0\,0\,0]^T$.

Obviously, the currents flowing outside of the power plane must be zero. This condition is applied to a cell that does not have a $x-$ or $y-$ *neighbor* using the definitions of Q_x and Q_y:

$$i_x(k)=0 \quad only\ if \quad Q_x(k)=0 \tag{9}$$

$$i_y(k)=0 \quad only\ if \quad Q_y(k)=0 \tag{10}$$

As clearly shown in (9) and (10), forcing $i_x(k)$ and/or $i_y(k)$ to zero can define the border cells represented by Q_x and Q_y, and then the geometry of power plane. This is the current boundary condition to tackle the irregular geometry of the power plane as long as the cells are either rectangular or approximated as a rectangular shape. This condition is generally met for the PCB designs in power electronic applications. In the example shown in Fig. 4, the current boundary condition is written as:

$$i_x(4)=i_x(8)=i_x(10)=0 \tag{11}$$

$$i_y(7)=i_y(8)=i_y(9)=i_y(10)=0 \tag{12}$$

In a more general way, based on cell equations (2)-(4) and the above definitions (5)-(10), the general Kirchhoff's laws for the cells shown in Fig. 4 are written in the matrix form as:

$$I_x=Y_xAV \tag{13}$$

$$I_y=Y_yBV \tag{14}$$

$$EI_x+DI_y=Y_zV \tag{15}$$

where V, I_x and I_y are the n x 1 column vectors representing the voltages and currents in the $x-$ and $y-$ directions for all of the cells, respectively. Y_x, Y_y and Y_z are the n x n diagonal admittance matrices in the $x-$, $y-$ and $z-$ directions, respectively. (13) and (14) are the Kirchhoff's voltage law equations in the $x-$ and $y-$ directions, respectively. (15) is the Kirchhoff's current law equation at each of the cells. The admittance matrices are described as follows.

$$Y_x(p,p)=[R_x(p)+j\omega L_x(p)]^{-1} \tag{16}$$

$$Y_y(p,p)=[R_y(p)+j\omega L_y(p)]^{-1} \tag{17}$$

$$Y_z(p,p)=\left[G(p)+\frac{1}{j\omega C(p)}\right]^{-1} \tag{18}$$

where p stands for the cell number. A, B, D and E are the n x n transformation matrices which are given as follows.

$$A(p,q)=\begin{cases} 1 & if \;\; q=p & and \;\; Q_x(p)\neq 0 \\ -1 & if \;\; q=Q_x(p) & and \;\; Q_x(p)\neq 0 \\ 0 & otherwise. \end{cases} \tag{19}$$

$$B(p,q)=\begin{cases} 1 & if \;\; q=p & and \;\; Q_y(p)\neq 0 \\ -1 & if \;\; q=Q_y(p) & and \;\; Q_y(p)\neq 0 \\ 0 & otherwise. \end{cases} \tag{20}$$

$$E(p,q)=\begin{cases} -1 & if \;\; q=p & and \;\; Q_x(p)\neq 0 \\ 1 & if \;\; p=Q_x(q) & and \;\; Q_x(p)\neq 0 \\ 0 & otherwise. \end{cases} \tag{21}$$

$$D(p,q)=\begin{cases} -1 & if \;\; q=p & and \;\; Q_y(p)\neq 0 \\ 1 & if \;\; p=Q_y(q) & and \;\; Q_y(p)\neq 0 \\ 0 & otherwise. \end{cases} \tag{22}$$

In (19)-(22), the conditions $Q_x(p) \neq 0$ and $Q_y(p) \neq 0$ are utilized to impose the current boundary conditions (9) - (10).

B. External Device Modeling

In this section, models of typical devices powered by a low power plane such as DC/DC converters, decoupling capacitors or filters, are presented. In practice, external devices are soldered onto PCBs through pads and vias which can effect the noise performance. However, the effect of the vias can be negligible due to their low impedance (below 100MHz). Moreover, the coupling between the power plane and the external devices are also neglected in the EMI frequency range. The modeling of this part involves the following two steps:

1) The impedance of devices is measured experimentally using a Network Analyzer. This ensures the accuracy of the parasitic elements of the device which can vary unexpectedly from the manufacturer specifications. The impedance is measured by scattering the parameters with proper methods, i.e. series and shunt, due to the impedance level in each of the frequency ranges.
2) The auxiliary admittance matrix Y_{aux} is created by inserting the impedance of the devices into the matrix's positions corresponding to the devices' physical locations. There are two locations for the equivalent impedance in Y_{aux} according to the device's physical dimensions. When the device's dimensions are smaller than the cell's dimensions, as with a decoupling capacitor, the equivalent impedance is placed in a diagonal line at the cell's number. Otherwise, once the device's dimensions are larger than the cell's dimensions, as with a DC/DC converter, the equivalent impedance is placed at a position where the column and row correspond to the cell's number to which the device is attached. Generally, Y_{aux} is defined as follows.

$$Y_{aux}(p,q)=\begin{cases} Z_{pq}^{-1} & if \; \exists Z_{pq} \; at\; cell\; p-q \\ 0 & otherwise. \end{cases} \tag{23}$$

Then, the full admittance between the power and the ground is obtained as Y_{aux} + Y_z. Using Y_{aux} as an additional matrix provides several advantages.

First, it is easy to change/add new devices in the model by simply modifying Y_{aux} at the corresponding matrix elements.

Second, the voltage/current distributions can be solved easily with multiple excited voltage ports, which is especially true in converters since noise can propagate from several sources simultaneously. The solving approach is presented in

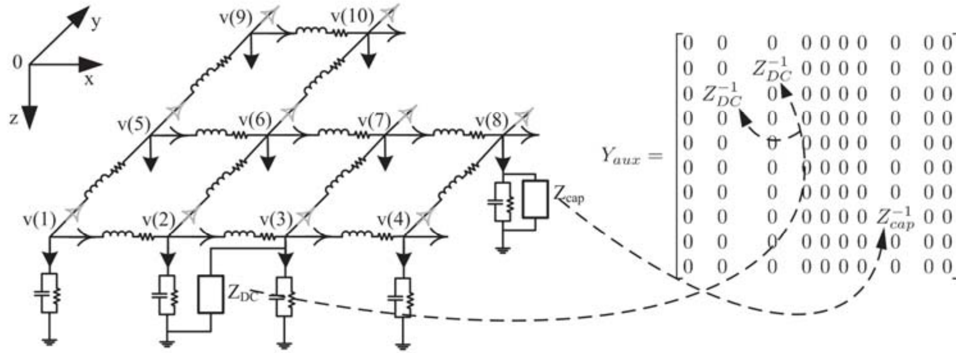


Fig. 6. 2D lumped model with external devices.

section III-C by canceling the corresponding columns of the connecting matrix.

Third, it allows to optimize the selections and locations of the decoupling capacitors and other devices since Y_{aux} can be treated independently in the model.

Fig. 6 shows the power plane structure given in Fig. 4 with added external devices. In this configuration, a decoupling capacitor is soldered between the power and ground plane at *cell 8* whereas a DC/DC converter is soldered at *cell 2* between the ground and *cell 3* on the power plane. The equivalent impedance of the DC/DC converter and decoupling capacitors are Z_{DC} and Z_{cap}, respectively. The admittance matrix Y_{aux} is defined at the right hand side of Fig. 6. As can be seen, the admittance Z_{DC}^{-1} is inserted into Y_{aux} at $Y_{aux}(2,3)$ and $Y_{aux}(3,2)$, whereas Z_{cap}^{-1} is placed at $Y_{aux}(8,8)$.

C. Solving Approach

In order to compute the VTG, the voltage vector, i.e. V, is decoupled from the source voltage and the distribution voltage vectors, i.e. V_0 and V_c, respectively.

$$V = V_0 + V_c \tag{24}$$

Assuming that the source voltage is excited at cell e, the source voltage vector is given as:

$$V_0(p) = \begin{cases} 1 & if \quad p = e \\ 0 & otherwise. \end{cases} \tag{25}$$

In order to represent (13) and (14), new transformation matrices A_0, A_c, B_0, B_c are created to satisfy (26) - (27).

$$AV = A_0 V_0 + A_c V_c \tag{26}$$

$$BV = B_0 V_0 + B_c V_c \tag{27}$$

$$A_0(p,q) = \begin{cases} 1 & if \quad q = p = e \\ -1 & if \quad q = e = Q_x(p) \\ 0 & otherwise. \end{cases} \tag{28}$$

$$B_0(p,q) = \begin{cases} 1 & if \quad q = p = e \\ -1 & if \quad q = e = Q_y(p) \\ 0 & otherwise. \end{cases} \tag{29}$$

$$A_c(p,q) = \begin{cases} 0 & if \quad q = e \\ A(p,q) & otherwise. \end{cases} \tag{30}$$

$$B_c(p,q) = \begin{cases} 0 & if \quad q = e \\ B(p,q) & otherwise. \end{cases} \tag{31}$$

Replacing (24), (26) and (27) into (13) - (15) yields:

$$I_x = Y_x(A_0 V_0 + A_c V_c) \tag{32}$$

$$I_y = Y_y(B_0 V_0 + B_c V_c) \tag{33}$$

$$EI_x + DI_y = Y_z(V_0 + V_c) \tag{34}$$

In (34), Y_z is replaced by Y_{aux} + Y_z to take the impedance of the external devices into the full model, as explained in section III-B:

$$EI_x + DI_y = (Y_z + Y_{aux})(V_0 + V_c) \tag{35}$$

From (32), (33) and (35), the voltage distribution on the power plane, i.e. V_c, is computed by:

$$V_c = (EY_x A_0 + DY_y B_0 - Y_z - Y_{aux})^{-1} T \tag{36}$$

where:

$$T = (-EY_x A_c - DY_y B_c + Y_z + Y_{aux}) V_0 \tag{37}$$

By injecting a voltage of *1V* at the excitation cell, i.e. cell *e*, the VTG from cell *e* to a typical cell l is computed as:

$$VTG_{e,l} = \frac{V(l)}{V(e)} = V(l) \tag{38}$$

IV. Experimental Results

A. Experimental Setup

In this section, a typical power converter low-power plane structure is analyzed through both computations and experimentation. The circuit and the board layout are depicted in Figs. 7 (a)-(b). The part numbers of the devices connected to the plane are summarized in Table. I. As shown in Fig. 1, the PS1 (typically 12V) supplies PS2, PS3 and PS4 (typically ±12V). These isolated low power converters then supply the power transistor gate drivers. There are 5 footprints on the board's top layer (x1 to x5) to include two types of capacitors, namely film and/or ceramic. The objective is to study the usual capacitor decoupling approach to validate the proposed modeling approach. Both capacitor technologies and their spatial distribution effects on the VTG are studied to provide a comprehensive validation. There is also one footprint on the board (x6) to include a ferrite bead (B1), a device typically used to solve noise problems at the

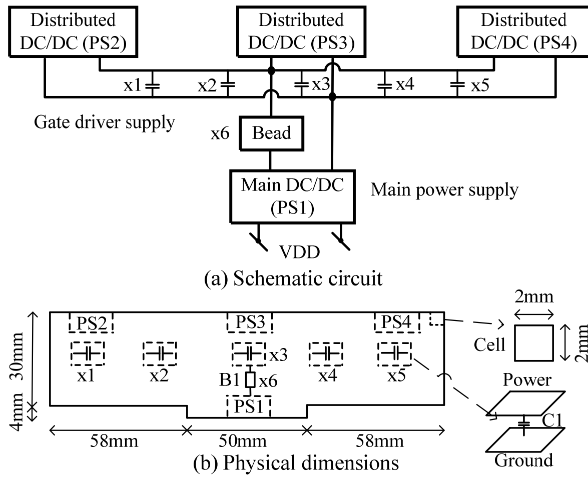


Fig. 7. Prototype of low power plane.

TABLE I
LIST OF EXTERNAL DEVICES

Designator	Manufacturer	Part Number
PS1	TRACOPOWER	THN 15-4812WI
PS2, PS3, PS4	CUI Inc.	VASD1-S12-D12-SIP
C1	EPCOS (TDK)	B32529C104J
B1	TDK	HF30ACC453215-T

board level. As mentioned in section II, the VTGs between each device pair (PS1 and PS2, PS1 and PS3...) are essential for quantifying the noise propagation in the power plane. The VTGs are extracted experimentally based on the scattering parameters, which is a standard function on every VNA. The scattering parameters are then converted to the VTG by a procedure described in the Appendix. For the remainder of this section, the focus will be on the VTG between PS2 and PS1. The other VTGs will be obtained in the same way.

B. 2D Lumped Model Parameters Identification

Prior to computing the VTG, the parameters are needed for both the low power plane and the external components. First, the low power plane is divided into small cells whose dimensions must be less than 15cm corresponding to the highest considered frequency of 100MHz following the conditions discussed in section III. Based on a numerical investigation, using square cells of 2mm × 2mm ensures good precision up to 100MHz, yielding the cell parameters given in Table II, as calculated by (1).

Second, the external devices impedance must be measured to complete the model. This task is performed using an Agilent Network Analyzer E5061B. The impedance of the PS1 output and PS2 input are measured offline by the VNA. Since the impedance of a DC/DC converter is same in both offline and online operations, as proved in [31], these results are valid for all of the operating conditions. The impedance of PS1, PS2, C1 and B1 are presented in Fig. 8. As shown in Fig. 8, the impedance of PS1, PS2 and C1 are capacitive at low frequencies and inductive at high frequencies. The

TABLE II
PARAMETERS FOR COMPUTATION

Resistance (R_x=R_y)	Inductance (L_x=L_y)	Capacitance (C)
0.96 $m\Omega$	1.8831 nH	0.1134 pF

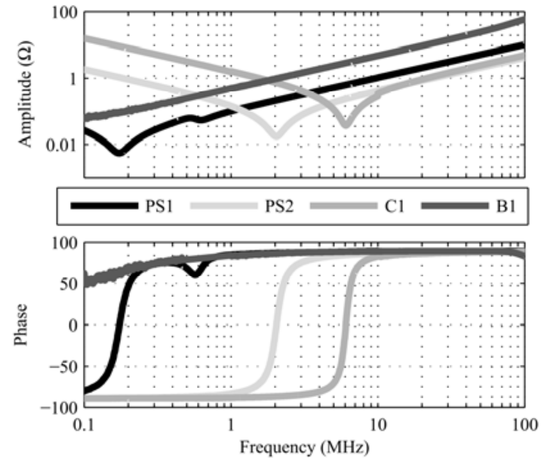


Fig. 8. Measured impedance of external devices.

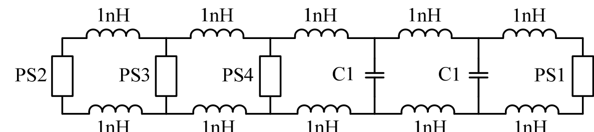
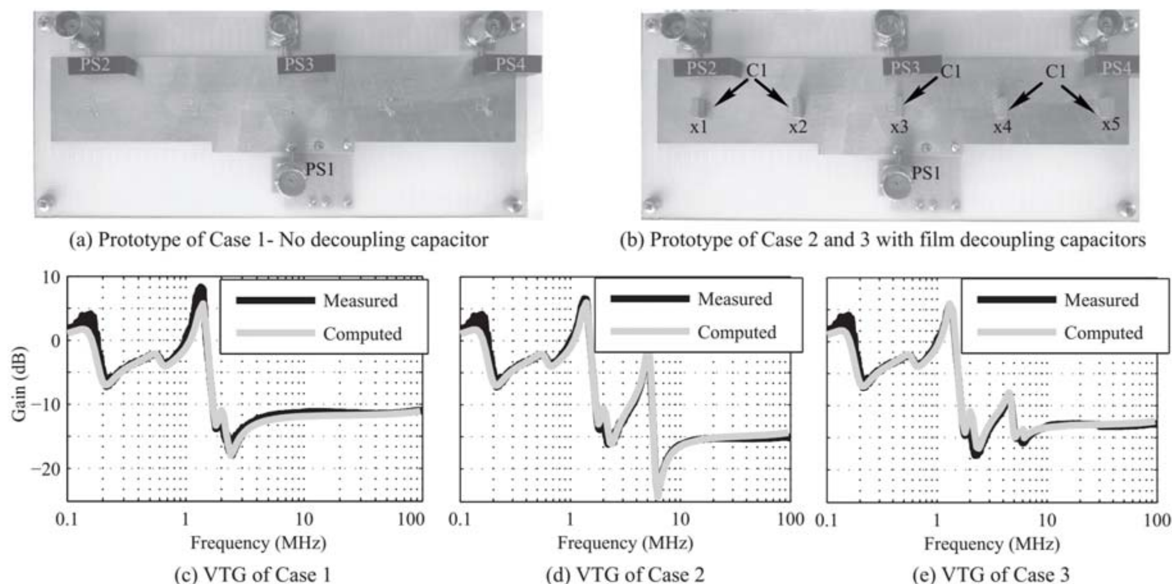


Fig. 9. 1D lumped model neglecting power plane.

resonant frequencies are 200kHz, 2.2MHz and 6MHz, respectively. The impedance of PS1 is lowest at frequencies below 1MHz and highest at frequencies above 10MHz. The effects of all of the external devices on the VTG are presented in the following sections.

C. VTG with Decoupling Capacitors

In order to validate the proposed modeling approach, the spatial distribution of the decoupling capacitors on the VTG is analyzed. In order to make this comparison, two decoupling capacitors are inserted into different rooms of the low power plane and the VTG is computed from 100kHz to 100MHz. For comparison, a lumped model neglecting the low power plane is used. This model, shown in Fig. 9, includes the impedance of PS1, PS2, PS3, PS4 and two decoupling capacitors C1. To account for the leads of the components, a small connecting inductance of 1nH is added. Three cases are presented for the low power plane. In the first case, no decoupling capacitor is soldered onto the board. In the second case, decoupling capacitors are inserted into x1 and x2 rooms. In the third case, capacitors are inserted into x4 and x5 rooms. The VTG of the both models is shown in Fig. 11. As depicted in Fig. 11, the VTGs are the same for each of the three cases below 2.5MHz. This means that the VTG in this frequency range is managed by the impedance of the devices in the circuit, while the influence of the low power plane is negligible. Over 5MHz, the clear influence of



(a) Prototype of Case 1- No decoupling capacitor (b) Prototype of Case 2 and 3 with film decoupling capacitors

(c) VTG of Case 1 (d) VTG of Case 2 (e) VTG of Case 3

Fig. 10. VTG of low power plane for different cases of decoupling capacitors. (a) Prototype without decoupling capacitors, (b) Prototype with decoupling capacitors, Computed and measured VTG of (c) Case 1 - No decoupling capacitor, (d) Case 2 - 2 decoupling capacitors at x1 - x2 and (e) Case 3 - 2 decoupling capacitors at x4 - x5.

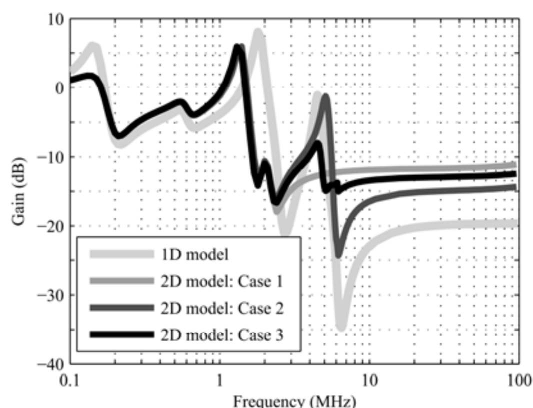


Fig. 11. Computed VTGs from PS1 to PS: 1D model, 2D model: Case 1 - Without decoupling capacitors, Case 2 - Decoupling capacitors at x1 - x2, and Case 3 - Decoupling capacitors at x4 - x5.

the low power plane is observed. First, the VTG is quite different from the 1D lumped model. Clearly, the low power plane has a lower impedance compared to the 1D lumped model, which imposes a higher transfer gain.

This is a major factor for considering a 2D model rather than a 1D model. In addition, this experiment clearly shows how the position of the decoupling capacitors impacts the VTG. Intuitively, including capacitors in x1 and x2 rooms should decrease the VTG since these decoupling capacitors are directly in the current path between PS1 and PS2. At high frequencies, these capacitors bypass an important part of the current. This reduces the collected voltage on PS1, which lowers the VTG. This behavior can be observed over 10MHz, where the VTG is lower for capacitors in x1 and x2 rooms, compared with x4 and x5 rooms. The influence of the low power plane is remarkable between 2.5MHz and 10MHz. Without decoupling capacitors, a purely resistive behavior of the low power plane is observed. However, with decoupling capacitors, two resonances which have a strong impact on the VTG, are observed. For the same capacitor parameters, these resonances appear at different frequencies with different amplitudes, which emphasizes the influence of the low power plane. Of course, this behavior cannot be predicted by using a 1D model. An experimental validation is shown in Fig.10 with a prototype. As observed in the figure, the experimental results closely match the computations in all cases.

D. *VTG with Ferrite Beads*

A ferrite bead and LC filter provide high attenuation on the VTG, which can exceed the precision of measurement devices. This makes it difficult to verify computations by measurement. Since the purposes of this section are to validate the computational model and to study the effect of EMI attenuators, a ferrite bead, i.e. B1, which provides a reasonable attenuation level is chosen to make an analysis without losing generality.

Fig. 12 shows experimental prototypes and the corresponding VTGs of the low power plane with EMI attenuators such as a ferrite bead and the combination of a ferrite bead with 5 film capacitors. There is good agreement between the computation and measurement, which verifies the accuracy of the proposed computational model.

The influence of the ferrite bead on the VTG of the low power plane is analyzed through a comparison between the different EMI attenuating configurations given in Fig. 13. As can be observed, the ferrite bead is effective for attenuating the VTG of 20dB in all of the considered frequency ranges.

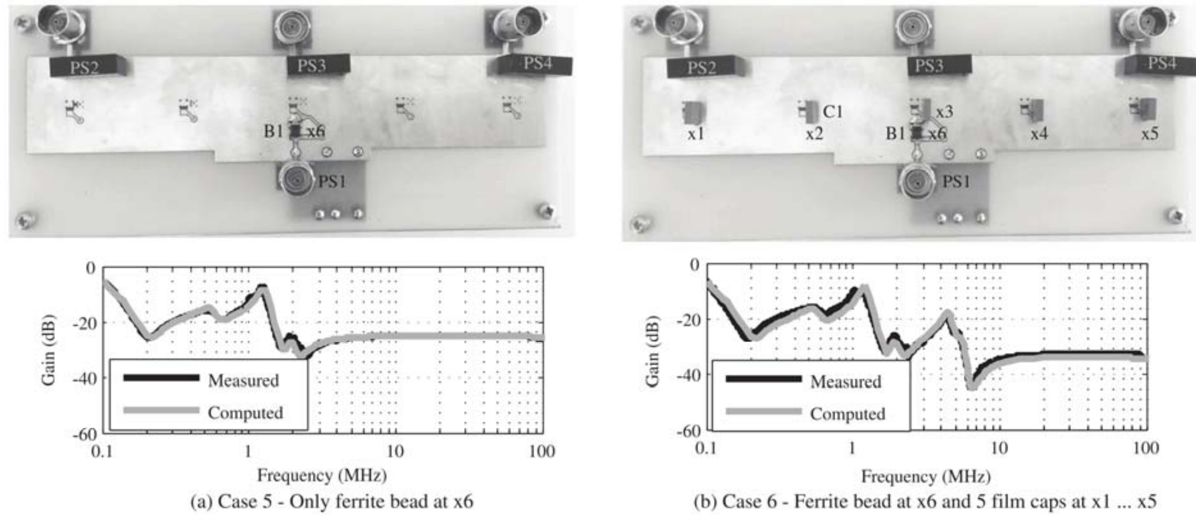


Fig. 12. VTG of low power plane with different combinations of ferrite bead.

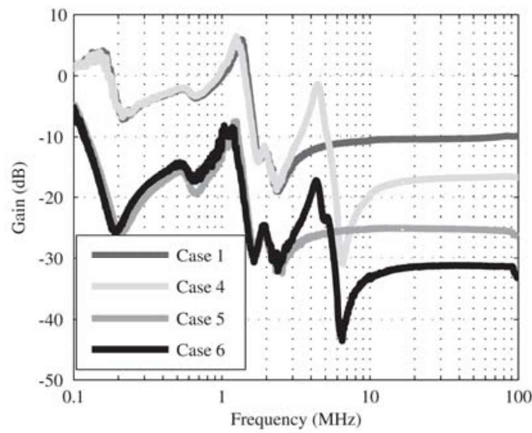


Fig. 13. Experimental results with bead and film capacitor. Case 1 - Without decoupling capacitors, Case 4 - 5 decoupling capacitors at x1 ... x5, Case 5 - Only ferrite bead at x6, and Case 6 - Ferrite bead at x6, 5 decoupling capacitors at x1 ... x5.

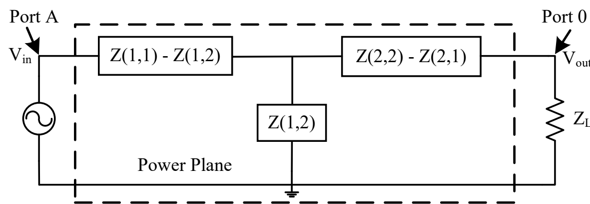


Fig. 14. Equivalent circuit of the low power plane.

This is due to the relationship between the impedance of B1 and PS1 while they are connecting serially. First, the impedance of B1 is 10 times higher than that of PS1. In addition, B1 impedance's phase is positive as is that of PS1. It is experienced that higher is the impedance of the ferrite bead, the higher the attenuation achieved. However, the power density is reduced. On the other hand, the noise attenuating ability of the ferrite bead decreases to below 200kHz since it has opposite impedance phase as PS1.

A combination of the ferrite bead and film decoupling capacitors provides a 6dB higher attenuation than the ferrite bead alone in the frequency range of 5MHz – 100MHz. However, this combination also results in a VTG gain in the frequency range of 2.2MHz – 5MHz due to the negative phase impedance of the film capacitor. The effects of decoupling film capacitors are analyzed in the previous section. The fast computing time which is an advantage of the proposed approach is shown in Table III.

TABLE III
COMPUTING TIME

CPU	Intel(R) Core i7 3.4GHz
RAM	8GB
Number of Cells	1312
Number of sampling frequency	211
Computing time (sec)	121

V. CONCLUSION

In this paper, a modeling strategy for computing the VTG between the port pairs of the low-power plane of power converters with external devices is proposed. Placing the real impedance of external devices into the model as an additional matrix adds flexibility for modifying the external devices, in terms of type, number and location. The precision of the proposed model is verified by experimental results. They also show the effects of the decoupling capacitors to the VTG. According to the impedance of the decoupling capacitors and other devices, both the VTG attenuation and amplification can be observed. The proposed model is well suited for avoiding the impedance mismatch resulting in VTG amplification. Moreover, the proposed approach is flexible and precise for the optimal design of the low-power plane. This point will be considered in a future work.

APPENDIX

The low power plane is a two-port reciprocal network, which can be represented by an equivalent circuit, as shown in Fig. 14. The transfer gain from Port A to Port 0 can be obtained by:

$$VTG_{A,0} = \frac{V_0}{V_A} = \frac{Z_L Z(1,2)}{[Z_L + Z(2,2)]Z(1,1) - [Z(1,2)]^2} \tag{39}$$

where Z_L is the load impedance, which is 50Ω in the experiment; and $Z(1, 1)$, $Z(1, 2)$, $Z(2, 1)$ and $Z(2, 2)$ are elements of the impedance matrix $[Z]$, which is computed as [30].

$$[Z] = ([I]+[S])([I]-[S])^{-1} Z_0 \tag{40}$$

where $[S]$ is the scattering matrix, $[I]$ is the 2 × 2 identity matrix, and Z_0 is the reference impedance.

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REFERENCES

[1] K. Raggl, T. Nussbaumer and J. Kolar, “Guideline for a simplified differential-mode EMI filter design,” *IEEE Trans. Ind. Electron.*, Vol. 57, No. 3, pp. 1031-1040, March 2010.

[2] H. Akagi and T. Shimizu, “Attenuation of conducted EMI emissions from an inverter-driven motor,” *IEEE Trans. Power Electron.*, Vol. 23, No. 1, pp. 282-290, Jan. 2008.

[3] A. J. McDowell and T. H. Hubing, “A compact implementation of parasitic inductance cancellation for shunt capacitor filters on multilayer PCBs,” *IEEE Trans. Electromagn. Compat.*, Vol. 57, No. 2, pp. 257-263, Apr. 2015.

[4] D. Shin , S. Kim, G. Jeong, J. Park, J. Park, K. J. Han, and J. Kim, “Analysis and design guide of active EMI filter in a compact package for reduction of common-mode conducted emissions,” *IEEE Trans. Electromagn. Compat.*, Vol. 57, No. 4, pp. 660-671, 2015.

[5] J. Biela, A. Wirthmueller, R. Waespe, M. L. Heldwein, K. Raggl and J. W. Kolar, “Passive and active hybrid integrated EMI filters,” *IEEE Trans. Power Electron.*, Vol. 24, No. 5, pp. 1340-1349, May 2009.

[6] Y. Maillet, R. Lai, S. Wang, F. Wang, R. Burgos and D. Boroyevich, “High-density EMI filter design for DC-fed motor drives,” *IEEE Trans. Power Electron.*, Vol. 25, No. 5, pp. 1163-1172, May 2010.

[7] J. Espina, J. Balcells, A. Arias, and C. Ortega, “Common mode EMI model for a direct matrix converter,” *IEEE Trans. Ind. Electron.*, Vol. 58, No. 11, pp. 5049-5056, Nov. 2011.

[8] E. Rondon-Pinilla, F. Morel, C. Vollaire, and J. L. Schanen, “Modeling of a buck converter with a SiC JFET to predict EMC conducted emissions,” *IEEE Trans. Power Electron.*, Vol. 29, No. 5, pp. 2246-2260, May 2014.

[9] M. Ferber, C. Vollaire, L. Krähenbühl, J. L. Coulomb and J. A. Vasconcelos, “Conducted EMI of DC–DC converters with parametric uncertainties,” *IEEE Trans. Electromagn. Compat.*, Vol. 55, No. 4, pp. 699-706, Aug. 2013.

[10] L. Zhai, B. Xu, N. Bondarenko, G. Li, T. Makharashvili, D. Loken, P. Berger, T. Van Doren, and D. Beetner, “A measurement – Based model of the electromagnetic emissions from a power inverter,” *IEEE Trans. Power Electron.*, Vol. 30, No. 10, pp. 5522-5531, Oct. 2015.

[11] V. Ardon, J. Aime, O. Chadebec, E. Clavel, J. M. Guichon and E. Vialardi, “EMC modeling of an industrial variable speed drive with an adapted PEEC method,” *IEEE Trans. Magn.*, Vol. 46, No. 8, pp.2892-2898, 2010.

[12] P. Musznicki, M. Turzynski, and P. J. Chrzan, “Accurate modeling of quasi-resonant inverter fed IM drive,” *in Proc. IECON 2013* , pp. 376-381, Nov. 2013.

[13] R. Mrad, F. Morel, G. Pillonnet, C. Vollaire, P. Lombard, and A. Nagari, “N-conductor passive circuit modeling for power converter current prediction and EMI aspect,” *IEEE Trans. Electromagn. Compat.*, Vol. 55, No. 6, pp. 1169-1177, 2013.

[14] H. Wu, J. Zhang, and Y. Xing, “A family of multi-port buck-boost converters based on DC-link-inductors (DLIs),” *IEEE Trans. Power Electron.*, Vol. 30, No. 2, pp. 735-746, Feb. 2015.

[15] M. Hagiwara and H. Akagi, “Control and experiment of pulse width modulated modular multilevel converters,” *IEEE Trans. Power Electron.*, Vol. 24, No. 7, pp. 1737-1746, Jul. 2009.

[16] G. Lei, R. W. Techentin, and B. K. Gilbert, “High-frequency characterization of power/ground-plane structures,” *IEEE Trans. Microw. Theory and Tech.*, Vol. 47, No. 5, pp. 562-569, May 1999.

[17] M. Hampe and S. Dickmann, “Damping of cavity-mode resonances in PCB power-bus structures using discrete capacitors,” *IEEE Trans. Electromagn. Compat.*, Vol. 47, No. 4, pp. 880-888, Nov. 2005.

[18] J. Fan, J. L. Drewniak, J. L. Knighten, N. W. Smith, A. Orlandi, T. P. Van Doren, T. H. Hubing and R. E. DuBroff, “Quantifying SMT decoupling capacitor placement in DC power-bus design for multilayer PCBs,” *IEEE Trans. Electromagn. Compat.*, Vol. 43, No. 4, pp. 588-599, Nov. 2001.

[19] Y. J. Kim, H. S. Yoon, S. Lee, G. Moon, J. Kim, and J. K. Wee, “An efficient path-based equivalent circuit model for design, synthesis, and optimization of power distribution networks in multilayer printed circuit boards,” *IEEE Trans. Adv. Packag.*, Vol. 27, No. 1, pp. 97-106, 2004.

[20] M. Hampe, V. A. Palanisamy, and S. Dickmann, “Single summation expression for the impedance of rectangular PCB power-bus structures loaded with multiple lumped elements,” *IEEE Trans. Electromagn. Compat.*, Vol. 49, No. 1, pp. 58-67, Feb. 2007.

[21] M. Stumpf and M. Leone, “Efficient 2-D integral equation approach for the analysis of power bus structures with arbitrary shape,” *IEEE Trans. Electromagn. Compat.*, Vol. 51, No. 1, pp. 38-45, Feb. 2009.

[22] M. Stumpf, “The time-domain contour integral method – An approach to the analysis of double - plane circuits,” *IEEE Trans. Electromagn. Compat.*, Vol. 56, No. 2, pp. 367-374, Apr. 2014.

[23] L. D. Smith, R. Andersonm and T. Roy, “Power plane SPICE models and simulated performance for materials and geometries,” *IEEE Trans. Adv. Packag.*, Vol. 24, No. 3, pp. 277-287, Aug. 2001.

[24] C. Guo and T. H. Hubing, “Circuit models for power bus structures on printed circuit boards using a hybrid FEM-SPICE method,” *IEEE Trans. Adv. Packag.*, Vol. 29, No. 3, pp. 441-447, Aug. 2006.

[25] C. Bednarz, A. Mantzke, and M. Leone, “Efficient FEM-based modal circuit representation of arbitrarily shaped plate pairs,” *IEEE Trans. Electromagn. Compat.*,

Vol. 56, No. 4, pp. 990-993, 2014.

[26] H. M. Lee, S. Gao, E. X. Liu, G. S. Samudra and E. P. Li, "Two dimensional discontinuous Galerkin time-domain method for modeling of arbitrarily shaped power-ground planes,"*IEEE Trans. Electromagn. Compat.*, Vol. 57, No. 6, pp. 1744-1747, Dec. 2015.

[27] R. Sourajeet, and A. Dounavis, "Macromodeling of multilayered power distribution networks based on multiconductor transmission line approach," *IEEE Trans. Comp. Packag. Manufact. Tech.*, Vol. 3, No. 6, pp. 1047-1056, 2013.

[28] J. -H. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution planes using transmission matrix method," *IEEE Trans. Adv. Packag.*, Vol. 24, No. 3, pp. 334-346, Aug. 2001.

[29] L. Sevgi, "Electromagnetic modeling and simulation: challenges in validation, verification, and calibration," *IEEE Trans. Electromagn. Compat.*, Vol. 56, No. 4, pp. 750-758, Aug. 2014.

[30] D. M. Pozar, *Microwave Engineering*, John Wiley & Sons, 2009.

[31] A. Ales, J. L. Schanen, D. Moussaoui and J. Roudet, "Impedances identification of DC/DC converters for network EMC analysis," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6445-6457, Dec. 2014.

[32] D. Baudry, C. Arcambal, A. Louis, B. Mazari, and P. Eudeline, "Applications of the near-field techniques in EMC investigations," *IEEE Trans. Electromagn. Compat.*, Vol. 49, No. 3, pp. 485-493, 2007.

[33] H. Shall, R. Zouheir Riah, and M. Kadi, "A 3-D near-field modeling approach for electromagnetic interference prediction," *IEEE Trans. Electromagn. Compat.*, Vol. 56, No. 1, pp. 102-112, 2014.

[34] H. W. Ott, *Electromagnetic Compatibility Engineering*, John Wiley & Sons, 2011.

[35] C. Rostamzadeh and B. Archambeault, "Numerical and experimental investigation of PCB ground-fill on radiated EMI," in *Proc. IEEE ISEC*, 2006.

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