

The Role of a Wiring Model in Switching Cell Transients: the PiN Diode Turn-off Case

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Abstract

Power converter design requires simulation accuracy. In addition to the requirement of accurate models of power semiconductor devices, this paper highlights the role of considering a very good description of the converter circuit layout for an accurate simulation of its electrical behavior. This paper considers a simple experimental circuit including one switching cell where a MOSFET transistor controls the diode under test. The turn-off transients of the diode are captured, over which the circuit wiring has a major influence. This paper investigates the necessity for accurate modeling of the experimental test circuit wiring and the MOSFET transistor. It shows that a simple wiring inductance as the circuit wiring representation is insufficient. An adequate model and identification of the model parameters are then discussed. Results are validated through experimental and simulation results.

Key words: Finite element method model, Modeling, PIN diode, Simulation, Wiring parasitic inductances

I. INTRODUCTION

The design of power electronic systems is using more and more computer simulations. Hence, accurate models of power semiconductor devices are required. Very accurate models of power semiconductor devices are based on the finite element method (FEM). These models rely on the technological parameters of power semiconductor devices. In the literature [1]-[5], some identification procedures for the main design parameters of such power semiconductor devices have been developed where good values for these design parameters were extracted and validated. However, a great deal of attention should also be focused on the wiring models of the power converter circuit layouts including the electromagnetic compatibility (EMC) contributions, especially during transients and when operating at elevated switching

frequencies. This paper intends to show that the minimal representation of power converter circuit layout is not sufficient if simulations are required to accurately estimate the power device behaviors during switching transients. An accurate description of the converter circuit layout relies on taking into account the right arrangement and position of devices and the wiring parasitic inductances of the layout and the mutual effects between them.

A switching cell is the simplest circuit representing a converter during switching operation [6]. This paper considers a simple experimental circuit including one switching cell where a MOSFET transistor controls the diode under test.

Accurate modeling for all of the components of a switching cell is required. In addition to the need of an accurate model of the MOSFET transistor, the wiring environment of the experimental circuit has to be taken into consideration for accurate simulations, since it affects the transient electrical behavior of the PIN diode. The modeling for all of the converter components including the wiring elements and magnetic coupling between each of the elements is essential for the accurate modeling of PIN diode turn-off behavior.

Section II describes a theoretical analysis leading to the development of an experimental test circuit for switching PIN

Manuscript received Apr. 11, 2016; accepted Nov. 19, 2016

Recommended for publication by Associate Editor Sang-Won Yoon.

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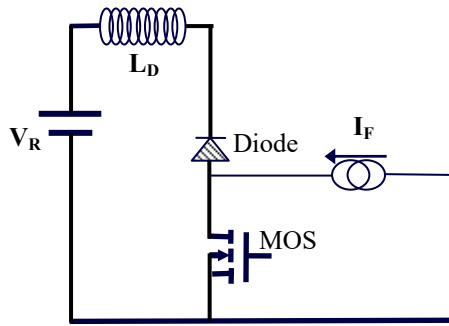


Fig. 1. A switching cell and its simplest environment.

diodes. The measurement techniques are also detailed in this section. Section III presents circuit modeling of the test circuit and it exhibits the necessity for an accurate representation of the circuit layout behavior during switching transients. For the switching cell circuit simulation, an advanced model MOS2KP [7], inspired by the IGBT model developed in [8], is selected instead of the so-called level-3 spice model for power MOSFET transistors. Owing to its very good accuracy, the FEM model is selected to be used as the PIN diode. Section IV describes the necessary model for the test circuit layout to insure simulation accuracy. In this simulation, the mutual-inductance and self-inductance effects are taken into consideration. Current and voltage probe models are also considered. Simulation results concerning the turn-off transients of the PIN diode show good agreements with the experimental results, particularly for high di/dt transients.

II. THEORETICAL AND EXPERIMENTAL ANALYSIS

A PIN-diode turn-off transient may be obtained inside the switching cell shown in Fig. 1. The switching cell circuit includes a diode (as a natural switch), a MOSFET transistor (as a controlled switch), a DC-voltage source, V_R , a DC-current source, I_F , and an inductor, L_D . At the switching time-scale, the inductive load of the converter behaves as a current source, which may be represented by an ideal current source. The behavior of the layout of the switching cell circuit can be represented by the wiring inductance. The turn-off process of the PIN diode is mainly controlled by the MOSFET transistor, the forward current (I_F), the reverse applied voltage (V_R) and the circuit layout behavior. Since the switching cell includes a controlled switch, the characteristics of the driving circuit of the switch are important in terms of switching speed. If the controlled switch turns on too slowly, then it fully controls the diode turn-off. Hence to obtain pertinent diode turn-offs, the controlled switch should be faster than the PIN diode.

A. Test Circuit for the PIN Diode Turn-Off Transient

The experimental test circuit presented in Fig. 2 has been built in the lab. The experimental circuit includes voltage and

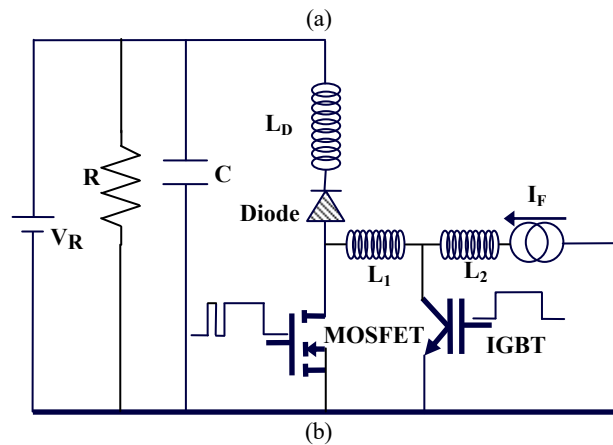
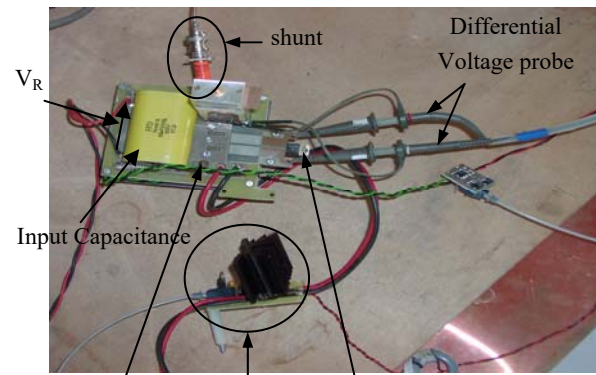


Fig. 2. The experimental circuit for the PIN diode turn-off measurements. (a) Picture. (b) Schematic ($R=10\text{ k}\Omega$, $C=1\text{ }\mu\text{F}$, $L_2=53\text{ mH}$ includes an air-core (3 mH) plus an iron-core (50 mH) inductors. $L_1\sim 1,4\text{ }\mu\text{H}$ is a twist pair).

TABLE I

BASIC ABSOLUTE MAXIMUM RATINGS OF THE CONTROLLED SWITCH AND THEIRS MAIN SWITCHING CHARACTERISTICS (RISE TIME, t_R , TURN-ON TIME, $t_{D(ON)}$, FALL TIME, t_F , OFF VOLTAGE RISE TIME, $t_R(\text{VOFF})$)

Devices	Main Switching Characteristics (Typical) from datasheets				Basic Absolute Maximum Ratings
	t_r	$t_{D(ON)}$	$t_{r(\text{VOFF})}$	t_f	
MOSFET (IRF740)	10 ns	17 ns	10 ns	10 ns	400 V, 10 A

current DC-supplies and a specific driving system, and its time diagrams are defined in Fig. 3. The diode package is inserted at the end of the simplistic bus-bar as shown in Fig. 2(a). A suitable MOSFET transistor (IRF740) is chosen as the controlled switch. An IR4429 IC driver is used with no gate resistance to offer the maximal switching speed of the MOSFET transistor. The basic absolute maximum ratings and the main switching characteristics of the MOSFET transistor are given in Table I

The turn-on delay time of the MOSFET transistor (IRF740) given in table I is much lower than the typical values for the reverse recovery time t_r of PIN diodes under test, as given in

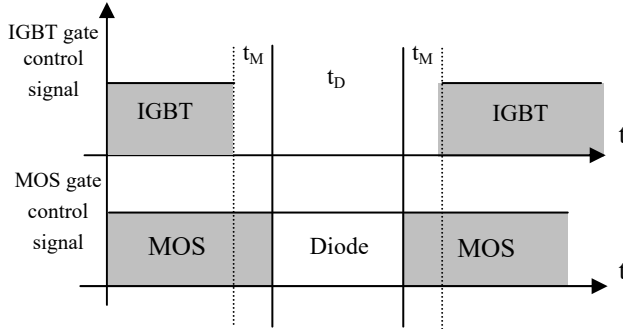


Fig. 3. Graphics-time behavior (when the MOSFET transistor is off, the diode freewheels).

their data-sheets [9]-[12]. This makes it possible to visualize turn-off transient behavior that is appropriate for the selected ultrafast PIN diodes. IGBT transistors (BUP304) are slower but more robust than MOSFET transistors. In addition, they can handle the forward current, I_F , most of the time. An IGBT is turned-off for several tens of microseconds during every hundreds of milliseconds. When the IGBT is off, the switching cell (diode and MOSFET transistor) normally operates for one switching cycle: i.e. the PIN-diode under test operates for one turn-on and one turn-off transient. This test circuit has the ability to avoid self-heating effects in the PIN diode since the device operates with a very low recurrence.

Before the IGBT is turned-off, the MOSFET transistor is turned-on to insure current continuity. A diode turn-on appears. When the MOSFET transistor is off, the PIN diode is in the freewheeling operation mode, which conducts the forward current for a short time interval, t_D (5 to 15 μ s) as shown in Fig. 3. The MOSFET transistor is then turned-on, which operates the required diode turn-off transient.

To stabilize the applied voltage V_R , a polypropylene and ceramic capacitor is added in parallel with the voltage source. Since the voltage source is not reversible in the current, a resistance is added in parallel with the voltage generator V_R to dissipate the average energy returned to the source, which allows proper regulation of the voltage source.

The inductor L_D in Fig. 2 accounts for a physical inductor that enables changing of the diode turn-off transient in terms of the current slope. The inductor value is estimated from measurements. The estimation depends on the circuit layout representation as shown in the next 2 sections. The inductor L_2 is a large and high-frequency inductor that keeps the current unchanged during transients of the switching cell. The inductor L_1 is a small high-frequency inductor that disconnects the IGBT of the switching cell during transients.

B. Current Slope Measurement

The diode current measurements are carried out using a 0.0025 Ω /1.2GHz TMS Research non-inductive shunt in series with the device under test (DUT). The shunt is connected through a cable to a 50 Ω oscilloscope. Since the test circuit produces hard diode turn-off at di/dt larger than 1A/ns, large

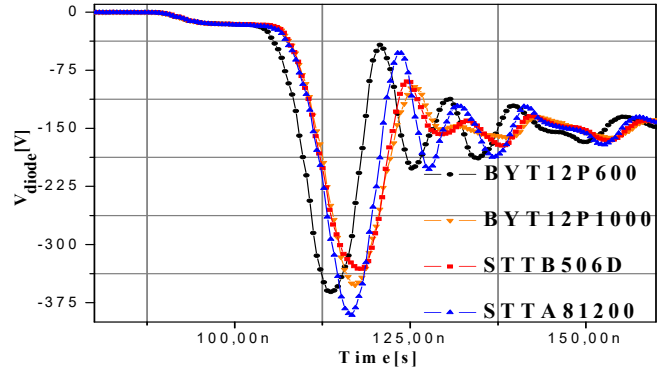
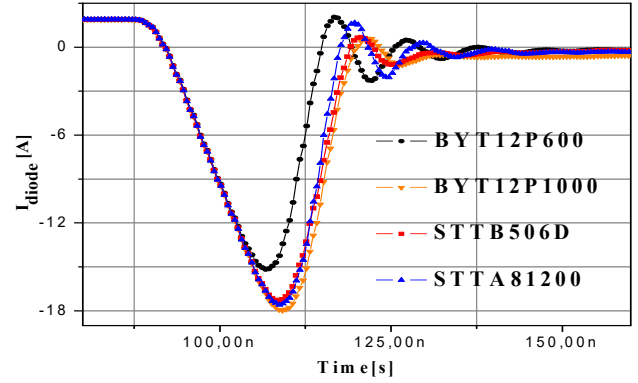


Fig. 4. Experimental turn-off waveforms for several PIN diodes ($V_R=150$ V, $I_F=2$ A, $R=10$ k Ω , $C=1$ μ F, $L_2=53$ mH, $L_1\sim 1,4$ μ H).

frequency bandwidth probes are required. Therefore, to measure the voltage drop across the PIN diode, V_{diode} , two voltage probes (Tektronix P5100 [13]) are connected in a differential manner. One is used to measure the anode voltage and the other is used to measure the cathode voltage of the DUT. All of the signals are measured with reference to the shunt voltage reference.

Experimental voltage and current waveforms for $V_R=150$ V and $I_F=2$ A are presented for several of the ultra-fast PIN diodes under test in Fig. 4.

In textbooks [6], [14] the diode current slope is approximated by $di/dt = -V_R/L_D$ (1) at beginning of reverse recovery. This is done inside a switching cell circuit where the unique wiring parasitic inductance L_D is taken into account.

Since these devices are tested in the same switching cell with the same current, I_F , voltage, V_R , and inductor, L_D , the same value of current slope, di/dt , is measured for these diodes at beginning of their turn-off transient behavior [15].

III. SWITCHING CELL CIRCUIT MODEL

A. Modeling of Switching Cell Circuit Wiring with One Self-Inductor

The accuracy of power converter simulations requires accurate models for the power semiconductor devices and for the experimental circuit layout behavior. This section investigates the accuracy when the circuit layout behavior is

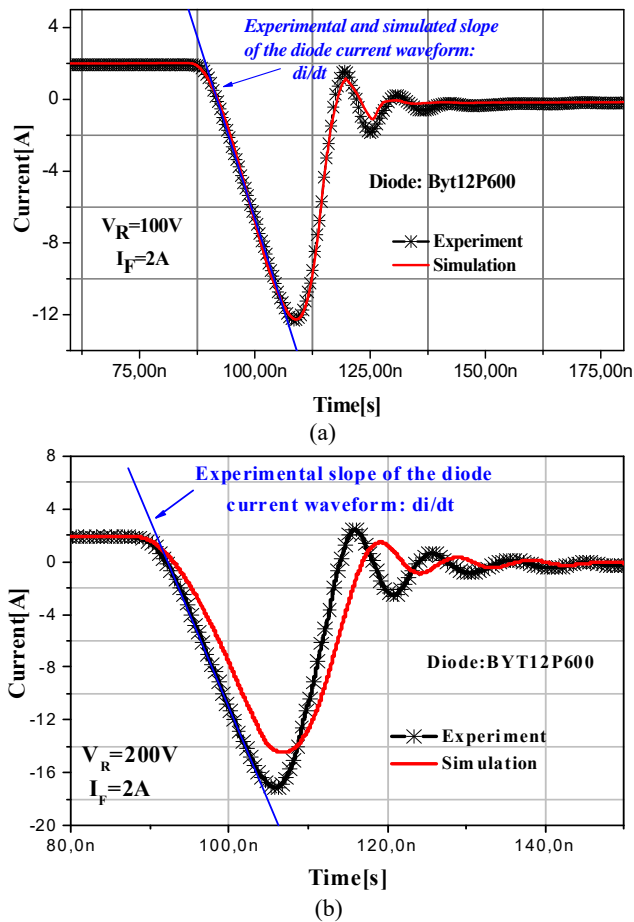


Fig. 5. Experimental and simulated current waveforms through BYT12P600 during its turn-off state (a) ($I_F = 2\text{ A}$, $V_R = 100\text{ V}$). (b) ($I_F = 2\text{ A}$, and $V_R = 200\text{ V}$).

represented only by one self-inductor.

The circuit simulation of experimental circuits is now considered. Because this supports heterogeneous simulations, the experimental switching cell circuit shown in Fig. 2 is implemented in a FEM simulator, DESSIS-ISE TCAD [16]. The IGBT transistor is not taken into account in the simulation since it has no influence on the switching cell behavior due to the high frequency inductor L_1 . The use of a MOSFET transistor (IRF 740) ensures a fast turn-off of the diode, and it should be accurately modeled. An advanced model MOS2KP [7] MOSFET transistor is considered instead of the so-called level-3 spice model. A comparative study between these two models is also highlighted in this section. However, any other analytical model could be considered providing it is accurate enough during transients. All of the components are simulated as equivalent circuit models except the PIN diode. For this semiconductor device, the FEM model is used because a high level of accuracy is required to obtain simulation results across this component that are as close as possible to the experimental results [17]. The values of the doping concentration, N_D , the width W of the low-doped base region, the ambipolar carrier lifetime in the low-doped region, τ , and the effective area, A ,

TABLE II
EXPERIMENTAL AND SIMULATED VALUES OF THE CURRENT SLOPE THROUGH BYT12P600 USING THE CIRCUIT OF FIG. 2(B)

Diode	byt12P600		
	Experimental values of current slope di/dt [A/ μ s]	Simulated values of current slope di/dt [A/ μ s]	Error (%)
$V_R = 100\text{ V}$	-810,1	-810,0	1 %
$V_R = 150\text{ V}$	-1162,6	-1022,2	14 %
$V_R = 200\text{ V}$	-1430,5	-1175,0	21 %

for the BYT12P600, have been accurately estimated and validated in [18]. The BYT12P600 is then used as a reference device in the simulation-based analysis. To evaluate the suitability of the circuit wiring representation with a simple self-inductor, a comparative study between the measured and simulated slopes of the diode current waveform is carried out. Fig. 5(a) presents the measured and simulated current waveforms through the BYT12P600 PIN diode, for an applied voltage of 100 V and a forward current of 2 A.

The value of the inductor L_D is determined by minimizing the difference between the simulated and measured current slope at the beginning of the diode turn-off transient. Hence, the inductor L_D value cumulates the inductance value from the physical inductor and the value of the self-inductance as the representation of the circuit layout behavior.

Using equation (1), the measured current slope in Fig. 5(a), for $V_R = 100\text{ V}$, gives $L_D = 122\text{ nH}$. However, when this value is inserted into a simulation a discrepancy is obtained between the experimental and simulated current slope di/dt . The minimization of the error between the experimental and simulated current slope di/dt given in Fig. 5(a) leads to the value $L_D = 77\text{ nH}$. As expected this is different.

This discrepancy is due to the involvement of the MOSFET transistor in the PIN diode switching. Hence, the drop voltage across the MOSFET transistor, V_{MOSFET} , is not negligible when compared to V_R during the current decay crossing the PIN diode, and it follows that:

$$\frac{di}{dt} = \frac{-V_R + V_{MOSFET}}{L_D} \quad (1)$$

A good agreement is obtained between the simulated and measured current slopes in Fig. 5(a). Obviously, the slope of the current waveform does not depend on the current level I_F . Unfortunately, the good agreement between the experimental and simulation results is no longer valid when the applied voltage V_R is varied without tuning the inductor L_D value, as shown in Table II. Fig. 5(b) presents simulated and experimental waveforms when the applied voltage, V_R is set to 200 V. From this figure, it is clear that a distortion is obtained between the simulated and experimental current waveforms during the turn-off transient behavior of the PIN diode. Therefore, a discrepancy is obtained between the simulated and experimental main switching parameters (I_{RM} , V_{RM} and t_{π}) of

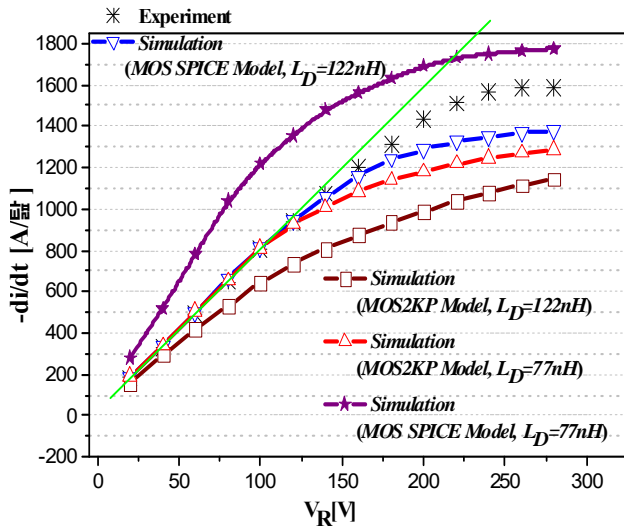


Fig. 6. Simulation and experimental behavior of the current slope di/dt versus V_R using different models of the MOSFET transistor and various values of L_D .

the device and as well a disagreement between the simulated and experimental power switching losses [19].

Using the MOS2KP and the so-called Level-3 Spice model for the MOSFET transistor, a comparative study between the experimental and simulated behavior of the current slope versus V_R is accomplished as shown in Fig. 6. From this figure it is noted that using the MOS2KP model and the extracted value of $L_D = 77$ nH, the agreement between the experimental and simulated current slope is no longer valid when the value of 100 V is reached for V_R . Therefore, the experiment contradicts this assumption with the circuit shown in Fig. 2(b).

This could be explained by the variation of the apparent inductance L_D versus V_R . Using the Level-3 Spice model for the MOSFET transistor instead of the MOS2KP model and an inductor value $L_D = 122$ nH deduced from equation (1) ($V_R = 100$ V) (the case of ultrafast switching of the MOSFET transistor) does not lead to a good agreement between the experimental and simulated behavior of the current slope versus V_R as shown in Fig. 6. It is also noticed that neither using the MOS2KP model for the MOSFET transistor with $L_D = 122$ nH nor the use of the Level-3 spice model for the MOSFET transistor with $L_D = 77$ nH minimizes this disagreement. In fact, the discrepancy was accentuated. Consequently, the circuit layout cannot be represented using only one self-inductor. Mutual-inductance effects explain that depending on the voltage and current levels, the so-called wiring inductance presents a varying value. Accurate analytical models of the MOSFET transistor are necessary but not sufficient for modeling the diode external circuitry with a high-degree of accuracy. The next section details the minimal acceptable representation of the circuit layout behavior that is compatible with the simulation accuracy required in the modeling of the switching cell circuit.

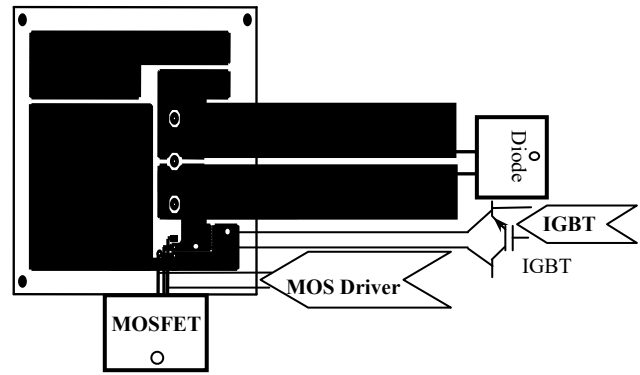


Fig. 7. Test circuit layout as implemented on a printed circuit board.

B. Modeling the Circuit Wiring Behavior with Mutual and Self-Inductors

The latter simulation analysis shows that the circuit layout representation may not be simplified to a simple wiring inductance. In fact, the wiring inductance should be considered in the test circuit simulation as an inductor matrix to take into account the effects of the mutual inductances in addition to the proper inductances. In this paper, the wiring parasitic model of the switching cell circuit is selected to be established using the commercial software INCA [20]. However, other parasitic extraction tools like Q3D [21] may also be used. INCA software is based on the Partial Element Equivalent Circuit (PEEC) method [22] to model printed circuit boards. This is a useful concept in Power Electronics that enables researchers to assign an equivalent electrical circuit to each portion of a conductor. This equivalent circuit is an L-R series circuit where all of the self-inductances are coupled by mutual-inductances. This method has been validated in multiple configurations and for various types of circuit structures [23]-[26]. The wiring modeling process supported by INCA software relies firstly on an accurate description of the geometry of a printed circuit board and the disposition of the power devices on the printed circuit. Secondly, owing to the meshing tool, the printed circuit board structure is discretized in partial parts. The number of the discretized elements depends a lot on the complexity of the printed circuit board geometry. Finally, by applying the PEEC method to the printed circuit board, the values of the self and mutual-inductors are calculated. The test circuit in Fig. 2 is implemented on a printed circuit board (Fig. 7) and using INCA its wiring parasitic model is pictured in Fig. 8.

The device package pin self-inductances and all the conductors between the silicon chip and the voltage probes are also considered in the modeling of the wiring model of a switching cell circuit. Indeed, L_{dio1} , L_{dio2} and L_d account for the inductors of the conductors between the device silicon chip and the voltage probes including the package pin self-inductors. The bonding source inductor L_s responsible of the power/driving interaction represents the conductors

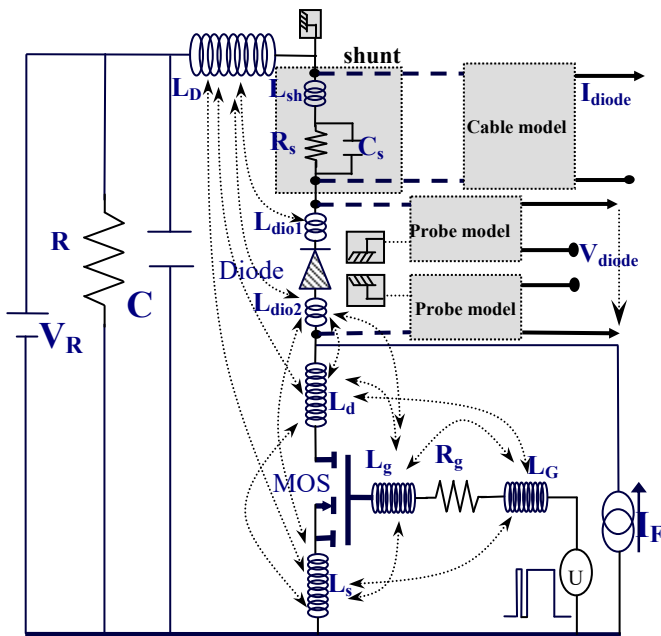


Fig. 8. Model equivalent diagram simulated in DESSIS-ISE TCAD.

TABLE III

INDUCTANCE MATRIX OF THE COMPLETE EQUIVALENT CIRCUIT

[nH]	L_D	L_G	L_g	L_d	L_S	$L_{dio1/2}$
L_D	70	-1,5	0,24	0,94	-1,06	0,093
L_G		20	0,043	-0,67	4,24	0,14
L_g			2	0,53	-3,58	0,27
L_d				14	-8,28	-0,4
L_S					10	0,2
$L_{dio1/2}$						10

between the source side of the MOSFET transistor silicon chip and the negative terminal of the DC-voltage source V_R . Meanwhile, L_g and L_G represent the driving cable inductor of the MOSFET transistor gate and the package pin self-inductor of the MOSFET transistor gate side, respectively. L_D is the inductor of the printed circuit track connected between the positive terminal of the DC-voltage source V_R and the shunt. The values of the self and mutual-inductors identified by INCA are given in Table III.

The values of the inductance matrix are also estimated by matching the experimental and simulated current slope di/dt for various value of V_R giving the same identified values obtained by INCA Software, which confirms its high level of accuracy. Particularly, it appears that the bonding source inductor of the MOSFET transistor suffers from a high mutual inductance and plays a major role in the power/driving interaction.

The equivalent circuit given in Fig. 8 and simulated in DESSIS-ISE TCAD includes a complete wiring model, an advanced power MOSFET transistor model, and current and voltage probe models. The voltage and current probes are taken into account in the switching cell modeling due to their

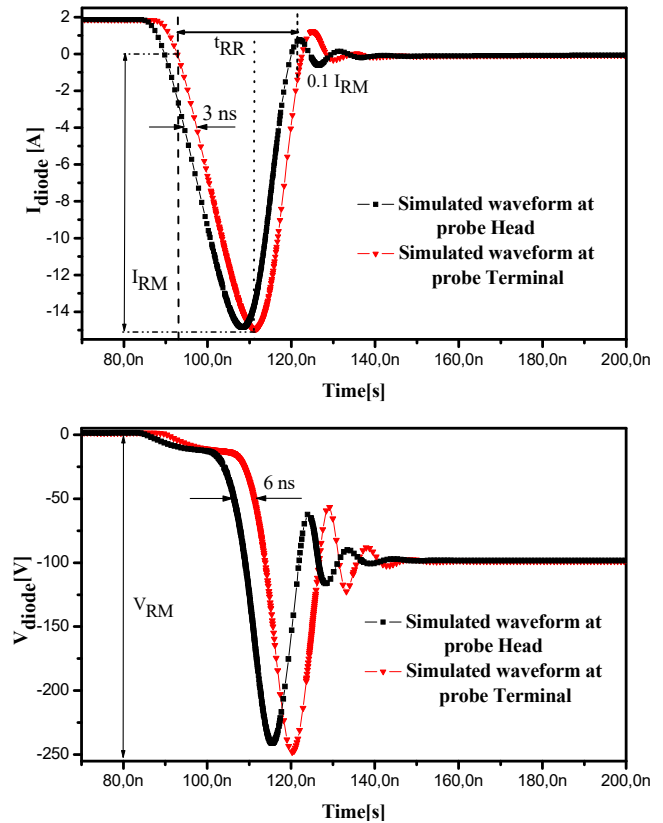


Fig. 9. Transient characteristics of PIN diode turn-off simulated by DESSIS-ISETCAD at probe head and terminal ($V_R=100V$, $I_F=2A$, $A=5\text{ mm}^2$, $W=83\text{ }\mu\text{m}$, $\tau=258\text{ ns}$, $N_D=1,5\cdot 10^{14}\text{ cm}^{-3}$)

alteration effects on the measured signals [27]. The shunt, connected to a $50\text{ }\Omega$ oscilloscope input, is modeled by a pure resistor R_s in parallel with a capacitor C_s , which are in series with a wiring inductor L_{sh} . The models of the voltage probe heads, shunt and cables [27] are used in the simulation of the complete test circuit shown in Fig. 8.

Since the wiring inductor, L_{sh} , has a low value (1pH), its coupling with other circuit components of the circuit is neglected. Simulations of the PIN diode ($A=5\text{ mm}^2$, $W=83\text{ }\mu\text{m}$, $\tau=258\text{ ns}$, $N_D=1,5\cdot 10^{14}\text{ cm}^{-3}$) transient characteristics before and after the probe models are pictured in Fig. 9.

The probe head is connected to the signal to be measured. The probe terminal is connected to a display device such as an oscilloscope. Fig. 9 shows that the voltage probes introduce overshoots and delays in the fast transient waveforms. In fact, a phase delay of about 3ns between the transient current and voltage waveforms simulated before and after the probes is detected. Therefore, the simulated waveforms at the probe terminals are selected to be compared with the experimental current and voltage waveforms across the PIN diode during diode turn-offs. Obviously, comparing simulation results prior to the probe models with experimental results would introduce an error in the estimated switching power losses.

TABLE IV

EXPERIMENTAL AND SIMULATED VALUES OF THE CURRENT SLOPE FOR BYT12P600 PIN DIODE USING THE COMPLETE EQUIVALENT CIRCUIT FOR SIMULATION

Diode	BYT12P600		
	Experimental values of current slope di/dt [A/ μ s]	Simulated values of current slope di/dt [A/ μ s]	Error (%)
$V_R = 100V$	-810,1	-812,0	0,2 %
$V_R = 150V$	-1162,6	-1162,8	0,02 %
$V_R = 200V$	-1430,5	-1432,2	0,1 %

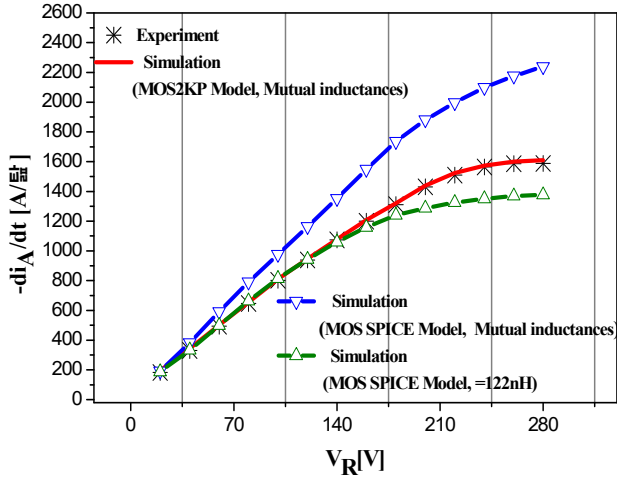


Fig. 10. Simulation and experimental behavior of the current slope di/dt as a function of V_R using different models for the MOSFET transistor and the taking into account the effect of mutual inductances.

IV. EXPERIMENT AND SIMULATION RESULTS

The validity of the developed wiring model of the switching cell circuit and the choice of the MOS2KP model for the MOSFET transistor is examined by comparative studies firstly between the experimental and simulated values of the current slope, di/dt , and then between the experimental and simulated current and voltage waveforms during the turn-off transient behavior for various PIN diodes under test and operating under various conditions. Table IV gives the measured and simulated current slopes as obtained for the PIN diode BYT12P600 for various values of V_R .

It can be seen that the maximum error between experiment and simulation using the inductance matrix for the wiring parasitic model of the switching cell circuit falls below 0.2 % instead of the 21% obtained when only one self-inductor is considered. The FEM models for the diodes under tests are implemented in a DESSIS-ISE TCAD simulator, including the well extracted values of the doping concentration N_D , the width W and ambipolar carrier lifetime, τ , of the low-doped base region, and the effective area A for the devices BYT12P600, BYT12P1000, STTB506D and STTA81200 [18]. Using the MOS2KP model for the MOSFET transistor

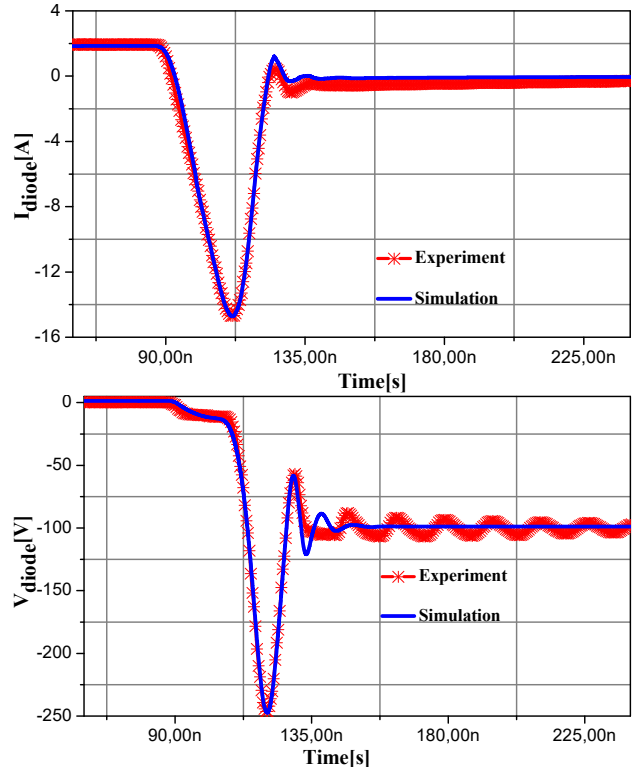


Fig. 11. Experimental and simulated current and voltage waveforms through BYT12P600 during its turn-off transient for $I_F = 2$ A, $V_R = 100$ V.

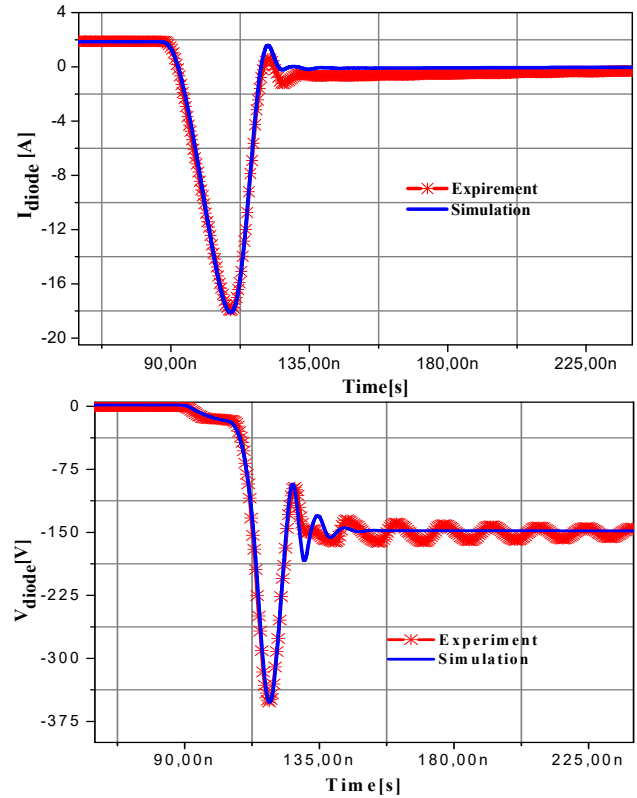


Fig. 12. Experimental and simulated current and voltage waveforms through BYT12P600 during its turn-off state for $I_F = 2$ A, $V_R = 150$ V.

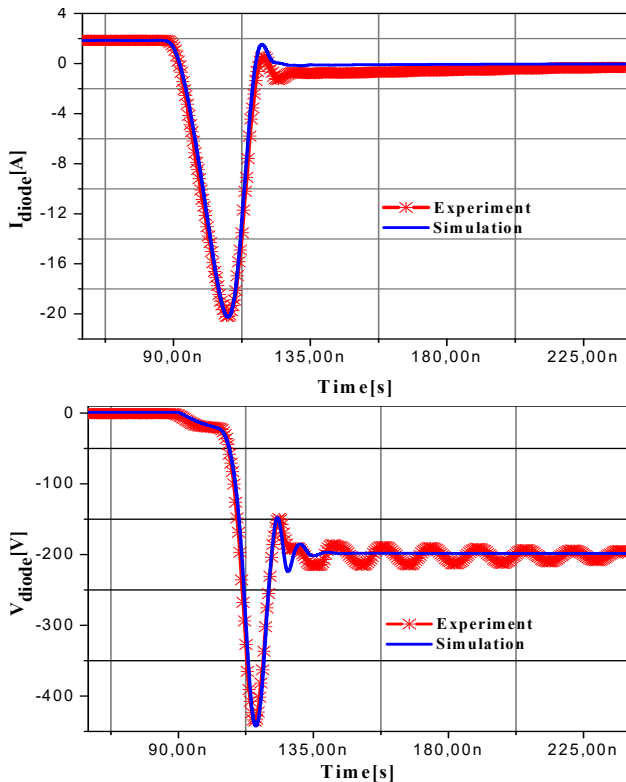


Fig. 13. Experimental and simulated current and voltage waveforms through BYT12P600 during its turn-off state for $I_F = 2$ A, $V_R = 200$ V.

and the identified inductance matrix given in Table III, an excellent agreement is found between the experimental and simulated behavior of the current slope as a function of V_R as pictured in Fig. 10.

From Fig. 10, it can be seen that neither the substitution of the MOS2KP model by the so-called Level-3 Spice model for the MOSFET transistor nor the use of an inductor matrix while keeping the Level-3 Spice model for the MOSFET transistor for the simulation of the switching cell circuit lead to satisfactory results.

To further validate the wiring model developed for the switching cell circuit, as well the choice of the MOS2KP model for the MOSFET transistor, a comparative study between the measured and simulated current and voltage waveforms across the panel of the DUT for various value of V_R is carried out. A very good agreement is obtained between them and even the main switching parameters V_{RM} , I_{RM} and t_{tr} are exactly the same for the experiments and simulations. Thus, the simulated and experimental power switching losses are practically identical. To avoid redundancy, only Figs. 11, 12 and 13 are used to represent a comparison between the experimental and simulated results for the PIN diode BYT12P1000.

V. CONCLUSIONS

It has been demonstrated that the minimal representation of a switching cell circuit layout is not sufficient to accurately

simulate power device behaviors during switching transients. Indeed, considering only one self-inductor for the wiring parasitic model of a printed circuit board of a switching cell circuit including a PIN diode controlled by a MOSFET transistor leads to a discrepancy between the experimental and simulated PIN diode current slope versus V_R during hard turn-off. It has also been verified that when using an advanced analytical model MOS2KP for the MOSFET transistor instead of the level-3 spice model, the disagreement between the experimental and simulation results still exists. Then, the wiring parasitic model of the switching cell circuit is performed using the parasitic extraction tool INCA. Thus, the corresponding inductance matrix taking into account the various wiring parasitic inductances of the circuit layout and the mutual effects between them is generated. Finally, using the advanced MOS2KP model for the MOSFET transistor along with the current and voltage probe models, the inductance matrix is validated by the excellent agreement between the experiment and simulation results for the different operating conditions of the switching cell circuit. This study is useful for designers that are worried about losses since it has been demonstrated that in addition to the necessity for accurate models of power semiconductor devices, the development of accurate wiring parasitic models of designed power converters is an essential task to predict transient electrical behavior via simulations that is as close as possible to that of experimental studies. This is especially true for converters operating at a high switching frequency.

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