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A Ripple-free Input Current Interleaved Converter with Dual Coupled Inductors for High Step-up Applications

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Abstract

This paper presents a ripple-free input current modified interleaved boost converter for high step-up applications. By integrating dual coupled inductors and voltage multiplier techniques, the proposed converter can reach a high step-up gain without an extremely high turn-ON period. In addition, a very small auxiliary inductor employed in series to the input dc source makes the input current ripple theoretically decreased to zero, which simplifies the design of the electromagnetic interference (EMI) filter. In addition, the voltage stresses on the semiconductor devices of the proposed converter are efficiently reduced, which makes high performance MOSFETs with low voltage rated and low resistance r_{DS}(ON) available to reduce the cost and conduction loss. The operating principles and steady-state analyses of the proposed converter are introduced in detail. Finally, a prototype circuit rated at 400W with a 42-50V input voltage and a 400V output voltage is built and tested to verify the effectiveness of theoretical analysis. Experimental results show that an efficiency of 95.3% can be achieved.

Key words: Dual coupled inductors, High step-up, Modified interleaved boost converter, Ripple-free input current

I. INTRODUCTION

Recently, photovoltaic and fuel cells have become increasingly important and widely used in distribution power generation systems in order to alleviate the problems of environmental pollution and depletion of fossil energy reserves [1]-[7]. However, the main characteristic of these energies is a low-output voltage. Hence, a DC–DC converter with a large voltage conversion ratio, to boost low voltage (15-50V) to high voltage (380-400V), is required as an interface to the main electricity source through a DC–AC inverter. Although some single switch boost converters with a high voltage gain have been proposed [8]-[13], these single switch topologies suffer from large input currents and current ripples for high power applications. Moreover, for renewable energy source applications, a large input pulsating current reduces their lifetime and even damage the power generation equipment.

The interleaved boost structure is a solution for high power conversion and low input current ripple applications [14], [15]. However, the voltage gain of the conventional interleaved boost converter is only determined by the duty ratio. In practical application, the voltage gain is limited to five times due to the influence of the parasitic parameters of the power devices, inductors and capacitors. In addition, the voltage stresses on the power devices are still equal to the high output voltage, and an extreme duty ratio will result in a serious reverse recovery problem of the output diodes [16]. Authors have proposed several high step-up interleaved boost converters by inserting switched capacitor cells into conventional interleaved boost converters [17]-[19]. However, massive switched capacitor cells are required to reach a very high voltage gain, which increases the circuit complexity. In addition, several high step-up interleaved boost converters with coupled inductors were introduced in [20], [21]. However, the voltage step-up capability is ordinary. In [22]-[26], some interleaved boost converters combined coupled inductors with switched capacitors for high step up and high power applications.

This paper presents a modified interleaved boost converter integrating dual coupled inductors and voltage multiplier techniques for a high step-up gain. The proposed converter inherits the merit of a ripple-free input current, which greatly

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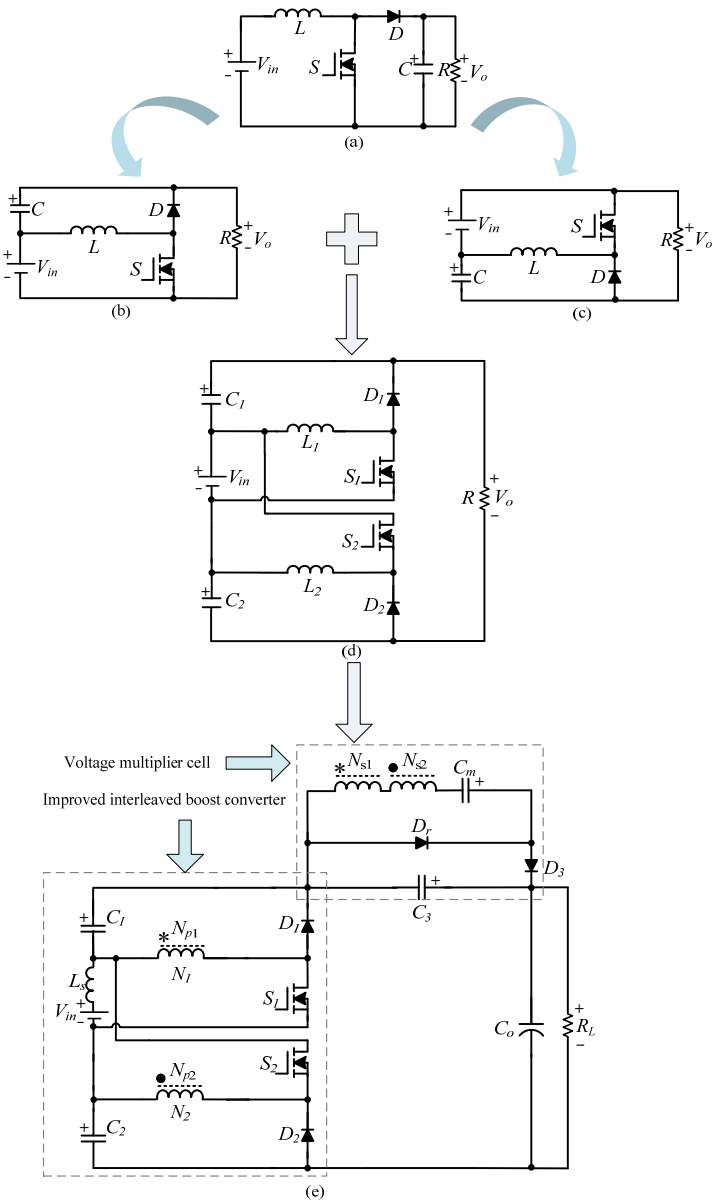


Fig. 1. Deduction process for the proposed topology. (a) Conventional boost converter. (b) Other boost converter structure. (c) Other boost converter structure. (d) Modified interleaved boost converter. (e) The proposed converter.

suppress electromagnetic interference problem. At the same time, the low voltages stress across the power switches is conducive to improving the efficiency of power conversion.

II. Operational Principle of the Proposed Converter

The deduction process for the proposed converter topology is shown in Fig. 1. It can be seen that this converter consists of two parts: a modified interleaved boost converter in the left dotted box and a voltage multiplier cell in the right dotted box. The conventional boost converter is shown in Fig. 1(a). Fig. 1(b) and (c) show other boost converter versions, whose output voltages are stacked by the capacitor C and the dc-source V_{in}, and the voltage gains are equal to that of the conventional boost converter. Fig. 1(d) is the modified interleaved boost converter, which is achieved by the integration of the converters in Fig.1 (b) and (c). Then, the two inductors L_1 and L_2 in the modified interleaved boost converter are separately substituted by the primary windings of the coupled inductors N_{p1} and N_{p2}, which are adopted as energy storage and filter inductors. In addition, the secondary windings of the two coupled inductors N_{s1} and N_{s2} are connected in series for a voltage multiplier cell to obtain a high voltage gain, as shown in Fig. 1(e).

The coupled inductor can be modeled as a magnetizing inductor, a leakage inductance in series with the magnetizing inductor and an ideal transformer with a corresponding turns ratio. The coupling references of the coupled inductors are indicated by the marks "*" and "·". Fig. 2 shows an equivalent

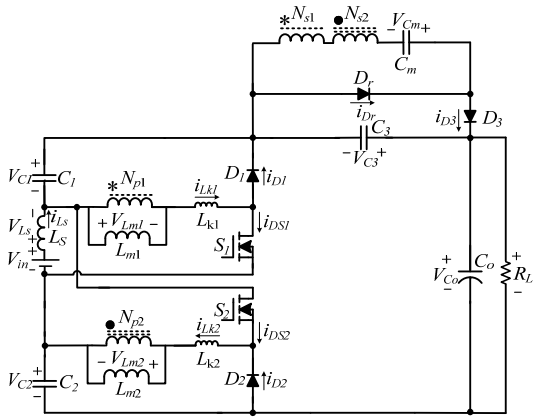


Fig. 2. Equivalent circuit of the proposed converter.

circuit of the proposed converter, in which:

1) L_{m1}, L_{m2}: magnetizing inductors
2) L_{k1}, L_{k2}: leakage inductances
3) L_S: a very small auxiliary inductor
4) C_1, C_2, C_3: intermediate storage capacitors
5) C_O: an output capacitor
6) S_1, S_2: power switches
7) D_1, D_2: clamp diodes
8) D_r, C_m: a regenerative diode and a capacitor
9) D_3: an output diode
10) N: the turns ratio of N_s/N_p

It is worth pointing out that the duty ratios of the power switches during steady operation are interleaved with a 180° phase shift and higher than 0.5. The voltage step-up capability is ordinary when the proposed converter is operating at a duty ratio less than 0.5. Thus, the steady state analysis is made only for this condition. To simplify the analysis, the very small auxiliary inductor is not considered. The key theoretical waveforms of the proposed converter are plotted in Fig. 3. Considering the effect of the leakage inductance, there are eight stages in one switching period, and the corresponding equivalent circuits for each operational stage are depicted in Fig. 4.

Stage I [t_0-t_1]: At t=t_0, S_1 begins to turn on, while S_2 remains conducting. Diodes D_1, D_2 and D_r are turned off, while diode D_3 is turned on. The current-flow path is shown in Fig. 4(a). The capacitor C_m is discharging its energy to the capacitor C_3 and the load R_L through the output diode D_3. The current falling rate through the diode D_3 is restrained by the leakage inductances L_{k1} and L_{k2}. Therefore, the reverse recovery problem of the diode D_3 is effectively alleviated. When the current through the diode D_3 becomes zero at t=t_1, D_3 switches off and this mode ends.

$$i_{D3}(t) = i_{D3}(t_0) - \frac{V_{C3} - V_{Cm}}{N^2(L_{k1} + L_{k2})}(t - t_0) \qquad (1)$$

Stage II [t_1-t_2]: In this mode, S_1 and S_2 remain conducting, and all of the diodes D_1, D_2, D_3 and D_r are turned off. The

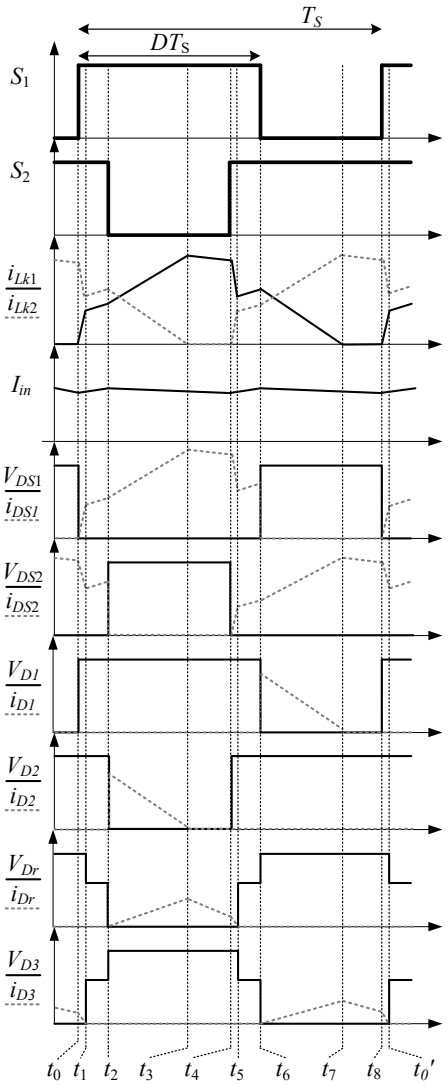


Fig. 3. Key theoretical waveforms of the proposed converter.

current-flow path is shown in Fig. 4(b). The magnetizing inductors L_{m1}, L_{m2} and the leakage inductances L_{k1}, L_{k2} are charged linearly by the dc power source V_{in}. There is no current flowing through the primary or secondary windings. This operating mode ends at t=t_2 when S_2 is turned off.

$$i_{Lk1}(t) \approx i_{Lk1}(t_1) + \frac{V_{in}}{(L_{m1} + L_{k1})}(t - t_1) \qquad (2)$$

$$i_{Lk2}(t) \approx i_{Lk2}(t_1) + \frac{V_{in}}{(L_{m2} + L_{k2})}(t - t_1) \qquad (3)$$

Stage III [t_2-t_3]: During this time interval, S_1 remains conducting, while S_2 is turned off. The diodes D_2 and D_r are turned on, while the diodes D_1 and D_3 are turned off. Fig. 4(c) depicts the current-flow path of this mode. The currents i_{Lk2} and i_{Lm2} decrease linearly, and the energy stored in the leakage inductance L_{k2} and the magnetizing inductor L_{m2} are released to the capacitor C_2 through D_2. Thus, the voltage across the switch S_2 is clamped at V_{in}+V_{C2}. In addition, a part

of the energy stored in the magnetizing inductor L_{m2} is transferred to the secondary side, which charges the capacitor C_m via D_r. When the current i_{Lk2} drops to zero at $t=t_3$, this mode is ends.

$$i_{Lk1}(t) \approx i_{Lk1}(t_2) + \frac{V_{in}}{(L_{m1}+L_{k1})}(t-t_2) \quad (4)$$

$$i_{Lk2}(t) \approx i_{Lk2}(t_2) - \frac{V_{C2}}{(L_{m2}+L_{k2})}(t-t_2) \quad (5)$$

Stage IV [t_3-t_4]: During this time interval, S_1 remains conducting and S_2 is still turned off. Diode D_r is turned on, D_1 and D_3 are turned off, while D_2 turns off naturally since the energy stored in the leakage inductance L_{k2} has been released completely to the capacitor C_2. Fig. 4(d) illustrates the current-flow path of this mode. The energy of the magnetizing inductor L_{m2} is transferred to the secondary side to continuously charge the capacitor C_m. This mode ends when S_2 begins to turn on at $t=t_4$.

$$i_{Dr}(t) = i_{Dr}(t_3) - \frac{V_{Cm}}{N^2(L_{k1}+L_{k2})}(t-t_3) \quad (6)$$

Stage V [t_4-t_5]: During this transition interval, S_1 remains conducting, while S_2 is turned on. Only diode D_r is turned on, while D_1, D_2 and D_3 are turned off. Fig. 4(e) depicts the current-flow path of this mode. The current through the diode D_r decreases linearly. The current falling rate through the diode D_r is limited due to the leakage inductances L_{k1} and L_{k2}. This mode ends when the current through the diode D_r becomes zero at $t=t_5$.

$$i_{Dr}(t) = i_{Dr}(t_4) - \frac{V_{Cm}}{N^2(L_{k1}+L_{k2})}(t-t_4) \quad (7)$$

Stage VI [t_5-t_6]: In this mode, both S_1 and S_2 are still turned on. All of the diodes D_1, D_2, D_3 and D_r are in the turn-off state. The operating mode of this stage is the same as that of Stage Ⅱ. The current-flow path is shown in Fig. 4(f). This mode ends when S_1 is turned off at $t=t_6$.

Stage VII [t_6-t_7]: At t_6, S_1 is turned off, while S_2 is still turned on. Diodes D_1 and D_3 are turned on, while D_2 and D_r are turned off. The current-flow path is shown in Fig. 4(f). The energy stored in the leakage inductance L_{k1} and the magnetizing inductor L_{m1} are released to the capacitor C_1 through the diode D_1. Thus, the voltage across the switch S_1 is clamped at $V_{in}+V_{C1}$. Meanwhile, the secondary windings of the coupled inductors are series connected with the capacitor C_m to charge the capacitor C_O and to provide energy to the load R_L. This mode ends when the current through the leakage inductance L_{k1} decreases to zero at $t=t_7$.

$$i_{D3}(t) = i_{D3}(t_6) + \frac{V_{C3}-V_{Cm}}{N^2(L_{k1}+L_{k2})}(t-t_6) \quad (8)$$

Stage VIII [t_7-t_8]: During this transition interval, S_1 is turned off, while S_2 remains conducting. The diodes D_1 and D_3 are turned on, while D_2 and D_r are turned off. The current-flow path of this mode is shown in Fig. 4(g). The energy stored in the leakage inductance L_{k1} has been completely released to the capacitor C_1, while the magnetizing inductor L_{m1} continuously delivers energy to the output via the secondary side of the coupled inductor N_1. This mode is ends when S_1 is turned onagain at $t=t_8$.

$$i_{D3}(t) = i_{D3}(t_7) - \frac{V_{C3}-V_{Cm}}{N^2(L_{k1}+L_{k2})}(t-t_7) \quad (9)$$

III. Steady-state Performance Analysis of the Proposed Converter

To simplify the circuit analysis, the following assumptions have been taken into account:

(1) The active switches and diodes are ideal, and the equivalent series resistances (ESR) of all the components including the inductor and capacitor are ignored.

(2) Capacitor C_1, C_2, C_3, C_m, and C_O are large enough. Thus, the voltages across them can be considered to be constant in one switching cycle.

(3) The coupling-coefficient of the coupled inductor k is equal to $L_m/(L_m+L_k)$ and the turns ratio of the coupled inductor N is equal to N_s/N_p.

(4) The parameters of two coupled inductors are completely symmetrical, that is to say, $L_{m1}=L_{m2}=L_m$, $L_{k1}=L_{k2}=L_k$, $N_{s1}/N_{p1}=N_{s2}/N_{p2}=N$,$k_1=L_{m1}/(L_{m1}+L_{k1})=k_2=L_{m2}/(L_{m2}+L_{k2})=k$.

A. Voltage Gain Express

To simplify the analysis, the very small auxiliary inductor L_S is not considered, and only stages Ⅱ, Ⅲ and Ⅶ are taken into consideration for the *CCM* operation. According to the topology structure, the output voltage can be expressed as:

$$V_O = V_{in} + V_{C1} + V_{C2} + V_{C3} \quad (10)$$

The following equations can be obtained from Fig. 4 (b) and (c):

$$V_{Lm1}^{\mathrm{II}} = V_{Lm2}^{\mathrm{II}} = kV_{in} \quad (11)$$

$$V_{Lm1}^{\mathrm{III}} = kV_{in} \quad (12)$$

$$V_{Lm2}^{\mathrm{III}} = -kV_{C2} \quad (13)$$

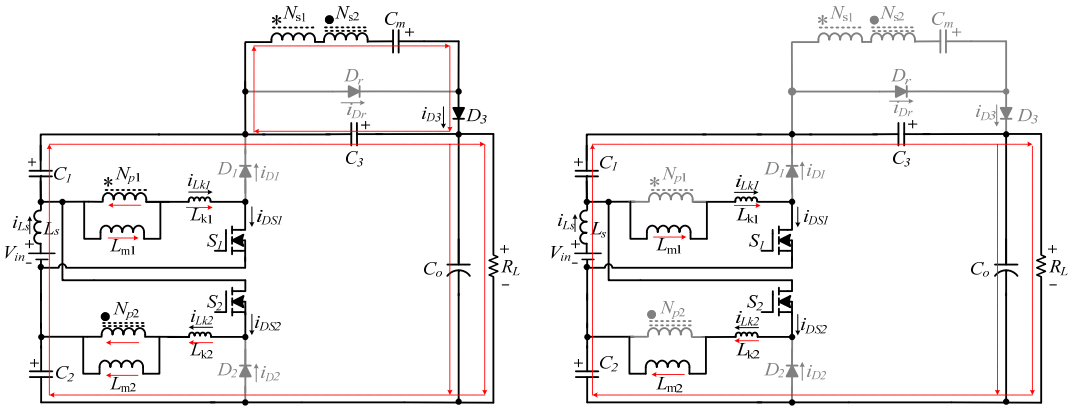
$$V_{Cm} = NkV_{in} + NkV_{C2} \quad (14)$$

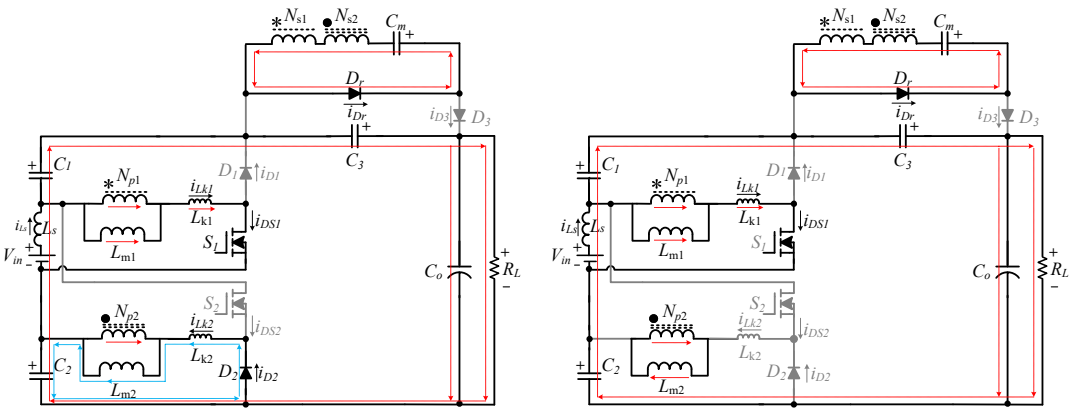
During Stage VII, the following equations can be obtained based on Fig. 4 (g):

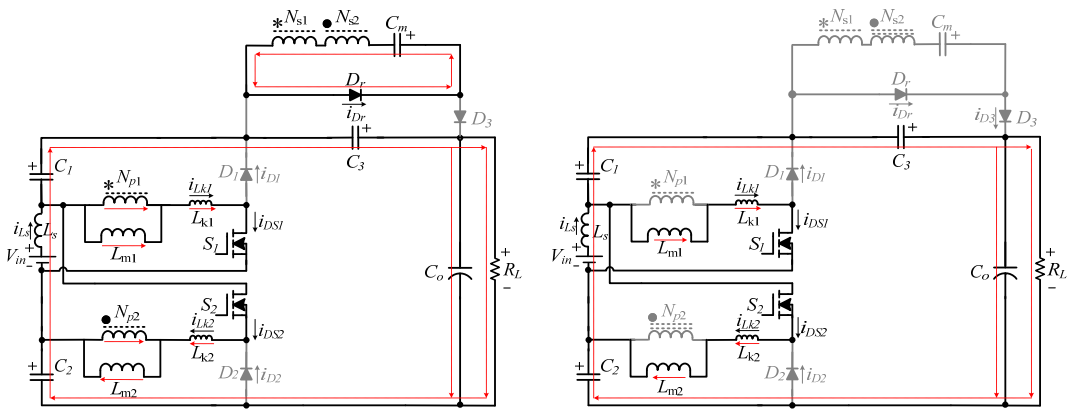
$$V_{Lm1}^{\mathrm{VII}} = -kV_{C1} \quad (15)$$

$$V_{C3} = 2NkV_{in} + NkV_{C1} + NkV_{C2} \quad (16)$$

Applying the volt-second balance principle on the magnetizing inductors L_{m1} and L_{m2} yields:







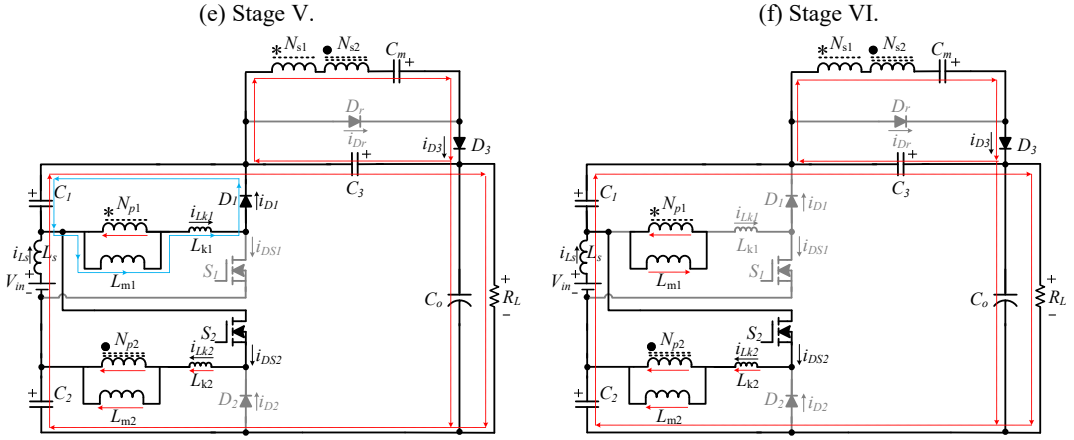


Fig. 4. Operating modes of the proposed converter.

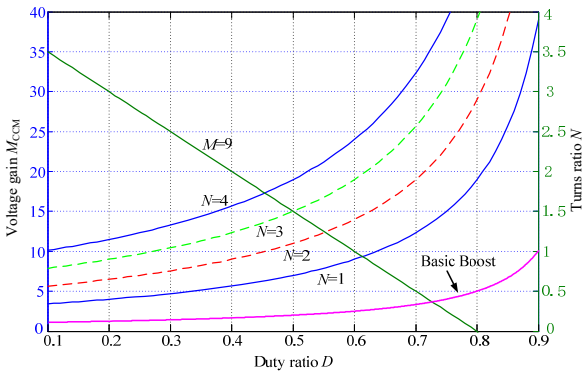


Fig. 5. Voltage gain M_{CCM} as a function of the duty ratio D with various turns ratios, the turns ratios versus the duty ratio under a voltage conversion of 9, and the basic boost converter gain curve.

$$\int_0^{DT_S} kV_{in}dt + \int_{DT_S}^{T_S} (-kV_{C1})dt = 0 \quad (17)$$

$$\int_0^{DT_S} kV_{in}dt + \int_{DT_S}^{T_S} (-kV_{C2})dt = 0 \quad (18)$$

The voltages across the capacitor C_1 and C_2 are derived as:

$$V_{C1} = V_{C2} = \frac{D}{1-D}V_{in} \quad (19)$$

Substituting (16) and (19) into (10), the output voltage can be derived by:

$$V_O = V_{in} + V_{C1} + V_{C2} + V_{C3} = \frac{1+D+2Nk}{1-D}V_{in} \quad (20)$$

Thus, the voltage gain M_{CCM} can be expressed as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{1+D+2Nk}{1-D} \quad (21)$$

The characteristic curve of the voltage gain M_{CCM} as a function of the duty ratio D by various turns ratios, the plot of the turns ratio N versus the duty ratio under a voltage gain of M_{CCM} = 9, and the gain curve of the basic boost converter are shown in Fig. 5.

Fig. 6 shows the voltage gain M_{CCM} versus the duty ratio under different coupling coefficients and turns ratios of the coupled inductor. It indicates that the coupling coefficient k has a minimal impact on the voltage gain, especially with a turns ratio of N=1. Thus, if the influence of the leakage inductances is ignored, namely k=1, the ideal voltage gain can be derived by:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{1+D+2N}{1-D} \quad (22)$$

B. Ripple-free Current Ripple Performance Analysis

It can be seen from Fig. 4 that in one switching period the dc source V_{in}, the auxiliary inductor L_S, the intermediate storage capacitors C_1, C_2 and C_3, and the output capacitor C_O constitute a voltage loop. Therefore, the voltage across the

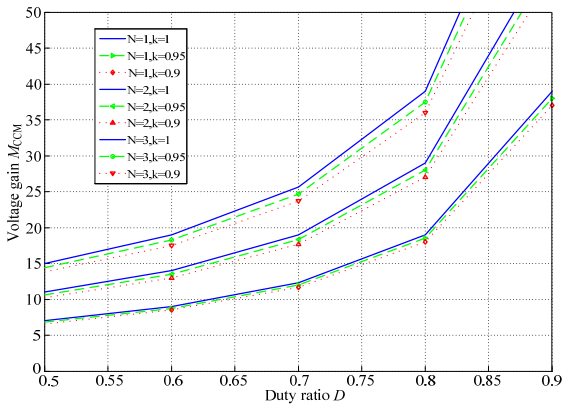


Fig. 6. Voltage gain versus the duty ratio under different turns ratios and coupling coefficients.

auxiliary inductor L_S can be expressed as:

$$V_{L_S} = L_S \frac{di_{L_S}(t)}{dt} = V_{in} + V_{C1} + V_{C2} + V_{C3} - V_{CO} \quad (23)$$

Since the capacitors C_1, C_2, C_3 and C_O are assumed to be large enough, their voltage ripples can be neglected and the voltages across them can be considered to be approximately constant in one switching period. As a result, there is an extremely small voltage drop across the auxiliary inductor L_S. Therefore, the voltage V_{LS} can be considered as a constant of zero.

According to V_{LS}/L_S=di_{LS}/dt=0, the auxiliary inductor current i_{LS} remains constant during one switching period. Thus, the ripple-free input current characteristic of the proposed converter can be achieved. It can be concluded that the realization of ripple-free input current is not dependent on other circuit parameters such as the duty ratio and turns ratio, and that only a very small auxiliary inductor L_S is needed, without increasing the control complexity of the circuit.

C. Voltage Stress Analysis

On the basis of the steady operating principle, the voltage stresses on the power components of the proposed converter are formulated as follows. In order to simplify the voltage stress analysis, the leakage inductances of the coupled inductors and the voltage ripples on the capacitors are neglected. The voltage stresses on the switches S_1 and S_2 can be derived by:

$$V_{DS1} = V_{DS2} = \frac{1}{1-D}V_{in} = \frac{V_O}{1+D+2N} \quad (24)$$

The voltage stresses of the diodes D_1, D_2, D_3 and D_r are expressed as:

$$V_{D1} = V_{D2} = \frac{1}{1-D}V_{in} = \frac{V_O}{1+D+2N} \quad (25)$$

$$V_{D3} = V_{Dr} = \frac{2N}{1-D}V_{in} = \frac{2NV_O}{1+D+2N} \quad (26)$$

Fig. 7 shows the relationship between the normalized

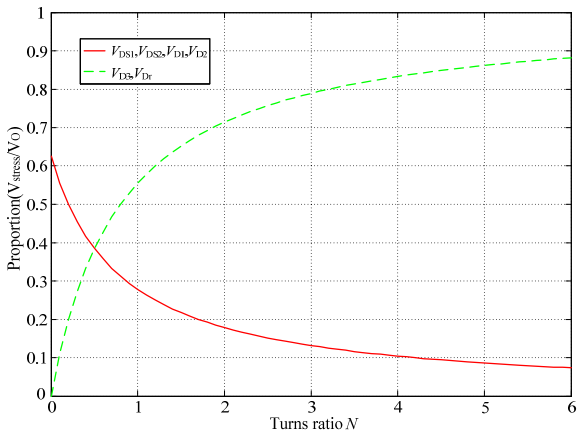


Fig. 7. Relationship between the normalized voltage stresses and turns ratios under D=0.6.

TABLE I
PERFORMANCE COMPARISON OF SIMILAR PROTOTYPES

Similar prototypes	Converter[25]	Converter[26]	The proposed converter
Number of switches	2	2	2
Number of diodes	4	4	4
Number of cores	2	2	2
Number of secondary side windings	1	1	1
Voltage gain	$\frac{2}{1-D}+ND$	$\frac{2N+1}{1-D}$	$\frac{1+D+2N}{1-D}$
Voltage stress on the active switches	$\frac{V_o}{2+ND(1-D)}$	$\frac{V_o}{2N+1}$	$\frac{V_o}{1+D+2N}$
Input current ripple	Medium	Large	Close to zero

voltage stresses on the power components and the turns ratio N under D=0.6. It can be concluded that when N=1, the voltage stresses on the switches S_1, S_2 and the diodes D_1, D_2 are approximately 1/4 of the output voltage, and the voltage stresses on the diodes D_3, D_r are equal to 5/9 of the output voltage

D. Key Performance Comparison

To demonstrate the performance of the proposed converter, the key component quantities, the voltage gain, the normalized voltages stress of the active switches, and the input current ripple performance of the proposed converter and other similar high step-up interleaved converters are displayed in Table I.

It can be seen that the voltage gain of the proposed converter is higher than that of the converters in [25] and [26]. In addition, the proposed converter has the lowest voltage stresses on the active switches. Moreover, the input current ripple of the proposed converter is close to zero, which simplifies the electromagnetic interference (EMI) filter design and helps to extend the lifetime of power generation equipment.

IV. DESIGN CONSIDERATIONS

A. Design Consideration of Coupled Inductors

The turns ratio is one of the key parameters of the suggested converter since it determines the voltage gain and voltage stresses on the power devices. In general, in order to reduce the conduction loss of the main switches, the duty ratio should be no higher than 0.8. The turns ratio of the coupled inductor can be calculated by:

$$N=\frac{1}{2}\left[M_{CCM}(1-D)-1-D\right] \tag{27}$$

The voltage gain of the proposed converter is designed as ninefold, and the duty ratios of the switches are chosen as 0.6. Once the duty ratios of the switches and the voltage gain are chosen, according to the above equation, N=1 will be the proper choice.

Based on the aforementioned analysis, the voltage gain is less sensitive to the coupling coefficient k. However, the leakage inductances of the coupled inductors can be designed to restrain the current falling rate and to alleviate the reverse recovery problem of the diode. In addition, the leakage inductances L_{k1} and L_{k2} should be designed to be as consistent as possible. The relationship of the leakage inductance, the diode current falling rate, and the turns ratio is given by:

$$\frac{di_{Dr}}{dt}=\frac{di_{D3}}{dt}\approx\frac{V_O}{N(1+D+2N)(L_{k1}+L_{k2})} \tag{28}$$

When the leakage inductances L_{k1} and L_{k2} are equal to 1.8μH, the current falling rate of the diodes D_r and D_3 can be decreased at approximately 30A/us, which alleviates the diode reverse-recovery problem. It can be concluded that a small leakage inductance can limit the diode current falling rate to a low level. The actual inductance of the magnetizing inductors L_{k1} and L_{k2} is measured as 2.1uH.

The value of the magnetizing inductors L_{m1} and L_{m2} can be designed based on the foundation of the boundary operating condition, which is derived from:

$$L_{mB}=\frac{R\cdot D(1-D)^2}{2f_S(1+N)(1+D+2N)}=66.7uH$$

To ensure the CCM operation of the proposed converter, the actual inductance of the magnetizing inductors L_{m1} and L_{m2} is designed as 80uH.

B. Design Consideration of the Capacitors

Energy transfers from the input dc source to the load through the auxiliary inductor L_S, and the capacitors C_1, C_2, C_3, C_O and C_m. According to $\Delta Q=C\cdot\Delta V_C=I_C\cdot\Delta T$, the relationship between the voltage ripple and the output power is derived as follows:

$$C = \frac{P_O}{V_O \Delta V_C f_S} \tag{29}$$

Where P_O is the output power, V_O is the output voltage, ΔV_C is the maximum tolerant voltage ripple on the capacitors C_1, C_2, C_3, C_O and C_m, and f_S is the switching frequency [26]. It can be seen that the voltage ripple on capacitors can be suppressed by a large capacitor. However, large capacitors have a bulky volume, high cost and short life. On the other hand, to realize ripple-free input current, the capacitances of the capacitors C_1, C_2, C_3 and C_O should be large enough to ensure that the voltages across C_1, C_2, C_3 and C_O are constant in one switching period. In addition, when the capacitance of an aluminum electrolytic capacitor increases, the ESR becomes smaller, which reduces the power losses. Therefore, a compromise should be made in the selection of a capacitor among the input current ripple performance, converter efficiency, converter lifetime, and cost.

V. Experimental Verifications

In order to verify the performance of the proposed converter, an experimental prototype has been built and tested with the specifications in Table II.

Some key experimental waveforms of the proposed converter are shown in Figs. 8-15. Fig. 8 displays the performance of the currents through the primary side leakage inductances i_{Lk1} and $_{Lk2}$ of the coupled inductors. It can be

TABLE II

Utilized Components and Parameters of the Prototype

Components	Parameters
Input voltage V_{in}	$42V$-$50V$
Output voltage V_O	$400V$
Maximum output power P_O	$400W$
Switching frequency f_S	40kHz
Coupled inductors $N1$,$N2$	$N1$=$N2$: 14T:14T
	L_{m1}=L_{m2}=80uH L_{k1}=L_{k2}=2.1uH
	Core:EE55 PC40
Auxiliary inductor L_S	20uH
Power switches S_1, S_2	IRFP260N(V_{DSS}=200V,$R_{DS(on)}$=0.04Ω)
Diodes D_1, D_2	MBR20200
Diodes D_3, D_r	MUR2040
Capacitors C_1, C_2, C_m	100uF/160V
Capacitor C_3	100uF/250V
Capacitor C_O	330uF/450V

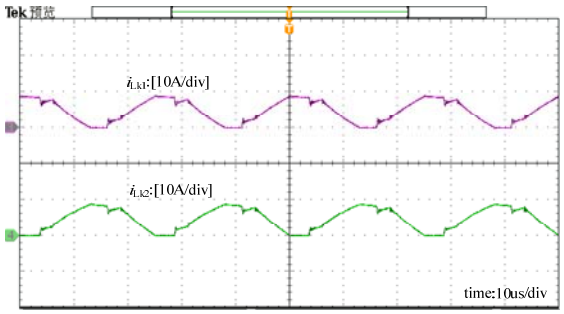


Fig. 8. Experimental results of i_{Lk1} and i_{Lk2}.

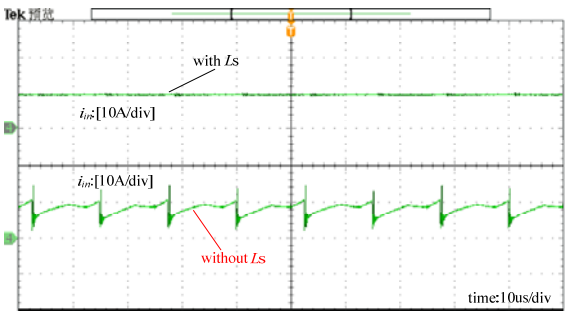


Fig. 9. Experimental comparison between input currents i_{in} with and without the auxiliary inductor Ls.

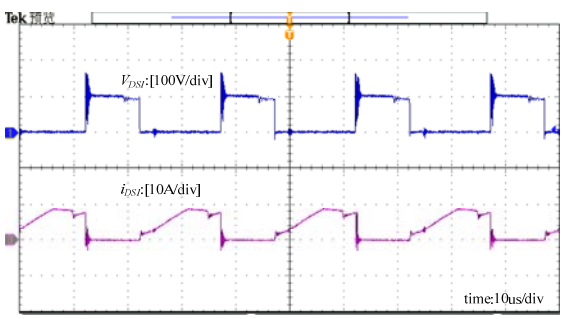


Fig. 10. Experimental results of V_{DS1} and i_{DS1}.

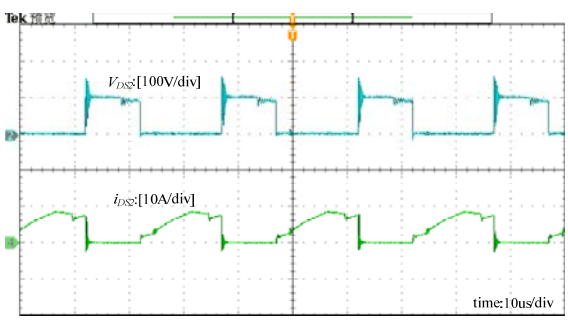


Fig. 11. Experimental results of V_{DS2} and i_{DS2}.

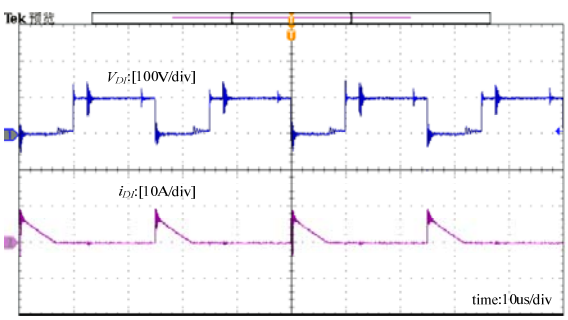


Fig. 12. Experimental results of V_{D1} and i_{D1}.

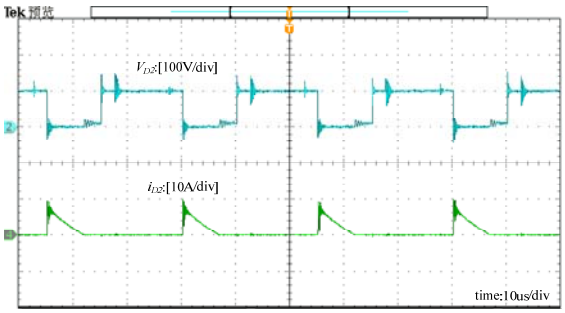


Fig. 13. Experimental results of V_{D2} and i_{D2}.

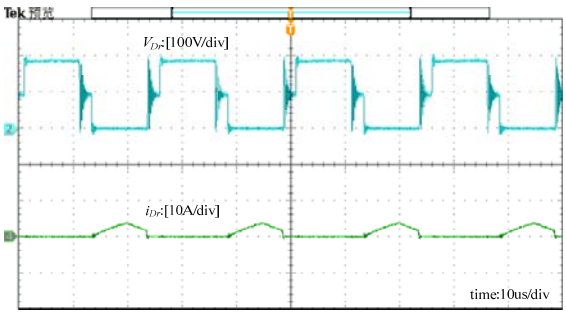


Fig. 14. Experimental results of V_{Dr} and i_{Dr}.

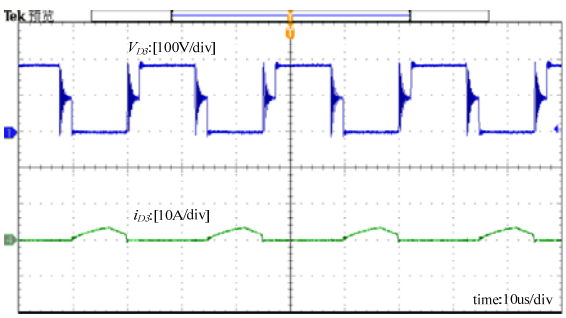


Fig. 15. Experimental results of V_{D3} and i_{D3}.

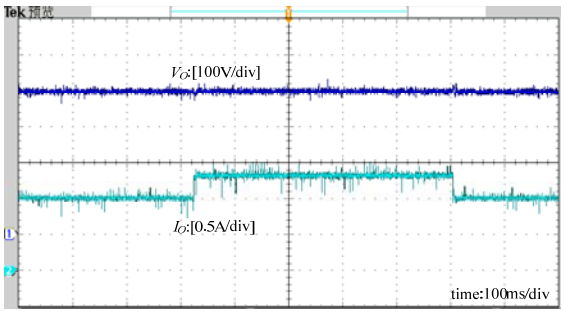


Fig. 16. Dynamic response waveforms from 400W to 550W.

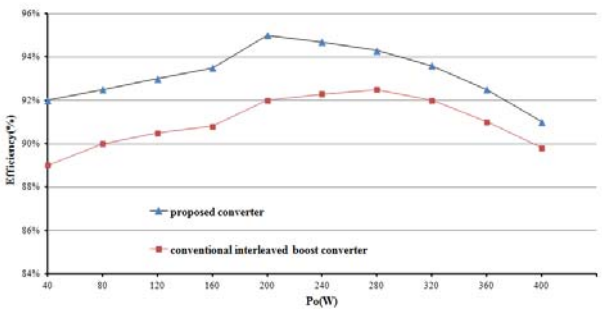


Fig. 17. Measured efficiency of the proposed converter.

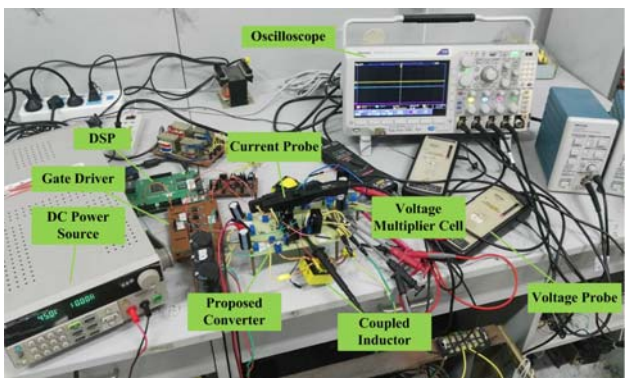


Fig. 18. Photo of the experimental system.

seen that the currents i_{Lk1} and i_{Lk2} are interleaving and approximately the same. This is in agreement with the theoretical analysis.

To demonstrate the influence of the auxiliary inductor Ls, an experimental waveform comparison between the input current i_{in} with Ls and the input current i_{in} without Ls is made in Fig. 9. It can be seen that the input current ripple is approximately zero when the auxiliary inductor Ls exists, while the input current ripple is relatively large when the auxiliary inductor Ls is removed. This is in agreement with the theoretical analysis.

Experimental results of the voltage stresses of S_1 and S_2 and the current waveforms passing through them are shown in Fig. 10 and Fig. 11. It can be seen that the voltage stresses on the switches S_1 and S_2 are clamped at approximately 100V and that there are voltage spikes across switches S_1 and S_2 due to the leakage inductances of the coupled inductors.

Fig. 12 and Fig. 13 show the voltage and current stresses on the diodes D_1 and D_2. It can be seen that the voltage stresses on the diodes D_1 and D_2 are about 100V. This is in agreement with the theoretical analysis. Thus, low-voltage rated diodes with high performance can be adopted for the proposed converter. In addition, the diodes D_1 and D_2 can be turned off naturally.

Fig. 14 and Fig. 15 display the voltage and current stresses on the diodes D_r and D_3. It can be seen that the voltage stress on diode D_r is approximately 180V, which is equal to the voltage stress on diode D_3. These results are in agreement with the steady-state analysis and operating principle.

Fig. 16 shows the dynamic response between 550W and 400W because of a step load variation. It can be seen that the output voltage is maintained at 400V.

A measured efficiency comparison according to the power variation between the conventional interleaved boost converter and the proposed converter is sketched in Fig. 17. The maximum efficiency of the proposed converter is about 95.3% at Pout=200W, while the efficiency is approximately 91.2% at a full load. Fig. 18 shows a photograph of the experimental system for the proposed converter.

VI. CONCLUSION

In this paper, a modified interleaved boost converter for high step-up applications is presented. The proposed converter can reach a high step-up gain without an extreme duty ratio. Meanwhile, the input current ripple of the proposed converter can be decreased to zero by employing a small auxiliary inductor, which simplifies the EMI filter design. Moreover, the voltage stresses on the power switches are very low. As a result, high performance MOSFETs with low voltage rated and low resistance r_{DS}(ON) can be selected to reduce the conduction losses and cost. In addition, the reverse recovery problem of the diodes is alleviated due to appropriate leakage inductances of the coupled inductors. Furthermore, the energy of the leakage inductances can be recycled to the output through the capacitors C_1 and C_2. All of these features make this converter suitable for high power applications where a large voltage gain is demanded. The steady-state characteristics and the main circuit performance are investigated minutely to explore the advantages of the proposed converter. An experimental prototype was developed with an input voltage source from 42V to 50V and a 400V output voltage. The results verified the correction of the theoretical analysis.

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