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Sequence Pulse Modulation for Voltage Balance in a Cascaded H-Bridge Rectifier

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Abstract

With the development of multilevel converters, cascaded single-phase H-bridge rectifiers (CHBRs) has become widely adopted in high-voltage high-power applications. In this study, sequence pulse modulation (SPM) is proposed for CHBRs. SPM is designed to balance the dc-link voltage and maintain the smooth changes of switch states. In contrast to phase disposition modulation, SPM balances the dc-link voltage even after removing the load of one submodule. The operation principle of SPM is deduced, and the unbalance degree of SPM is analyzed. All the proposed approaches are experimentally verified through a prototype of a four-module (nine-level) CHBR. Conclusions are drawn in accordance with the results of SPM and its imbalance degree analysis.

Key words: CHBR, Sequence pulse modulation, Voltage balance

I. INTRODUCTION

Multilevel converters are widely adopted in industry applications, thereby providing an attractive solution to high-voltage high-power issues [1]-[3]. Cascaded H-bridge converters, a type of multilevel converter, are regarded as an interesting topology due to their modularization, extendibility, and simple layout [4], [5]. Capable of transforming ac voltage to lower dc voltage, cascaded H-bridge rectifiers (CHBRs) are used as components of power electronic traction transformers (PETTs) and solid-state transformers (SSTs). These transformers are considered as competitive alternatives to traditional transformers [4]-[6]. However, CHBRs are prone to dc-link voltage imbalance caused by unbalanced input or output power [7]-[20].

To balance the dc-link voltage of CHBRs, industries and the academe have developed a variety of solutions [4]-[17]. The topology of a PETT is shown in Fig. 1. Each module of the CHBR is linked to a dc/dc converter. Each dc/dc converter in a PETT or SST is regarded as independent, thereby allowing the dc-link voltage imbalance problem to be thoroughly researched [6]-[20]. In [4], a dc/dc converter is used in a PETT to isolate the output of a CHBR and allow each cell to be paralleled to rate the full power. In addition, a PI controller is adopted to maintain the dc-link voltage around the average value [4], [5]. Without a parallel connection, a voltage balance strategy is needed to control a CHBR once the output powers of its modules become unequal. In [7], three PI-based balance solutions for CHBRs are discussed. However, only one of the solutions is correct. The limitation of voltage balance caused by PI control is analyzed and verified in [8]. A novel modular cascaded multilevel converter with a multi-winding high-frequency transformer equipped with a PI controller is applied for voltage balancing in [9]. In [10], voltage and power balance control for a three-module CHBR is developed, and the maximum power unbalance is controlled with a PI-based balance solution. The experiment shows that the maximum values of power imbalance are 32, 32, and 65 Ω. These existing studies illustrate how the PI controller changes the input power of each module to balance the voltage. This method is always applied in the industry because of its robustness [4]-[10].

Alternative modulation-based solutions are widely studied to extend the voltage balance region [11]-[16]. In [11], a general switching technique for voltage balance is proposed. To balance the dc-link voltage with extremely unbalanced loads, the work in [12] extends the operating region used in [11] and finds that the three-module CHBR works well when the load of one module is removed, that is, 120, 120, and 0 W, in comparison with that in [10]. A 2D modulation is described in [13], [14] with two-module cascaded converters in multidimensional representation. Based on this method, a

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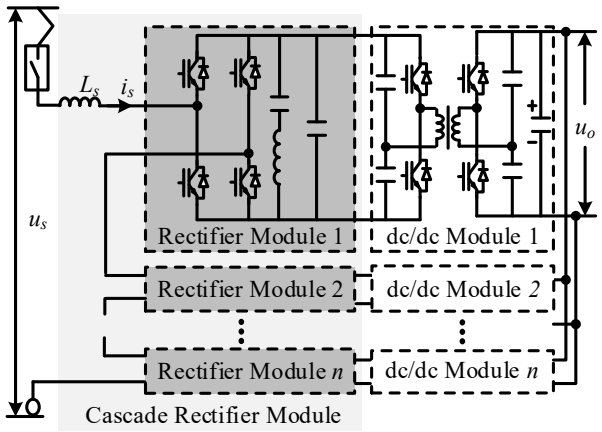


Fig. 1. Topology of power electronic traction transformer.

3D space modulation technique is proposed for a three-module SST [15]. However, with several modules connected in series, the increased number of switch states adds to the complexity of the n-D concept. In [15], the PI control and PI-based method is compared with an alternative modulation-based solution under the same condition; the switching technique is proved to be particularly effective because alternative modulation-based solutions could not change the control of CHBRs. In [16], the stable operation area of dimensional modulation is analyzed. In [17]–[20], the voltage balance of cascade converters is developed and discussed.

On the basis of existing studies, the present work proposes a sequence pulse modulation (SPM) for balancing the voltage in CHBRs. At the same time, the switch state of each module is ruled to change smoothly. This modulation is comprehensible and suitable for the N-module because the sequence pulse of switch states is calculated ahead of CHBR start-up. The study also involves an analysis of the calculation of imbalance degree. The experimental results show that the proposed SPM can be used to balance the voltage when one load of a CHBR is removed.

The rest of this paper is organized as follows. Section II describes the configuration, control, and theory of voltage balance of CHBRs. Section III explains and analyzes the proposed SPM. Finally, Section IV illustrates the experiment result of the SPM in a four-module CHBR.

II. CONFIGURATION

A. Configuration

The topology of a CHBR is shown in Fig. 2(a). The H-bridge converter modules are cascaded to transform the grid voltage U_s to dc voltage V_{dc}. In studying the dc-link voltage balance, the loads of the CHBR can be regarded as two independent loads. The CHBR is mathematically described as follows:

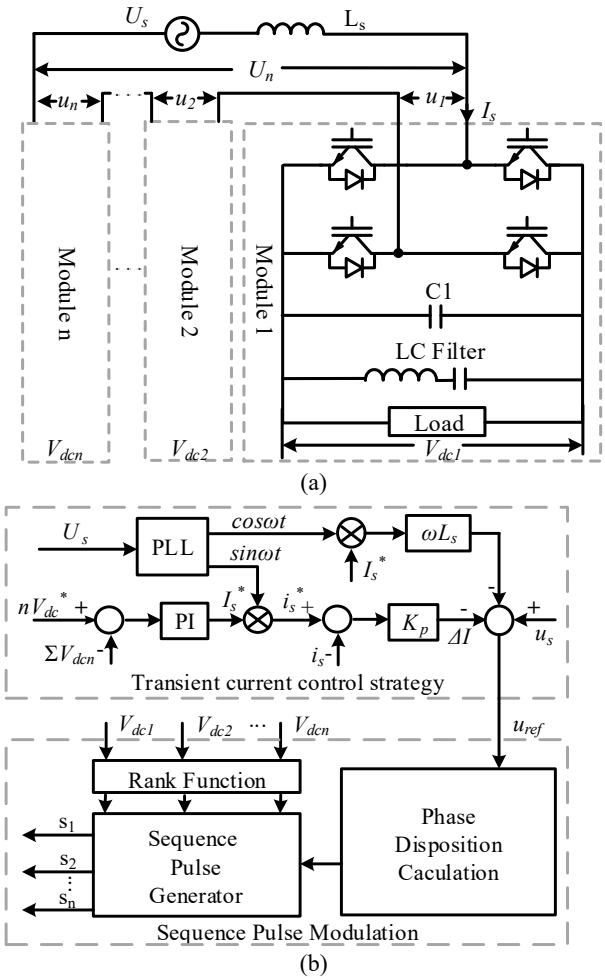


Fig. 2. Configuration of CHBR: ((a) topology of CHBR and (b) control of CHBR)).

$$\begin{cases} U_n = \sum_{i=1}^{n} u_i \\ U_s - j\omega L_s i_s = U_n \end{cases}, \tag{1}$$

where L_s is the filter inductance of the rectifier, U_n is the input voltage of the CHBR, and u_i is the input voltage of the H-bridge. The process of the algorithms is illustrated in Fig. 2(b). The transient current control strategy (TCCS) is adopted. Once the result (U_n) of the TCCS is obtained, the voltage level is calculated through phase disposition calculation (PDC), which is based on the modulation of phase disposition. Then, the rank function is used to rank the module through the dc-link voltage. Finally, the switch state of each module is determined with a sequence pulse generator.

The TCCS is applied to achieve the following goals: to maintain the sinusoidal grid current and power factor unity and to trace the sum of the reference dc-link voltages. The TCCS is made up of the voltage outer loop and current inner loop, as shown in Fig. 2(b). I_s* is acquired by processing the error between V_{dc}* and the sum of V_{dci} through a PI controller, V_{dc}* is the sum of the reference dc-link voltages, and V_{dci} is the dc-link voltage of each module.

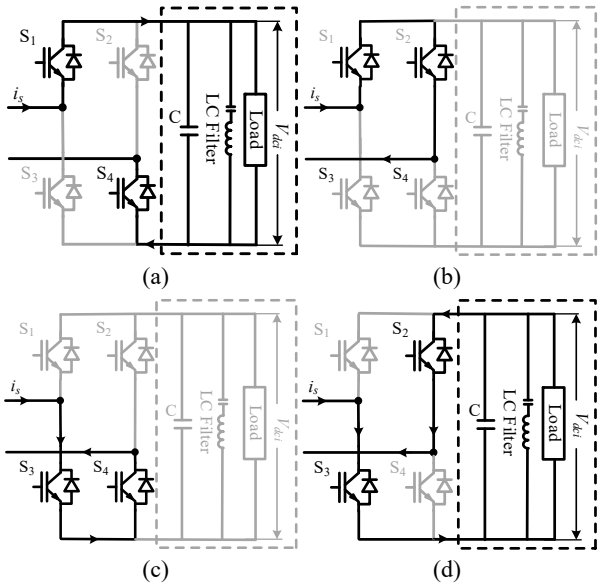


Fig. 3. Switch state of H-bridge. ((a) IGBT state (1001), switch state (1); (b) IGBT state (1100), switch state (0); (c) IGBT state (0011), switch state (0); (d) IGBT state (0110), switch state (−1)).

The phase and frequency of u_s are detected by the phase-locked loop and can be used as the phase and frequency of i_s*. A sinusoidal grid current is obtained by adopting a proportional controller to keep the grid current i_s in accordance with i_s*. Thus, u_{ref} is acquired and can be written as

$$\begin{cases} i_s^* = K_{vp}(V_{dc}^* - \sum V_{dc}) + \int (V_{dc}^* - \sum V_{dci})dt / K_{vi} \\ u_{ref} = u_s - \omega L i_s^* \cos \omega t - K_{ip}(i_s^* \sin \omega t - i_s) \end{cases}. \quad (2)$$

Analysis of CHBR

The CHBR is analyzed to explain the theory of PDC, sequence pulse generator, and rank function clearly. Based on the Kirchhoff voltage law, the U_n of the CHBR can be expressed as

$$\begin{cases} u_i = S_i \cdot V_{dci} \\ U_n = \sum_{i=1}^{n} S_i \cdot V_{dci} \end{cases}, \quad (3)$$

where n is the number of modules and S_i is the switch state of the module i. The switch states of one module in this study are illustrated in Fig. 3. According to the different IGBT states of the H-bridge, three results of S_i are shown.

$$S_i = \begin{cases} 1, IGBT\ state(1001) \\ 0, IGBT\ state(1010\ or\ 0101) \\ -1, IGBT\ state(0110) \end{cases}, \quad (4)$$

where the IGBT state denotes the state of the power semiconductors from S_1 to S_4. With regard to the IGBT as an ideal switch, "1" represents the on state while "0" represents the off state. Thus, couples of a switch state sequence satisfy equation (3) while ignoring the bias among V_{dc} of each module.

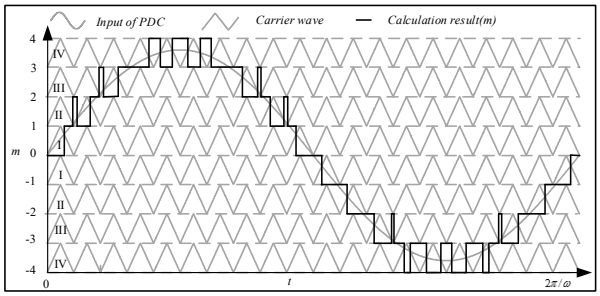


Fig. 4. Phase disposition calculation for CHBR.

According to the switch states of the H-bridge module, the input power of the module is

$$P_i = S_i \cdot V_{dci} \cdot i_s, \quad (5)$$

where P_i is the input power of the module. As the dc-link voltage is positive, whether the power flow is positive depends on S_i and i_s. Based on power conservation, the output power of the module is

$$P_i = C \cdot V_{dci} \frac{dV_{dci}}{dt} + \frac{V_{dci}^2}{R}. \quad (6)$$

The possibilities of P_i are described as follows:

P_i is positive when both S_i and i_s are positive or negative. The module absorbs power from the grid, and V_{dci} increases according to (6).

P_i is zero when S_i or i_s is zero. The module rejects the power from the grid. V_{dci} may decline according to (6). However, when the module is under no-load condition, V_{dci} remains unchanged.

P_i is negative when S_i and i_s are opposite. The module releases power to the grid, and V_{dci} declines according to (6).

III. Sequence Pulse Modulation

As parts of SPM, the algorithm of the PDC, the sequence pulse generator, and the rank function are described in this section. A four-module CHBR prototype is adopted to illustrate the advantage of SPM in CHBRs and verify it experimentally.

A. Phase Disposition Calculation

The result of PDC is obtained on the basis of phase disposition (PD) modulation. The calculation is illustrated in Fig. 4. The levels of the modulation wave are determined by the number of CHBR modules. The output of PDC is considered as the reference of the summation of S_i.

According to the result of PDC, the switch states could be arranged (as in Table I) to balance the dc-link voltage; the dc-link voltage relationship is $V_{1st}<V_{2nd}<V_{3th}<V_{4th}$. Nevertheless, the voltage could be balanced with PD modulation as the switch states change smoothly, as described in the analysis of CHBR in the previous section. When the CHBR transmits power from the grid to the load, the PD modulation could offer minimal switch states for the

TABLE I
PHASE DISPOSITION MODULATION FOR VOLTAGE BALANCE

m	S_{1st}	S_{2nd}	S_{3th}	S_{4th}
4	1	1	1	1
3	1	1	1	0
2	1	1	0	0
1	1	0	0	0
0	0	0	0	0
−1	−1	0	0	0
−2	−1	−1	0	0
−3	−1	−1	−1	0
−4	−1	−1	−1	−1

TABLE II
VOLTAGE LEVEL AND SWITCH MODE

Initial	Final	Initial	Final	Times
1	0	1001	1100(0011)	2
1	−1	1001	0110	4
0	1	1100(0011)	1001	2
0	−1	1100(0011)	0110	2
−1	0	0110	1100(0011)	2
−1	1	0110	1001	4

release of power to the grid. That is, the voltage balance ability could be extended.

B. Proposed Sequence Pulse Generator

With the summation of S_i, the sequence pulse generator is designed for scheduling S_i of each module. The switching times of the IGBTs when S_i changes are presented in Table II with consideration of the possibility of switch states. Obviously, the switch state that changes between 1 and −1 is subjected to the maximum switching time.

The role of switch states is explained to select the proper switch state for the module.

S_i=1. P_i is positive if i_s>0. Otherwise, P_i is negative if i_s<0. This state is able to change V_{dci}, and it is useful in balancing the dc-link voltage.

S_i=0. P_i is zero regardless of i_s. This state is not helpful in balancing the dc-link voltage. However, a "0" state is necessary because it could smoothen the modulation by preventing the state switch from jumping from 1 to −1. That is, S_i=0 is favorable in the modulation, but the number of S_i=0 should be restricted.

S_i=−1. P_i is negative if i_s>0. Otherwise, it is positive. Capable of changing V_{dc}, this state is useful in balancing the dc-link voltage.

As for the dc-link voltage balance of the modules, if i_s>0, the module with a high dc voltage is required to absorb low active power or release active power from the dc-link capacitor to the ac grid (switch state −1 or switch state 0) to keep the dc-link voltage of each module balanced. By contrast, the module with a low dc voltage is required to absorb active power from the ac grid (switch state 1 or switch state 0). If i_s<0, the module in which the dc-link voltage is high requires switch state 1 or switch state 0, whereas the module in which the dc-link voltage is low requires switch state −1 or switch state 0.

TABLE III
PROPOSED SEQUENCE PULSE GENERATOR

m	S_{1st}	S_{2nd}	S_{3th}	S_{4th}
4	1	1	1	1
3	1	1	1	0
2	1	1	0	0
1	1	1	0	−1
0	0	0	0	0
−1	−1	−1	0	1
−2	−1	−1	0	0
−3	−1	−1	−1	0
−4	−1	−1	−1	−1

The number of switch states of the four-module CHBR is expressed as

$$\begin{cases} p + ng + z = n \\ p - ng = m \end{cases}, \tag{7}$$

where p is the number of modules in which S_i=1, z is the number of modules in which S_i=0, ng is the number of modules in which S_i=−1, n is the number of modules, and m is the result of PDC. The solution is made unique by establishing two restrictions based on the principles of modulation: 1) p, ng, and z are natural numbers; and 2) z is 1 or 2 when $m \neq \pm n$ or 0. The solution is expressed as

$$\begin{cases} p = (m + n - z)/2 \\ ng = (-m + n + z)/2 \\ z = 1 \; or \; 2 \end{cases}, \tag{8}$$

where z=1 when m+n is an odd number and z=2 when m+n is an even number. In this way, the solutions of formula (8) are guaranteed to be integers. No "0" state occurs when m=±n, and all S_i modules are 0 when m=0 for changing the state smoothly.

We assume that the TCCS manages to control the power factor of the CHBR. The sequence pulse of the four-module CHBR is calculated and presented in Table III; the dc-link voltage relationship of these modules is V_{1st}<V_{2nd}<V_{3th}<V_{4th}.

However, for example, S_i may jump between 1 and −1 if m changes between 2(−2) and 1(−1). Thus, the sequence pulse could balance the voltage while the switch state changes smoothly as long as the rank of V_{dci} changes smoothly. The rank function is needed to smoothen the rank of V_{dci}.

C. Rank Function

As shown in Table III, if m changes from 2 to 1, the rank number of the dc-link voltage changes from 2 to 4, the switch state jumps from 1 to −1, and the switch frequency increases. The rank function is designed to avoid this jump. The module

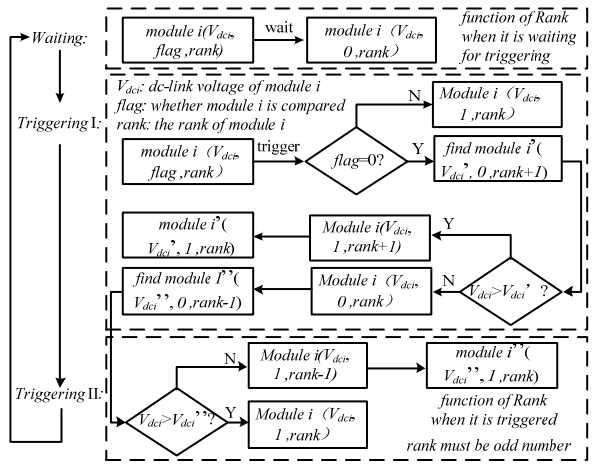


Fig. 5. Rank function.

i is formatted as

$$module\,i(V_{dci}, flag, rank)\,, \tag{9}$$

where V_{dci} is the input and *flag* stands for a register to save the number of exchanges. *rank* is the rank number of the module. When the rank number of the module is high, the dc-link voltage of the module is also high. According to the modulation principles, two goals of rank function should be achieved. One is to confirm the rank number of the modules for voltage balance, and the other is to change the rank number of the modules smoothly to prevent the switch state from jumping.

The function process is shown in Fig. 5. The following three steps are taken:

1. Waiting for triggering. In maintaining the smooth change of the switch states, the rank function works only if *m* is changing. The *flag* is reset to 0 in this step.

2. Trigging I. When *m* changes, the module with an odd rank number, such as the module with *rank*, is selected and compared with the module with *rank*+1. If the dc-link voltage of the module with *rank* is bigger than that of the module with *rank*+1, they exchange their *rank*, and their flags are refreshed to 1. Otherwise, their flags remain 0.

3. Trigging II. When step 2 is finished, the modules with *rank* are selected and compared with the modules with *rank-1* but only if both of their flags are 0. If the dc-link voltage of the module with *rank* is smaller than the module with *rank*+1, they exchange their *rank*, and their flags are refreshed to 1. Otherwise, no exchanges occur, and their flags remain 0.

D. Unbalance Degree Analysis

The dc-link capacitor voltages of all modules are equal in the cascaded converter if the loads are balanced. The imbalance degree is defined as

$$\Delta y = \frac{n \cdot Y_{min}}{\sum_{j=1}^{n} Y_j}\,, \tag{10}$$

where Y_{min} is the minimum admittance of the CHBR. If the loads of all modules are equivalent, Δy=1. If the load of one module is 0, Δy=0. Therefore, the range of Δy is between 0 and 1. Thus, Δy is able to indicate the load imbalance degree. According to the analysis of part II, the input power of module 1 is

$$P_{i1} = u_1 \cdot i_s\,. \tag{11}$$

The dc-link voltage of this module is defined as V_{dc1}, and the admittance of module 1 is defined as Y_1. We assume that Y_1 equals Y_{min}. The output active power of module 1 is

$$P_{o1} = V_{dci}^2 \cdot Y_1\,. \tag{12}$$

According to the volt-second balance principle,

$$\begin{cases} V_{dca}T_a + V_{dcb}T_b = 4V_{dc}Msin(\omega t)T_s \\ T_a + T_b = T_s \end{cases}, \tag{13}$$

where T_a and T_b are the working times of the low and high voltage levels in one period T_s. V_{dca} and V_{dcb} are the voltages of each area. *M* is the peak value of the modulation wave generated by the TCCS. When the modulation wave transits from area I to area IV (Fig. 4), T_a and T_b can be calculated accordingly, as shown in Table IV.

TABLE IV
WORKING TIME OF VOLTAGE LEVEL

m	T_a	T_b
I	$(1\text{-}4M\sin(\omega t))T_s$	$(4M\sin(\omega t))T_s$
II	$2\text{-}4M\sin(\omega t)\ T_s$	$(4M\sin(\omega t)\text{-}1)T_s$
III	$3\text{-}4M\sin(\omega t)\ T_s$	$(4M\sin(\omega t)\text{-}2)T_s$
IV	$4\text{-}4M\sin(\omega t)\ T_s$	$(4M\sin(\omega t)\text{-}3)T_s$

We assume that the modulation waves are symmetrical in one period. The calculation could be simplified into a quarter period. As Y_1 is the minimum, V_{dc} increases if all CHBR modules acquire the same power. Therefore, according to SPM, the output power of module 1 should be the lowest to balance the dc-link voltage. The relationship between the PDC reference and S_1 is described as follows.

1. In area I, S_1 is 0 when *m* is 0 and S_1 is −1 when *m* is 1.
2. In area II, S_1 is −1 when *m* is 1 and S_1 is 0 when *m* is 2.
3. In area III, S_1 is 0 when *m* is 2 and S_1 is 0 when *m* is 3.
4. In area IV, S_1 is 0 when *m* is 3 and S_1 is 1 when *m* is 4.

The output power is integrated to obtain the output energy. Thus, the output energy can be calculated as

$$\begin{cases} Q_{11} = -\int_0^{\sin^{-1}(\frac{1}{4M})} V_{dc1} i_s (4M\sin t)dt \\ Q_{12}' = -\int_{\sin^{-1}(\frac{1}{4M})}^{\sin^{-1}(\frac{1}{2M})} V_{dc1} i_s (2-4M\sin t)dt \\ Q_{14} = \int_{\sin^{-1}(\frac{3}{4M})}^{\frac{\pi}{2}} V_{dc1} i_s (4M\sin t-3)dt \\ Q_{11}' = Q_{12} = Q_{13} = Q_{13}' = Q_{14}' = 0 \end{cases}. \tag{14}$$

This process of calculation is shown in Fig. 6. Q_{11}, Q_{11}', Q_{12}, Q_{12}', Q_{13}, Q_{13}', Q_{14}, and Q_{14} are the output energies of

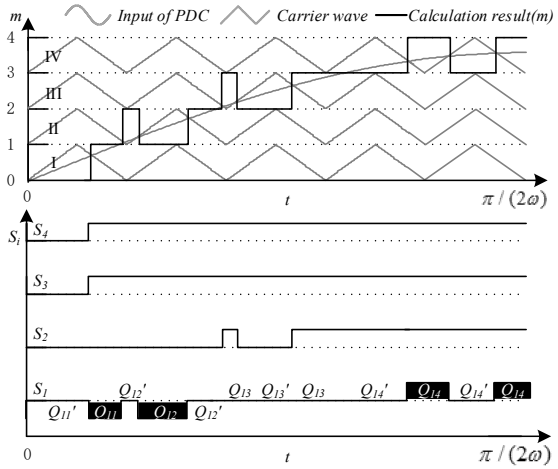


Fig. 6. Calculation of imbalance degree.

the four areas and $\sin^{-1}()$ is the inverse trigonometric sine function. V_{dc1} is the dc-link voltage of module 1. According to the energy conservation law, the output energy is equal to the input energy.

$$\begin{aligned} Q_1 &= \sum_{t=1}^{4} Q_{1t} + \sum_{t=1}^{4} Q_{1t}' = V_{dc} \cdot I_s \cdot q_1 = Q_{o1} + Q_{c1} \\ &= V_{dc}^2 Y_1 \cdot \pi / 2 + C\Delta V_{dc}^2 / 2 \end{aligned}, \quad (15)$$

where Qo1 is the output energy of module 1 and Qc1 is the energy storage in the capacitor during one quarter of a period. If Qc1 is less than 0, then the dc-link voltage decreases in this quarter period. As Q_1 is the minimum energy when SPM operates, Q_{o1} should be less than Q_1. The judgment of the imbalance degree is illustrated as

$$Q_1 = V_{dc} \cdot I_s \cdot q_1 \le Q_{o1}, \quad (16)$$

where $q_1 = Q_1/(V_{dc} \cdot I_s)$, which is an intermediate variable. q_1 is simplified by Q_1. Combining formulas (14) and (15) yields

$$V_{dc}^2 \cdot \sum_{i=1}^{n} Y_i = U_s \cdot I_s . \quad (17)$$

Moving items can obtain

$$I_s = V_{dc}^2 \cdot \sum_{i=1}^{n} Y_i / U_s . \quad (18)$$

According to the preamble analysis, m_i is the modulation depth of each module, which is equal to the cascaded rectifier modulation depth when loads are balanced. The voltage of each module is

$$\sqrt{2} U_{ni} = m_i \sum V_{dci} . \quad (19)$$

According to the relationship between the output voltage and modulation, the maximum of the output voltage is

$$U_s \approx U_n = n \cdot M \cdot V_{dc} / \sqrt{2} . \quad (20)$$

According to the preceding equations, the simultaneous equations of $\Delta y'$ can be constructed as

$$\Delta y \ge \Delta y' = \frac{n \cdot Y_i}{\sum_{j=1}^{n} Y_i} = \frac{2\sqrt{2} \cdot q_1}{\pi \cdot M}, \quad (21)$$

Experiment

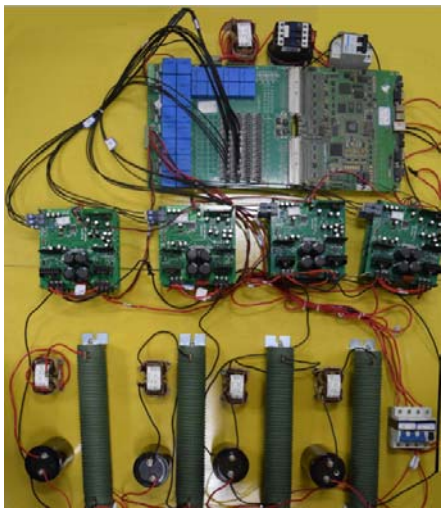


Fig. 7. Prototype of four-module (nine levels) CHBR.

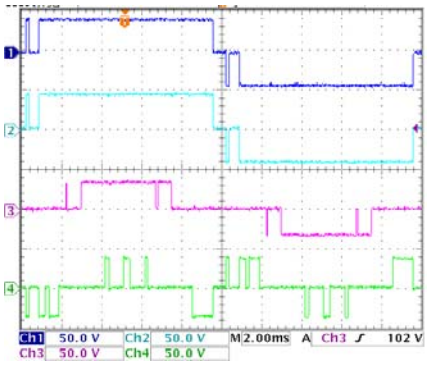
TABLE V
EXPERIMENTAL CIRCUIT PARAMETERS

Parameter Name	Values
Voltage source	100 V/50 Hz
Filter inductance	1 mL
dc-link output	38–60 V
dc-link capacitor	1,880 μF
Output power	360 W
Carrier wave frequency	1,000 Hz
Inductance of LC filter	1 mH
Capacitance of LC filter	2,200 μF
Number of modules	4

where $\Delta y'$ is the limitation of the imbalance degree. SPM could not keep the balance when $\Delta y' > \Delta y$ under the same M theoretically. $\Delta y'$ could be equal to 0 when M<0.83, which indicates that the CHBR is able to function well when one of the modules is not loaded in this condition.

As shown in Fig. 7, a four-module CHBR prototype is built to verify the controller and proposed modulations. The CHBR works in this case for the 50 Hz 100 V input voltage and 38 V to 60 V dc output voltage. The controller of the CHBR is based on the EP3C55F484C8 FPGA chip. The detailed parameters of the experiment system are listed in Table V.

Fig. 8(a) shows the input voltages of the four modules when the dc-link voltages are related as $V_{dc1} < V_{dc2} < V_{dc3} < V_{dc4}$. As the PDC could retain the total frequency of the carrier wave, the maximum module frequency is less than 1,000 Hz, although the change of the switch state focuses on the unbalanced module. In balancing the dc-link voltage, the transmission power of module 4 at the minimum became that of V_{dc4} at the maximum; the opposite is true for module 1.



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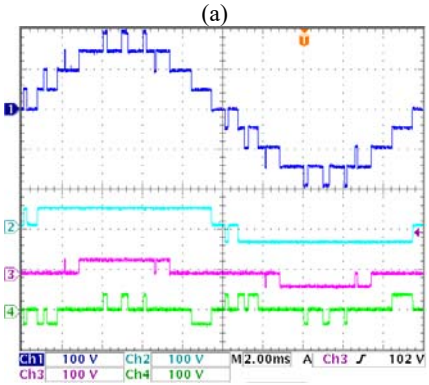

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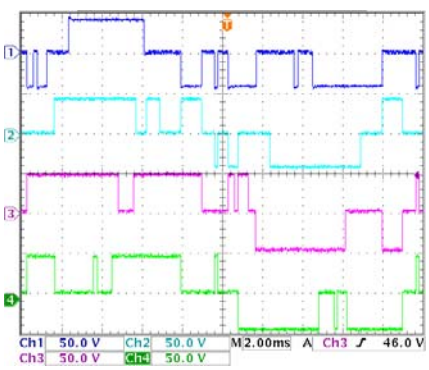
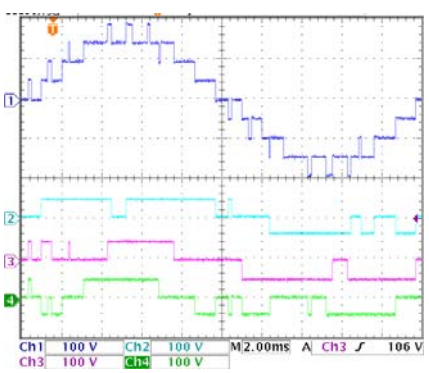
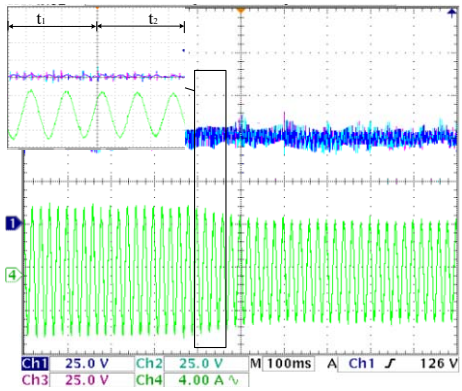


(c)

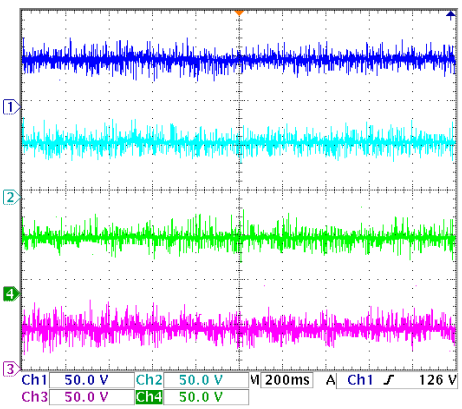


(d)

Fig. 8. Input voltage of SPM. ((a) Input voltage when V_{dc1}< V_{dc2}< V_{dc3}< V_{dc4} (CH1: U_n, CH2: u_2, CH3: u_4, CH4: u_4); (b) input voltage when V_{dc1}< V_{dc2}< V_{dc3}< V_{dc4} (CH1: u_1, CH2: u_2, CH3: u_3, CH4: u_n); (c) input voltage when the dc-link voltage changes (CH1: U_n, CH2: u_2, CH3: u_3, CH4: u_4); and (d) input voltage when the dc-link voltage changes (CH1: u_1, CH2: u_2, CH3: u_3, CH4: u_n)).



(a)

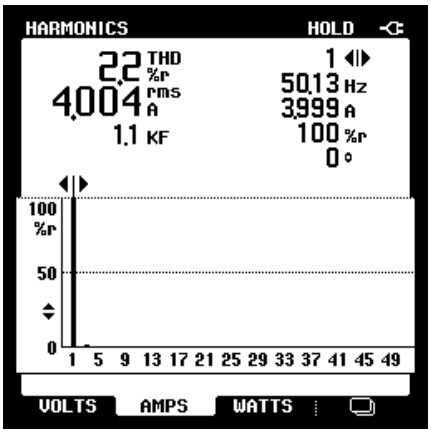


(b)

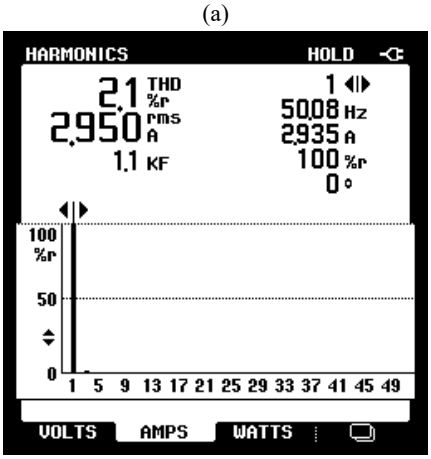
Fig. 9. Waveforms when the load of module 4 is removed. ((a) M=0.8. CH1: V_{dc1}, CH2: V_{dc2}, CH3: V_{dc3}, CH4: i_s; and (b) M=0.8. CH1: V_{dc1}, CH2: V_{dc2}, CH3: V_{dc3}, CH4: V_{dc4}).

Fig. 8(b) shows the input voltage of the CHBR, which is calculated via PDC. Figs. 8(c) and 8(d) show the input voltage when the loads of the modules are balanced. In Fig. 8(c), the input voltage of each module synthesizes U_n as the PDC requires. Fig. 8(d) shows the SPM succeeding in preventing voltage jump. As all the loads of the modules are the same in Figs. 8(c) and 8(d), the input transmission power is almost the same across all modules. In addition, the process is dynamic such that the transmission powers of all modules are not absolutely equal. As shown in Fig. 8, the input voltages change smoothly when SPM is operated.

As shown in Fig. 9(a), the loads of all modules are balanced in the period of t_1. The dc-link voltages of all modules are balanced except for the fluctuation of the dc-link voltage, the average transmission powers of various H-bridge modules are the same. In the period of t_2, the load of module 4 is removed (Δy=0) when SPM is working under M=0.83, and the dc-link voltages of all modules are balanced. Fig. 9(b) shows the voltage and current of the grid when module 1 is under no-load condition. The current declines to three quarters, and the dc-link voltage of each module remains steady. When the CHBR uses the PD modulation, the output power of each module cannot be easily controlled to reach the average output power. Thus, the dc-link voltage fluctuates



(a)



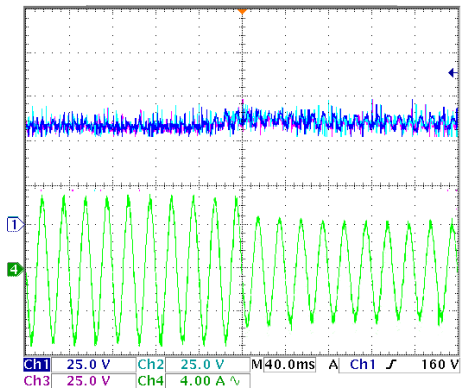
(b)

Fig. 10. THD of i_s. ((a) All modules are balanced; and (b) load of module 4 is removed).

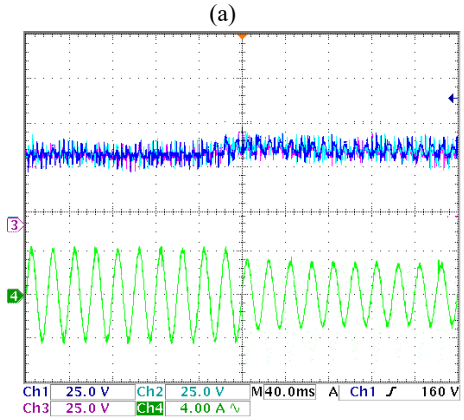
because SPM is based on PD modulation. However, the dynamic characteristic of SPM guarantees that the output power of each module is controllable even under some serious conditions. Furthermore, the modulation in the CHBR could adjust the dc-link voltage, but the inverter could not.

As shown in Fig. 10, the THD in Fig. 9 is measured when the loads are balanced and unbalanced. As the CHBR decreases the THD, its current remains sinusoidal when the module is balanced, as shown in Fig. 9(a). Although the SPM rearranges the switch state of each module, U_n of the CHBR remains unchanged due to the principle of SPM.

A step change experiment is performed to verify the unbalance degree analysis, as shown in Fig. 9 under Fig. 11(a) (M=0.6, V_{dc}=60 V) and Fig. 11(b) (M=1, V_{dc}=38 V). In Fig. 11(a), the load of module 4 is removed (Δy=0), and all dc-link modules remain balanced. In Fig. 11(b), Δy changes from 1 to 0.44 (30, 30, 30, and 70 Ω), and all dc-link modules remain balanced. Based on the calculation in Section 3.3 and the experiment, the curve of the imbalance degree is illustrated in Fig. 12. The results show a good agreement. Moreover, Fig. 11 verifies that the input transmission powers of all modules are the same when the loads of all modules are the same.



(a)



(b)

Fig. 11. Waveforms when M=1 and 0.6. ((a) M=1; CH1: V_{dc1}, CH2: V_{dc2}, CH3: V_{dc3}, CH4: i_s; and (b) M=0.6; CH1: V_{dc1}, CH2: V_{dc2}, CH3: V_{dc3}, CH4: i_s).

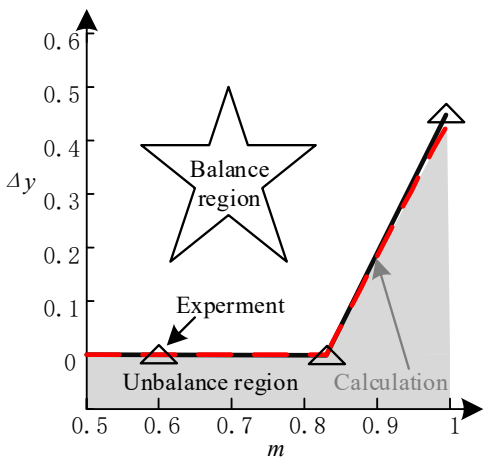


Fig. 12. Comparison between calculation and experiment.

IV. Conclusions

In this study, SPM for CHBRs is proposed, and the imbalance degree of the proposed SPM is calculated. Through an analysis of the performance of the CHBR, the principles of the modulation for the voltage balancing strategy are identified. All results are verified experimentally.

The jump of switch states between 1 and −1 leads to an

increased switch frequency. However, the switch state changes smoothly through the optimized SPM principles. The dc-link voltages of the four-module CHBR are well-balanced with those of the proposed SPM method, even with one of the modules operating without load (Δy=0) at M<0.83.

The voltage balance ability and simplified version of the SPM are illustrated with an increased number of CHBR modules. This issue will be addressed in detail in future publications.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, Ma. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2553-2580, Aug.2010.

[2] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: an enabling technology for high-power applications," *Proceedings of the IEEE*, Vol. 97, No. 11, pp. 1786-1817, Nov. 2009.

[3] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 1884-1896, May 2013.

[4] D. Dujic, C. Zhao, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer-low voltage prototype," *IEEE Trans. Power Electron.*, Vol. 28, No. 12, pp. 5522-5534, Dec. 2013.

[5] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer medium voltage prototype," *IEEE Trans. Ind. Electron.*, 61, No. 7, pp. 3257-3268, Jul. 2014.

[6] X. She, A. Q. Huang, and X. Ni, "Current sensorless power balance strategy for DC/DC converters in a cascaded multilevel converter based solid state transformer," *IEEE Trans. Power Electron.*, Vol. 29, No. 1, pp. 17-22, Jan. 2014.

[7] A. Dell'Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, "Overview of PI-based solutions for the control of DC buses of a single-phase H-bridge multilevel active rectifier," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 3, pp. 857-866, May/Jun. 2008.

[8] T. Zhao, G. Wang, S. Bhattacharya, and A. Q. Huang, "Voltage and power balance control for a cascaded H-bridge converter-based solid-state transformer," *IEEE Trans. Power Electron.*, Vol. 28, No. 4, pp. 1523-1532, Apr. 2013.

[9] Z. Zheng, Z. Gao, C. Gu, L. Xu, K. Wang, and Y. Li, "Stability and voltage balance control of a modular converter with multiwinding high-frequency transformer," *IEEE Trans. Power Electron.*, Vol. 29, No. 8, pp. 4183-4194, Aug. 2014.

[10] J. Shi, W. Gou, H. Yuan, T. Zhao, and A. Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," *IEEE Trans. Power Electron.*, Vol. 26, No. 4, pp. 1154-1166, Apr. 2011.

[11] H. Iman-Eini, J. L. Schanen, S. Farhangi, and J. Roudet, "A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers," *IEEE Trans. Power Electron.*, Vol. 23, No. 5, pp. 2428-2442, Sep. 2008.

[12] M. Moosavi, G. Farivar, H. Iman-Eini, and S. M. Shekarabi, "A voltage balancing strategy with extended operating region for cascaded-bridge converters," *IEEE Trans. Power Electron.*, Vol. 29, No. 9, pp. 5044-5053, Sep. 2014.

[13] J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, and E. Dominguez, "Two-dimensional modulation technique with dc voltage control for single-phase two-cell cascaded converters," *IEEE International Conference on Industrial Technology (ICIT)*, pp. 1365-1370, Mar 2010.

[14] J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.,* Vol. 58, No. 2, pp. 412-420, Feb. 2011.

[15] X. She, A. Q. Huang, and G. Wang, "3-D space modulation with voltage balancing capability for a cascaded seven-level converter in a solid-state transformer," *IEEE Trans. Power Electron.*, Vol. 26, No. 12, pp. 3778-3789, Dec. 2011.

[16] C. Wang, G. Zhang, H. Cheng, and Y. Li, "A novel modulation strategy based on two dimensional modulation for balancing DC-link capacitor voltages of cascaded H-bridges rectifier," in *38th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp. 116-122, Oct. 2012.

[17] X. He, A. Guo, X. Peng, Y. Zhou, Z. Shi, and Z. Shu, "A traction three-phase to single-phase cascade converter substation in an advanced traction power supply system," *Energies*, Vol. 8, No. 9, pp.9915-9929, Sep. 2015.

[18] Z. Gao and H. Fan, "A modular bi-directional power electronic transformer," *Journal of Power Electronics*, Vol. 16, No. 2, pp.399-413, Mar. 2016.

[19] X. Peng, X. He, P. Han, A. Guo, Z. Shu, and S. Gao, "Smooth switching technique for voltage balance management based on three-level neutral point clamped cascaded rectifier," *Energies*, Vol. 9, No. 10, pp. 1996-1073, Oct. 2016.

[20] A. Moeini, H. Iman-Eini, and A. Marzoughi, "DC link voltage balancing approach for cascaded H-bridge active rectifier based on selective harmonic elimination-pulse width modulation," *IET Power Electronics*, Vol. 8, No. 4, pp. 583-590, Apr. 2015.

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