JPE 17-3-11

https://doi.org/10.6113/JPE.2017.17.3.686
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

An Analysis of the Limit Cycle Oscillation in Digital PID Controlled DC-DC Converters

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Abstract

Due to the wide use of electronic products, digitally controlled DC-DC converters are attracting more and more attention in recent years. However, digital control strategies may introduce undesirable Limit Cycle Oscillation (LCO) due to quantization effects in the Analog-to-Digital Converter (ADC) and Digital Pulse Width Modulator (DPWM). This results in decreases in the quality of the output voltage and the efficiency of the system. Meanwhile, even if the resolution of the DPWM is finer than that of the ADC, LCO may still exist due to improper parameters of the digital compensator. In order to discover how LCO is generated, the state space averaging model is applied to derive equilibrium equations of a digital PID controlled DC-DC converter in this paper. Furthermore, the influences of the parameters of the digital PID compensator, and the resolutions of the ADC and DPWM on LCO are studied in detail. The amplitude together with the period of LCO as well as the corresponding PID parameters are obtained. Finally, MATLAB/Simulink simulations and FPGA verifications are carried out and no-LCO conditions are obtained.

Key words: DC-DC Buck converter, Digital PID control, LCO, Quantization effects

I. INTRODUCTION

Digitally controlled DC-DC converters are widely used in electronic products owning to the following advantages: flexible programmability, low noise sensitivity, easy to implement and so on [1]-[6]. LCO may be introduced into a system due to quantization effects in the ADC and DPWM module, which is a kind of nonlinear low frequency oscillation [7]-[12]. The LCO in digitally controlled DC-DC converters is attracting more and more attention because it seriously degrades the quality of output voltage and the efficiency of systems.

In 2003, V. Peterchev and S. R. Sanders proposed three conditions to eliminate the LCO in PID controlled DC-DC converters, though corresponding verifications were not done [13]. Static and dynamic models including quantization effects were established in 2004, and some no-LCO conditions were proposed [14]. However, the input signals of the quantizers must be sinusoidal, which severely restricts the application of the models. W. Stefanutti et al. established a model of a voltage-mode converter that includes a digital PID compensator, and the probability of LCO in the system was predicted by a statistical method [15]. Then W. Stefanutti et al. proposed a new LCO forecasting method based on incremental energy, and the no-LCO boundary was estimated [16]. However, complexity and low accuracy are the drawbacks of this method. In 2012, Mark Bradley et al. studied the LCO in a digital PI controlled DC-DC buck converter. The magnitude and frequency expressions of the LCO were given and the characteristics of the LCO on two duty-cycle levels and multiple duty-cycle levels were analyzed [17], [18]. However, the absence of experimental verifications is a shortcoming of this study. Some scholars have studied three conditions to avoid LCO in digital PID controlled DC-DC Buck converters [19]. However, the specific forms of LCO and the influence factors were not analyzed in detail. These shortcoming will be addressed in this paper.

This paper focus on the modeling of digital PID controlled DC-DC converters and discovering the reasons why LCO exist in digital DC-DC converters. Meanwhile, the specific forms and influence factors of LCO are analyzed in detail. Furthermore, simulations and experimental verifications are carried out. Accurate system modeling, an analysis of the forms of LCO and discussions of the influence factors of LCO are included in section II. Section III presents a Simulink model of the system and the related simulation results. FPGA verifications are described in section IV, and

Manuscript received Aug. 9, 2016; accepted Jan. 20, 2017
Recommended for publication by Associate Editor Se-Kyo Chung.
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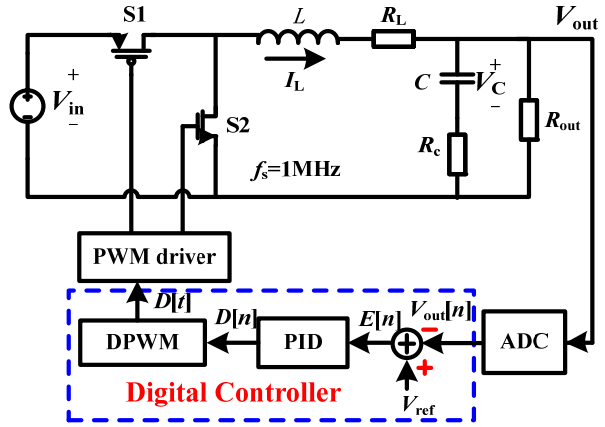


Fig. 1. Diagram of a digital PID controlled DC-DC Buck converter.

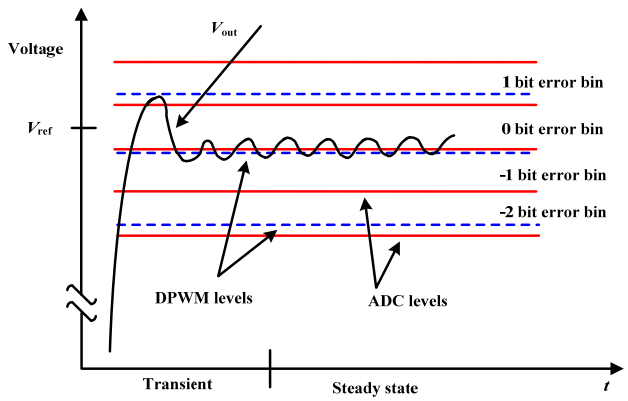


Fig. 2. LCO resulted from low resolution DPWM and a relatively high resolution ADC.

TABLE I
PARAMETERS OF THE DC-DC BUCK TOPOLOGY

Parameters	Values
V_{in}	3.6-5.0V
V_o	1.8V
T_s	1μs
I_{load}	0-1A
L	4.7μH
C	10μF
R_L	0.2Ω
R_C	0.1Ω

section V summarizes the main ideas of this paper.

II. MODELING OF THE SYSTEM AND ANALYSIS OF LCO

A schematic diagram of a digital PID controlled Buck converter is presented in Fig. 1, and the parameters adopted in this paper are listed in Table I. Due to the quantization effects in the ADC and in the DPWM module, there may be a case where the steady state output voltage cannot match the zero-error bin of the ADC. As a consequence, the output voltage periodically oscillates near the zero-error bin of the ADC. A typical waveform of LCO is shown in Fig. 2.

A. Modeling of Digital PID Controlled DC-DC Buck Converter

The state space averaging model of the system shown in Fig. 1 can be written as:

$$\begin{pmatrix} \frac{dV_{out}(t)}{dt} \\ \frac{dI_L(t)}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{R_{out}}{R_{out}+R_c}\left(\frac{R_c}{L}+\frac{1}{R_{out}C}\right) & \frac{R_{out}}{R_{out}+R_c}\left(\frac{1}{C}-\frac{R_cR_L}{L}\right) \\ -\frac{1}{L} & -\frac{R_L}{L} \end{pmatrix} \begin{pmatrix} V_{out}(t) \\ I_L(t) \end{pmatrix} + \begin{pmatrix} \frac{R_{out}R_c}{L(R_{out}+R_c)} \\ \frac{1}{L} \end{pmatrix} V_{in}\sigma \quad (1)$$

where σ is the switching signal, $\sigma = 1$ means that the switch S_1 is on, and $\sigma = 0$ means that the switch S_2 is off.

Let $X = \begin{pmatrix} V_{out}(t) \\ I_L(t) \end{pmatrix}$,

$$A = \begin{pmatrix} -\frac{R_{out}}{R_{out}+R_c}\left(\frac{R_c}{L}+\frac{1}{R_{out}C}\right) & \frac{R_{out}}{R_{out}+R_c}\left(\frac{1}{C}-\frac{R_cR_L}{L}\right) \\ -\frac{1}{L} & -\frac{R_L}{L} \end{pmatrix},$$

$B = \begin{pmatrix} \frac{R_{out}R_c}{L(R_{out}+R_c)} \\ \frac{1}{L} \end{pmatrix}$, then the system model can be rewritten as:

$$\frac{d}{dt}X(t) = AX(t) + BV_{in}\sigma \quad (2)$$

Obviously, σ is equal to 1 during $(0, DT_s]$ and 0 during $[DT_s, T_s]$. The solution of above equation is:

$$\begin{aligned} X(T_s) &= e^{A(T_s-DT_s)}\{e^{ADT_s}X(0) + \int_0^{DT_s} e^{(DT_s-\tau)A}Bd\tau V_{in}\} \\ &= e^{AT_s}X(0) + e^{A(T_s-DT_s)}\int_0^{DT_s} e^{(DT_s-\tau)A}Bd\tau V_{in} \end{aligned} \quad (3)$$

where $X_0=X(0)$ represents the state matrix at the beginning of a switching period, and $X_1=X(T_s)$ represents the state matrix at the end of a switching period. Let $N(D) = e^{A(1-D)T_s}\int_0^{DT_s} e^{(DT_s-\tau)A}Bd\tau$ and $X_1 - X^* = e^{AT_s}(X_0 - X^*)$, then equation (3) can be transformed as:

$$\begin{aligned} X_1 &= e^{AT_s}X_0 + N(D)V_{in} \\ &= e^{AT_s}X_0 + (I - e^{AT_s})X^* \end{aligned} \quad (4)$$

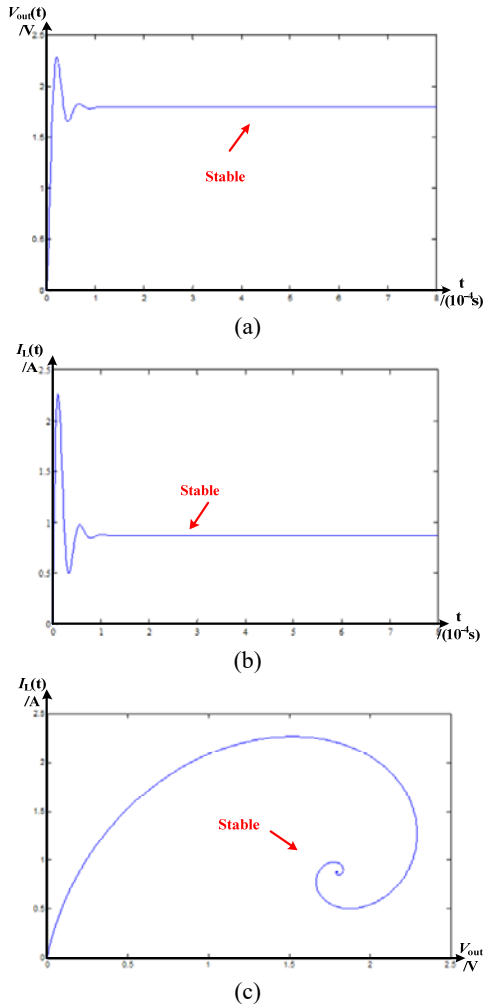
where X^* represents the equilibrium point of a DC-DC Buck converter, which can be expressed as:

$$X^* = (I - e^{AT_s})^{-1}N(D)V_{in} \quad (5)$$

Therefore, the equilibrium point X^* can be calculated according to the duty ratio D in the steady state, and the value of D determines the value of X^* of the system. If X^* is unique (i.e. D is unique), the state matrix $X(t)$ of the system is:

$$X(t) = e^{At}X(0) + (I - e^{At})X^* \quad (6)$$

Waveforms of the output voltage and inductor current as



(a) (b) (c)

Fig. 3. Waveforms of the output voltage. (a) the inductor current (b) and the corresponding phase portrait in the V_{out}-I_L plane (c) when the equilibrium point is unique. The parameters are listed in Table I except for D = 103/256 and Q_{dpwm} = 1/256.

well as the corresponding phase portrait are shown in Fig. 3, where the switching ripple is ignored to make the plots clearer. It can be seen form Fig. 3 that the system is stable when the equilibrium point is unique without any other external disturbance and that the phase portrait in the V_{out}-I_L plane is a convergent spiral.

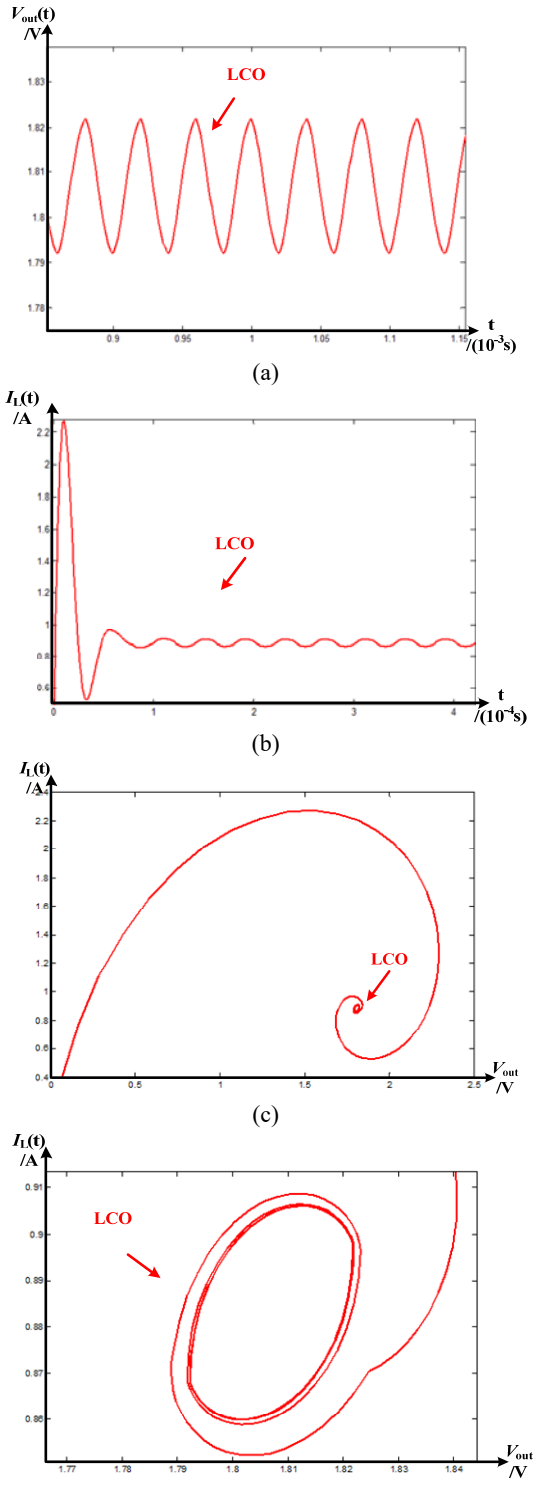
If the system has two equilibrium points X_1^* and X_2^*, the switching point when the equilibrium point switches from X_1^* to X_2^* is P_2, and the switching point when the equilibrium point switches from X_2^* to X_1^* is P_1. In addition, the value of the state matrix is $X(n)$ at the point of P_1 and it is $X(n+1)$ at the point of P_2. The following condition must be satisfied according to equation (5), which is:

$$X(t) = e^{A(t-nT_s)}X(n) + (I - e^{A(t-nT_s)})X_1^* \quad (7)$$

From P1 to P2, the state matrix can be expressed as:

$$X(t) = e^{A(t-(n+1)T_s)}X(n+1) + (I - e^{A(t-(n+1)T_s)})X_2^* \quad (8)$$

In this situation, waveforms of the output voltage and inductor current as well as the corresponding phase portrait in



(a) (b) (c) (d)

Fig. 4. Waveforms of the output voltage (a), the inductor current (b), the corresponding phase portrait in the V_{out}-I_L plane (c) and a partially enlarged version (d) under the condition of two equilibrium points. The parameters are consistent with those in Fig. 3 except for D_1=104/256 and D_2=103/256.

the V_{out}-I_L plane are shown in Fig. 4. It is obvious that the system exhibits LCO when the equilibrium point is not unique and that the phase portrait in the V_{out}-I_L plane is

approximately circular in the steady state. Similarly, it can be deduced that when the number of equilibrium points continues to grow, LCO occurs on multiple duty-cycle levels.

In summary, the number of equilibrium points is equal to the number of values for the duty ratio, and the system is stable if there is only one equilibrium point, while LCO exists with two or more equilibrium points. If there are n values of the duty ratio in the system, the output voltage possesses LCO on n duty-cycle levels, and the specific situation of the LCO can be analyzed by the method mentioned above.

B. Analysis of the Influence Factors of LCO

One of the no-LCO conditions is presented in [20]:

$$Q_{\text{dpwm}} V_{\text{in}} < Q_{\text{adc}} \Rightarrow \frac{V_{\text{in}}}{2^{N_{\text{dpwm}}}} < \frac{V_{\text{adc,max}}}{2^{N_{\text{adc}}}} \tag{9}$$

That is:

$$N_{\text{dpwm}} > N_{\text{adc}} + \log_2\left(\frac{V_{\text{in}}}{V_{\text{adc,max}}}\right) \tag{10}$$

The input voltage V_{in} in this paper is 5V, and the reference voltage of the ADC is 2V. Therefore, equation (10) in this paper should be:

$$N_{\text{dpwm}} \geq N_{\text{adc}} + 2 \tag{11}$$

However, equation (11) is a condition which provides at least one output stage corresponding to the DPWM within the zero-error bin. Under the condition $N_{\text{dpwm}} = N_{\text{adc}}+1$, as long as there is one output stage corresponding to the DPWM and suitable PID parameters, a stable output voltage should also be provided. The conditions are shown in Fig. 5.

The following discussions are under the condition of $N_{\text{dpwm}} = N_{\text{adc}}+1$. N_{dpwm} is set to 8bits, and N_{adc} is set to 7bits (i.e. $Q_{\text{dpwm}} = 1/256$ and $Q_{\text{adc}} = 1/64$).

If there is one LSB change in the output signal of the DPWM, the corresponding variation on V_{out} should be $\Delta V_{\text{out}} = Q_{\text{dpwm}} * V_{\text{in}} = 1/256 * 5 = 1.25 * 1/64 = 1.25 Q_{\text{adc}}$, which means that it is possible for the ADC to find a suitable quantization bin to match the V_{out} in this situation, which avoids LCO.

The incremental PID algorithm is:

$$\begin{aligned}\Delta D_c[n] &= D_c[n] - D_c[n-1] \\ &= K_p(E[n] - E[n-1]) + K_i E[n] + K_d(E[n] - 2E[n-1] + E[n-2])\end{aligned} \tag{12}$$

Equation (12) shows that when the parameters of the PID algorithm are small, especially for a small integral gain K_i, LCO on the two duty-cycle levels cannot occur. Since $\Delta V_{\text{out}} = Q_{\text{dpwm}} V_{\text{in}} = 1.25 Q_{\text{adc}} < 2Q_{\text{adc}}$, the error of the output voltage lies in two adjacent error bins, it is reduced gradually and finally stabilized within the zero-error bin. As a consequence, the system eventually becomes stable. That is to say, if LCO exists in a system in this condition, it should be on three duty-cycle levels and the output voltage oscillates within the three error bins of the ADC. The diagram of output voltage in this condition is shown in Fig. 6.

If K_i continues to increase, the variation range of $D_c(n)$ is increased. When the variation of $D_c(n)$ is greater than one LSB of the DPWM, the duty cycle signal D may have three values, which leads to LCO on three duty-cycle levels. Similarly, the variation of V_{out} should be $\Delta V_{\text{out}} = 2Q_{\text{dpwm}} V_{\text{in}} = 2.5 Q_{\text{adc}}$, which means that the output voltage exists in three error bins (i.e. +1bit, 0bit, -1bit), as shown in Fig. 7.

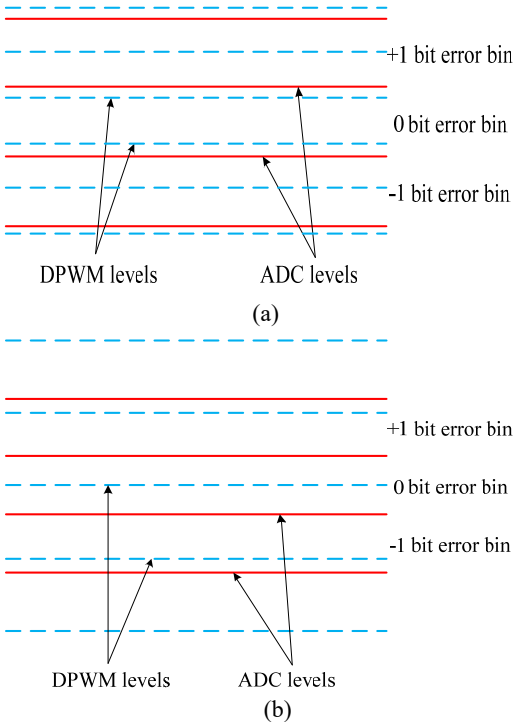


Fig. 5. Conditions of N_{dpwm} when (a) $N_{\text{dpwm}} \geq N_{\text{adc}} + 2$ and (b) $N_{\text{dpwm}} = N_{\text{adc}}+1$.

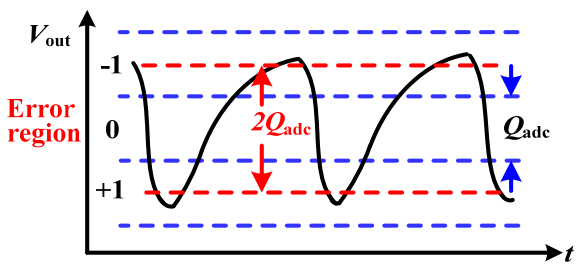
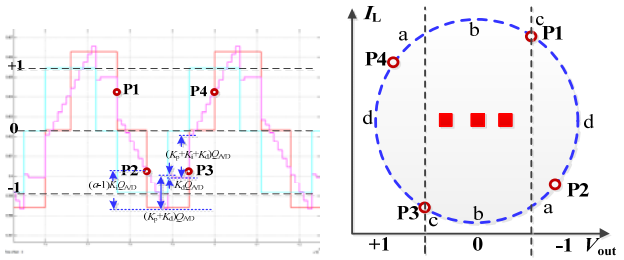


Fig. 6. LCO of output voltage on three duty-cycle levels.

Suppose that the system experiences aT_s to enter the zero-error bin from the switching point P_2, bT_s within the zero-error bin, cT_s to reach to the switching point P_3, and dT_s to reach to the switching point P_4. Where a, b, c and d are the numbers of iterations in the corresponding error bins when the system is working in the steady state. Then it is possible to obtain:

$$\begin{aligned}&(a-1)K_i Q_{\text{adc}} - (K_p + K_d)Q_{\text{adc}} + K_d Q_{\text{adc}} \\ &\approx (K_p + K_i + K_d)Q_{\text{adc}} + (K_d - K_i)Q_{\text{adc}} - (c-2)K_i Q_{\text{adc}}\end{aligned} \tag{13}$$

Therefore, if the LCO on three duty-cycle levels occurs under this condition, one of the requirements of the PID parameters is:



(a) (b)

Fig. 7. Time domain waveforms of D and $D_c(n)$ (a) as well as a sketch of the phase portrait in the V_{out}-I_L plane (b) when the LCO on the three duty-cycle levels occurs under the conditions of N_{dpwm} = 8bits and N_{adc} = 7bits.

$$\frac{K_p}{K_i} \approx \frac{a-c-1}{2} \tag{14}$$

In particular. for c = 1, it takes T_s to get to P_3 from the boundary between the "0" and "+1" error bins.

Similarly, when $D_c(n)$ changes from P_3 to P_4, there is one LSB variation of the DPWM. Then it is possible to get:

$$Q_{dpwm} - 2dK_i Q_{adc} \approx 0 \tag{15}$$

Since the peak-peak value of the output voltage is superposed by the fluctuation of the DC value of the output voltage and the voltage ripple, the peak-peak value of the output voltage when LCO occurs on the three duty-cycle levels is:

$$V_{LCO} = 2Q_{dpwm}V_{in} + V_{out,ripple} \tag{16}$$

where $V_{out,ripple}$ is the ripple of the output voltage, which can be calculated as:

$$\Delta V_{out,ripple} = \frac{V_{out}(1-D)T_s}{L}\left(\frac{T_s}{8C} + R_c\right) \tag{17}$$

In addition, the period of LCO on the three duty-cycle levels is:

$$T_{LCO} = 2(a+b+c+d)T_S \tag{18}$$

If K_i continues to increase, the error signal occupies more error bins of the ADC, LCO on four or more duty-cycle levels appears and the system eventually becomes divergent. Likewise, the peak-peak value of the output voltage when LCO on N duty-cycle levels occurs is:

$$V_{LCO} = (N-1)Q_{dpwm}V_{in} + V_{out,ripple} \tag{19}$$

Increasing K_p helps accelerate the transient response of the system, and the time when the error signal of the output voltage lies in three or more error bins of the ADC is reduced, which decreases the probability of LCO. In addition, the amplitude and period of LCO are decreased even if it still exists. Therefore, increasing K_p helps stabilize the system.

III. System Modeling and Simulation in Simulink

A Simulink model of a digital PID controlled DC-DC Buck converter is shown in Fig. 8. According to above analysis, when the parameters of the PID algorithm are small,

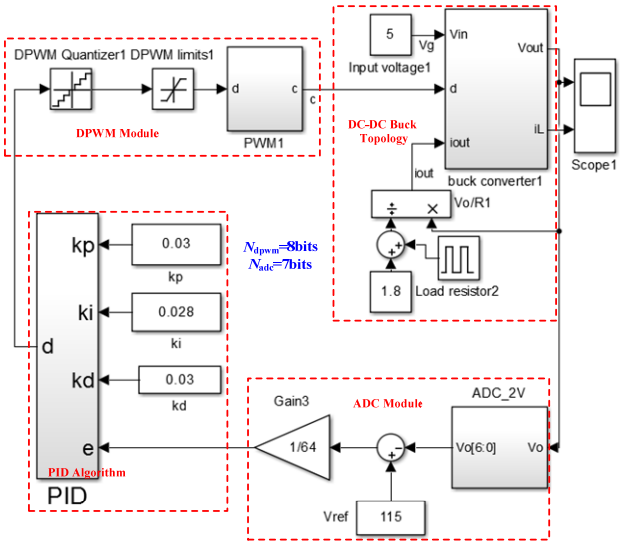
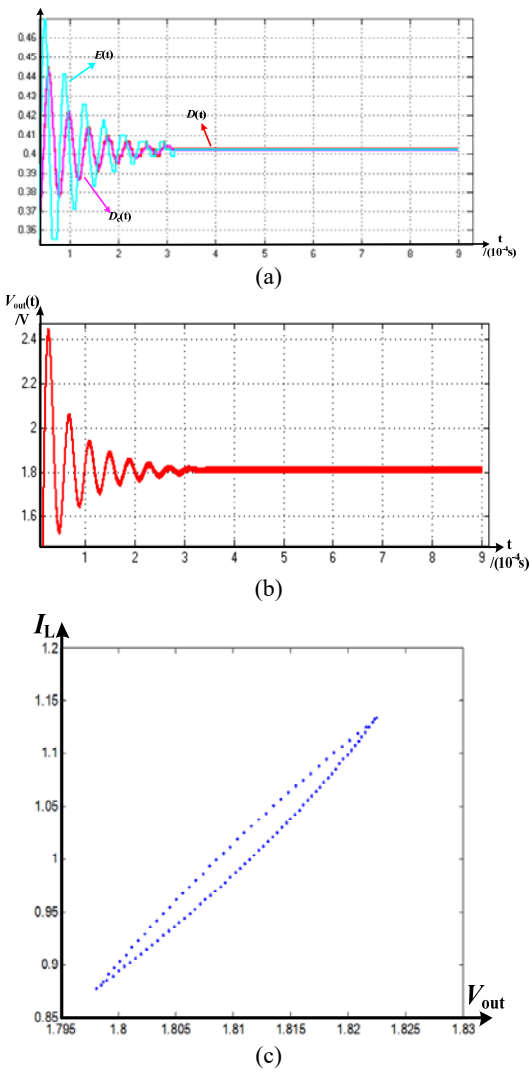


Fig. 8. Simulink model of the entire system under the conditions of N_{dpwm} = 8bits and N_{adc} = 7bits.



(a) (b) (c)

Fig. 9. Time domain waveforms of $D(t)$, $D_c(t)$ and $E(t)$ (a), the output voltage (b), and the phase portrait in the V_{out}-I_L plane (c) when the system is stable under the conditions of K_p = 0.03, K_i = 0.022 and K_d = 0.03.

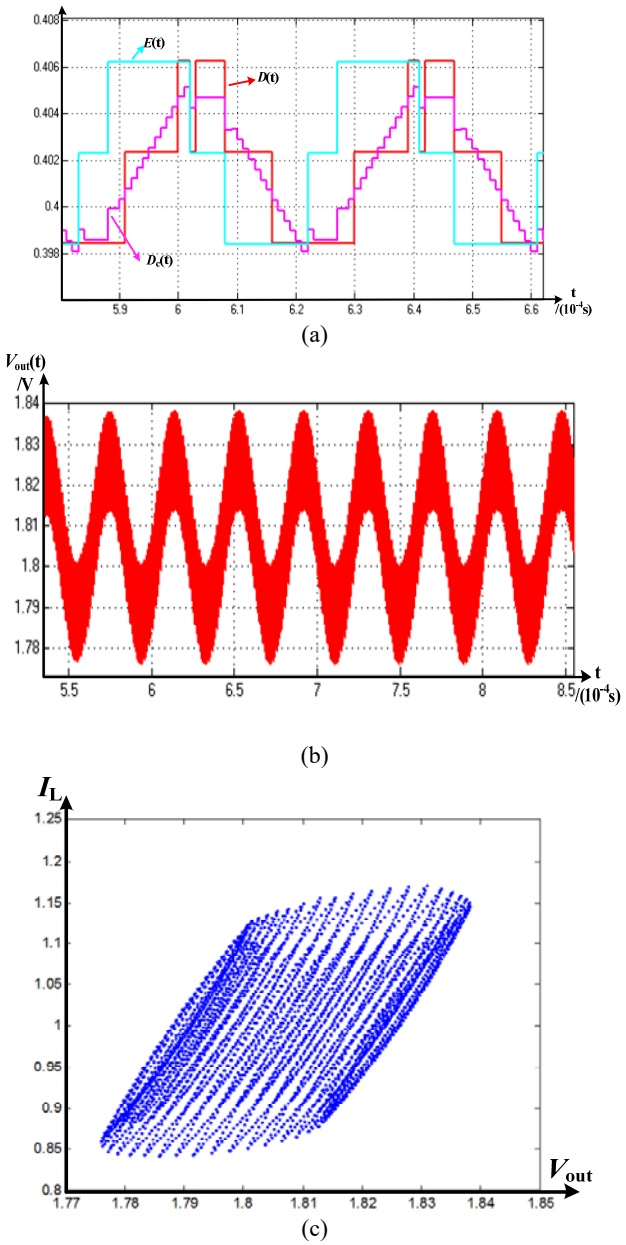


Fig. 10. Time domain waveforms of $D(t)$, $D_c(t)$ and $E(t)$ (a), the output voltage (b), and the phase portrait in the V_{out}-I_L plane (c) when LCO occurs on the three duty-cycle levels under the conditions of $K_p = 0.03$, $K_i = 0.028$ and $K_d = 0.03$.

especially for a small K_i, it is difficult for the system to achieve voltage regulation. With an increase in the PID parameters, especially for an increase of K_i, the voltage regulation can be realized. However, the transient performance is not very good. Here $K_p = 0.03$, $K_i = 0.022$ and $K_d = 0.03$ are adopted, and the corresponding simulation results are shown in Fig. 9. It can be seen from Fig.9 that the system is stable and voltage regulation can be achieved under the conditions of $N_{dpwm} = N_{adc} + 1$ and small values of the PID parameters.

When K_i increases, according to the previous analysis, LCO on the two duty-cycle levels cannot occur. However,

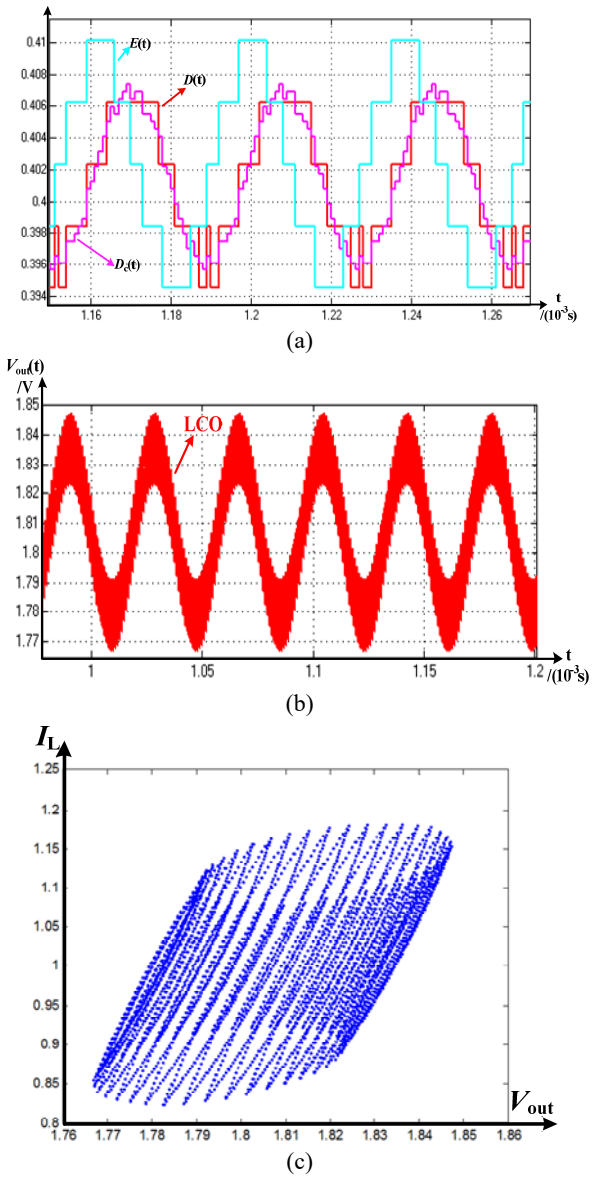


Fig. 11. Time domain waveforms of $D(t)$, $D_c(t)$ and $E(t)$ (a), the output voltage (b), and the phase portrait in the V_{out}-I_L plane (c) when LCO on the four duty-cycle levels occurs under the conditions of $K_p = 0.03$, $K_i = 0.03$ and $K_d = 0.03$.

LCO on the three duty-cycle levels exists. Here $K_p = 0.03$, $K_i = 0.028$ and $K_d = 0.03$ are adopted, and the corresponding simulation results are shown in Fig. 10. It can be seen from Fig. 10 that LCO on the three duty-cycle levels appears and that the error signal lies in three error bins of the ADC. The peak-peak value of the output voltage is approximately 62mV, and it is close to the value calculated by Equation (16), which is 64.9mV.

If K_i continues to increase, LCO on multiple duty-cycle levels exists. For example, when $K_p = 0.03$, $K_i = 0.03$ and $K_d = 0.03$, LCO on the four duty-cycle levels appears, and the error signal lies in five error bins of the ADC (see Fig. 11). It can be seen from the above analysis that when LCO on the four duty-cycle levels exists, the variation of the output

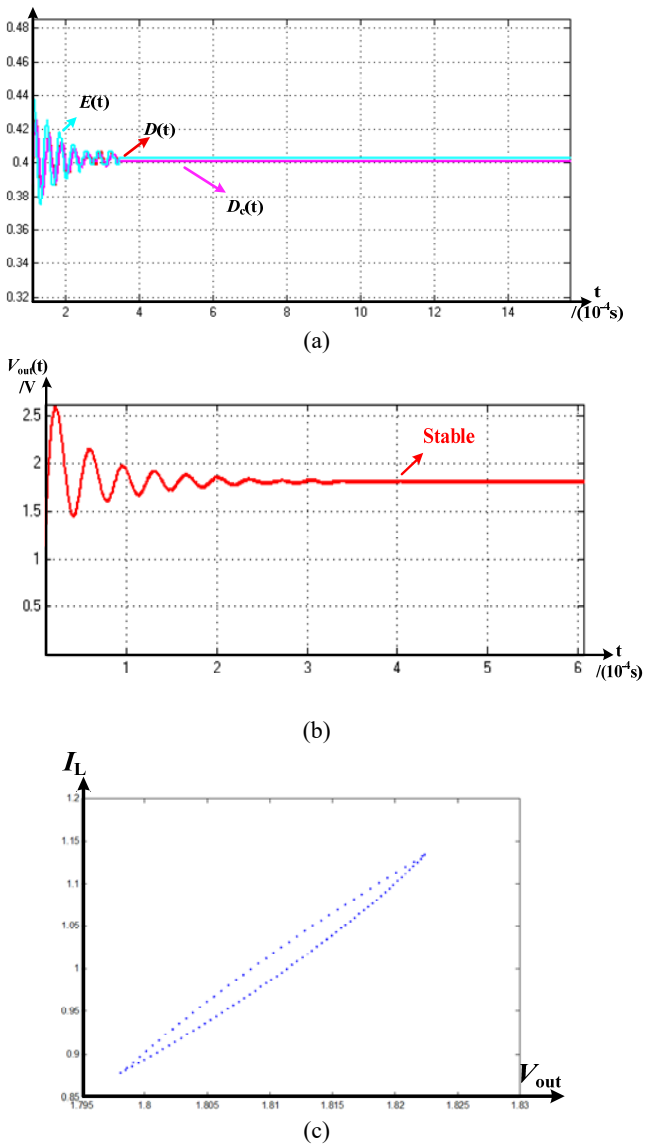


Fig. 12. Time domain waveforms of $D(t)$, $D_c(t)$ and $E(t)$ (a), the output voltage (b), and the phase portrait in the V_{out}-I_L plane (c) when the system becomes stable again under the conditions of K_p = 0.1, K_i = 0.03 and K_d = 0.03.

voltage caused by the fluctuation of the duty cycle signal is $\Delta V_{out} = 4Q_{dpwm}V_{in} = 4\times1.25Q_{adc} = 5Q_{adc}$, which means that the error signal lies in five error bins of the ADC. This is consistent with the simulation results in Fig. 11.

Increasing K_p helps stabilize the system. Here K_p = 0.1, K_i = 0.03 and K_d = 0.03 are adopted, and the corresponding simulation results are presented in Fig.12. It can be seen that the system is stable in this condition. Meanwhile, increasing K_i may lead to divergence of the system. For example, if K_p = 0.03, K_i = 0.035 and K_d = 0.03, the system is divergent, and the simulation results can be seen in Fig. 13. The simulation results in this section validate previous analysis.

IV. Experimental Verification Based on a FPGA

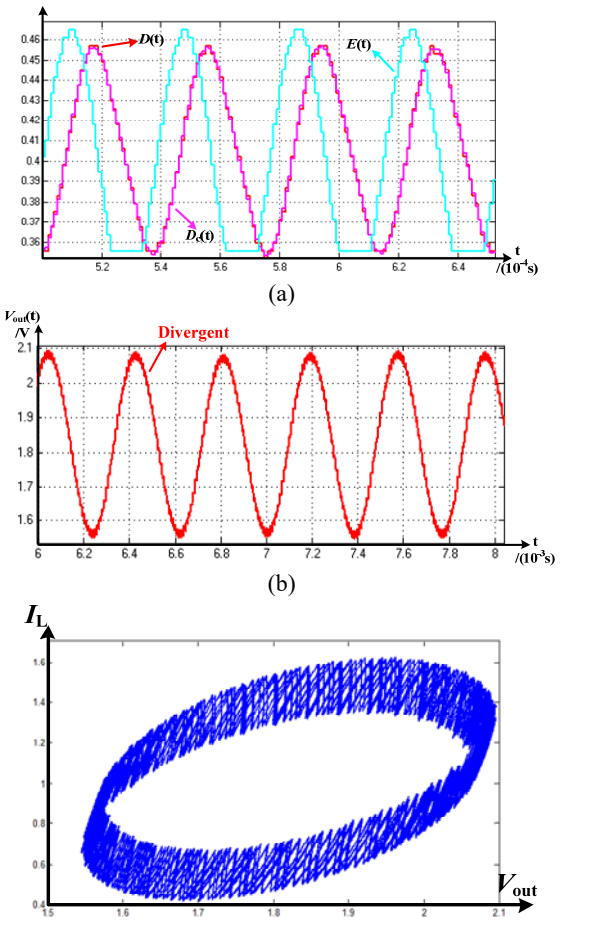


Fig. 13. Time domain waveforms of $D(t)$, $D_c(t)$ and $E(t)$ (a), the output voltage (b), and the phase portrait in the V_{out}-I_L plane (c) when the system is divergent under the conditions of K_p = 0.03, K_i = 0.035 and K_d = 0.03.

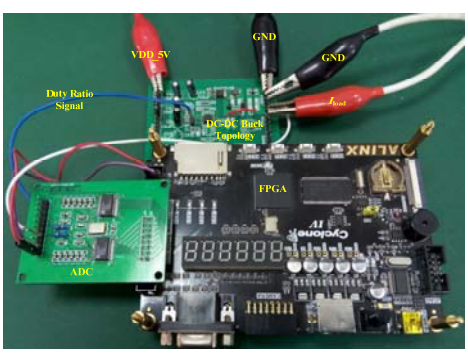
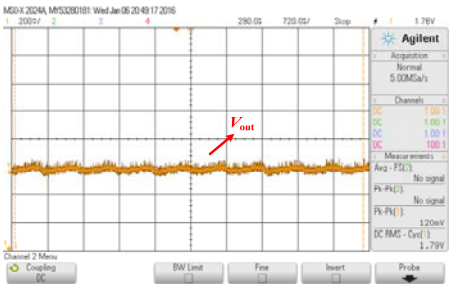
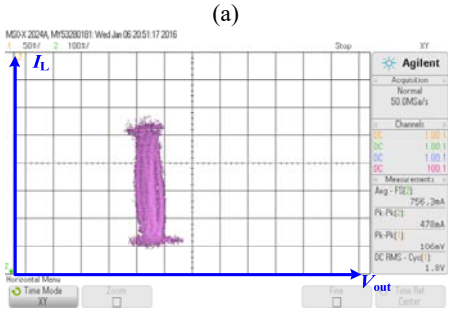


Fig. 14. Verification platform of the entire system.

The verification platform of the digital PID controlled DC-DC Buck converter is shown in Fig. 14. It is composed of a DC-DC Buck topology, an ADC and a FPGA. N_{dpwm} and N_{adc} are set to 8bits and 7bits, respectively, and the high 7-bit output signals of the ADC are linked to the FPGA as the sampling signal of V_{out}. Here K_p = 55/256, K_i = 15/256 and K_d = 25/256 are adopted, and the experimental results are shown in Fig. 15. It can be seen that LCO on the three duty-cycle levels occurs, and the phase portrait in the V_{out}-I_L plane forms

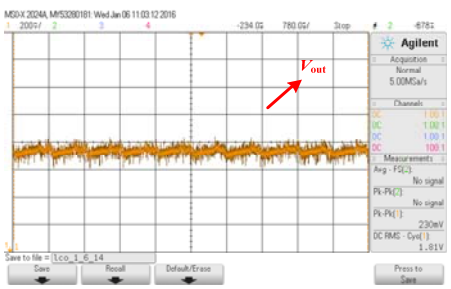


(a)

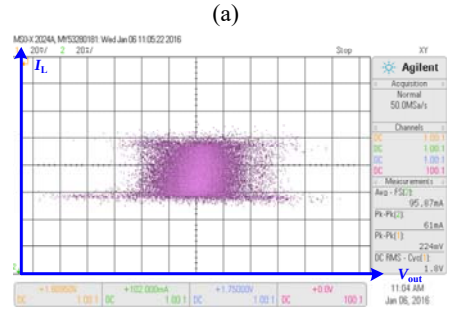


(b)

Fig. 15. Time domain waveform of V_{out} (a) and the phase portrait in the V_{out}-I_L plane (b) when LCO on the three duty-cycle levels occurs under the conditions of K_p = 55/256, K_i = 15/256 and K_d = 25/256.



(a)

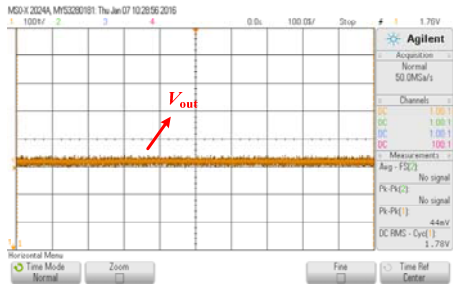


(b)

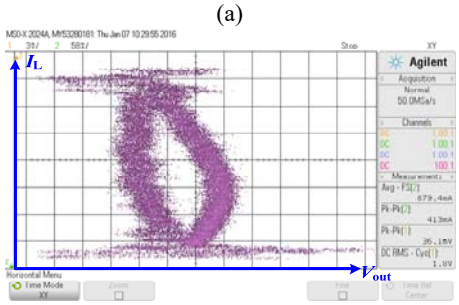
Fig. 16. Time domain waveform of V_{out} (a) and the phase portrait in the V_{out}-I_L plane (b) when LCO on multiple duty-cycle levels occurs under the conditions of K_p = 55/256, K_i = 25/256 and K_d = 25/256.

a cylindrical surface, which is basically consistent with the results presented in section III.

When K_i continues to increase, LCO on multiple duty-cycle levels occurs. Here K_p = 55/256, K_i = 25/256 and K_d = 25/256 are adopted, and the corresponding test results can be seen in Fig. 16. From these results, it can be seen that increasing K_i may lead to more duty-cycle levels of LCO or divergence of the system.



(a)



(b)

Fig. 17. Time domain waveform of V_{out} (a) and the phase portrait in the V_{out}-I_L plane (b) when the system returns to stability under the conditions of K_p = 150/256, K_i = 10/256 and K_d = 35/256.

When K_p increases, the corresponding experimental results are presented in Fig. 17. From these results, it can be seen that the system is stable and that the phase portrait in the V_{out}-I_L plane forms an oval. The results in Fig. 17 indicate that increasing K_p helps stabilize the system, which is in accordance with the conclusion proposed in section II.

V. Conclusion

This paper focused on analyzing the LCO in digital PID controlled DC-DC converters. Firstly, the state space averaging method is used to model a DC-DC Buck converter. In addition, the equilibrium equations of the system are derived and the reasons why LCO occurs are analyzed. Next, specific forms of LCO and the influences of PID parameters are discussed, under the premise that the resolution of the DPWM is one bit finer than that of the ADC. In addition, the amplitude and period of LCO as well as the corresponding parameters of the PID algorithm are presented. Finally, MATLAB/Simulink simulations and FPGA verifications are carried out to validate the effectiveness of the theoretical analysis.

It is found that the higher the resolution of the DPWM is, when compared with that of the ADC, the lower the probability of LCO becomes. Furthermore, increasing K_p is helpful for stabilizing the system, while LCO on multiple duty-cycle levels or divergence can occur due to an excessive increase of K_i. Fortunately, if the resolution of the DPWM is one bit higher than that of the ADC, and the parameter of K_p is relatively high with a relatively low value of K_i, LCO can be avoided. This provides a useful guidance for the design of the PID related digital compensators in DC-DC converters.

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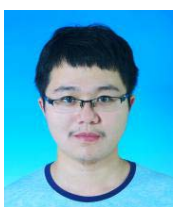

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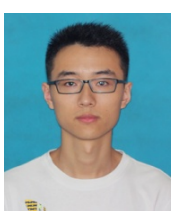

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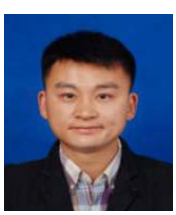

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