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A Hybrid Filtering Stage Based Quasi-type-1 PLL under Distorted Grid Conditions

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Abstract

For three-phase synchronization applications, the synchronous reference frame phase-locked loop (SRF-PLL) is probably the most widely used technique due to its ease of implementation and satisfactory phase tracking performance under ideal grid conditions. However, under unbalanced and distorted grid conditions, its performance tends to worsen. To deal with this problem, a variety of filtering stages have been proposed and used in SRF-PLLs for the rejection of disturbance components at the cost of degrading the dynamic performance. In this paper, to improve dynamic performance without compromising the filtering capability, an effective hybrid filtering stage is proposed and incorporated into the inner loop of a quasi-type-1 PLL (QT1-PLL). The proposed filtering stage is a combination of a moving average filter (MAF) and a modified delay signal cancellation (DSC) operator in cascade. The time delay caused by the proposed filtering stage is smaller than that in the conventional MAF-based and DSC-based PLLs. A small-signal model of the proposed PLL is derived. The stability is analyzed and parameters design guidelines are given. The effectiveness of the proposed PLL is confirmed through experimental results.

Key words: Moving average filter, Phase locked loop, Synchronization

I. INTRODUCTION

Proper synchronization with the utility grid is one of the most important control aspect for many grid-connected applications [1]. For three-phase power systems, the SRF-PLL is probably the most widely used synchronization technique owing to its simple structure and satisfactory performance under ideal grid conditions [2]. However, under unbalanced and distorted grid conditions, the phase-tracking performance of the SRF-PLL is significantly degraded owing to the existence of a fundamental frequency negative sequence (FFNS) voltage component and harmonic sequence voltage component [3].

To deal with this problem, low-pass filters (LPFs) are integrated into the inner-loop of the SRF-PLL to mitigate the influence of FFNS and harmonics components [4]. However, to provide a satisfactory disturbance rejection capability, the cutoff frequency of the LPF needs to be rather low, which results in a slow dynamic response speed [5]. A compromise must be made between the speed of the response and the disturbance rejection capability. Moreover, a LPF cannot totally eliminate the disturbance, which means that the phase-tracking error remains. To improve the dynamic performance of LPF-based PLLs, a variety of advanced PLLs (DSOGI-PLL [6], DDSRF-PLL [7], MSOGI-PLL [8], MCCF-PLL [9], [10], etc.) have been presented. The filtering stages of these PLLs can be divided into two parts. The first part, which act as a notch filter, is responsible for eliminating the FFNS. The second part, which plays the role of a LPF, is used to mitigate the other dominant disturbances. Since the FFNS is eliminated, the cutoff frequency of the LPF can be increased. Although the dynamic performance of these PLLs are improved, the LPF-based PLLs can attenuate but not totally eliminate all of the dominant harmonic components [11]. To completely filter out all of the dominant disturbances without degrading the dynamic performance, many nonlinear filtering techniques, such as MAF and DSC, have been utilized in SRF-PLLs.

Since the MAF can act as an ideal filter at a specific frequency by setting its window length (T_ω), the MAF-PLL

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becomes one of the most widely used PLLs [12]. When compared with a LPF, the MAF can completely eliminate the FFNS and dominant harmonics components [13]. Since the filtering capability of the MAF directly depends on the value of T_ω, the time delay caused by the MAF cannot be reduced, which slows down the transient response of the MAF-PLL [14]. To overcome this weakness, a hybrid filtering stage based PLL referred to as the differential MAF-PLL (DMAF-PLL) was presented in [15]. A special proportional component is incorporated into the filtering stage of the conventional MAF-PLL to eliminate the FFNS. The MAF in the hybrid filtering stage is responsible for rejecting the other dominant harmonics. Since the FFNS is blocked out by the proportional component instead of the MAF in the conventional MAF-PLL, T_ω of the MAF is reduced from 0.01s to 0.0033s. This method greatly improves the dynamic performance of the MAF-PLL. However, under a phase jump condition, a large overshoot of the frequency estimation error occurs, which can cause an undesirable disconnection of renewable power sources [16], [17]. This is unacceptable in many grid-connected applications. To achieve satisfactory dynamic performance, a quasi-type-1 PLL (QT1-PLL) with a new control structure was proposed in [18]. The QT1-PLL has a hybrid type-1/type-2 PLL structure. It acts as a type-1 control system when the grid frequency is at its nominal value. When the grid frequency is not at its nominal value, it becomes a type-2 control system. Hence, it can provide a faster transient response without worsening the filtering capability, when compared with type-2 PLLs [19]. However, the window length of the MAF (0.01s) is still not reduced.

Recently, many studies have introduced a delayed signal cancellation (DSC) operator into PLLs to improve the filtering capability [20]-[25]. Similar to the MAF, the DSC can also completely block certain frequency components if proper conditions hold [26]. However, unlike the MAF, the DSC does not have the capability to attenuate other disturbances, which means that a single DSC cannot eliminate all of the dominant harmonic components and cannot effectively immune high frequency noise. To overcome this weakness, the majority of existing DSC-based PLLs make their filtering stage act as a LPF by cascading multiple DSC blocks with different time delay factors. However, the time delay introduced by the filtering stage becomes the sum of the delays of all the DSC blocks, which significantly increases the settling time of the PLL. Moreover, the implementation complexity and computational burden are also increased.

The main objective of this paper is to present a hybrid filtering stage based PLL that provides satisfactory dynamic performance without degrading its filtering capability. The hybrid filtering stage consists of a single modified DSC (MDSC) and MAF in cascade, which is incorporated into the inner loop of the QT1-PLL structure. The modified DSC and MAF are responsible for eliminating different disturbance components. Since T_ω of the MAF is reduced from 0.01s to 1/600s and the delay of the MDSC is small, the proposed PLL can achieve a fast dynamic response. A small-signal model of the proposed PLL is derived for stability analysis and parameter design. The effectiveness of the proposed PLL is validated through experimental results.

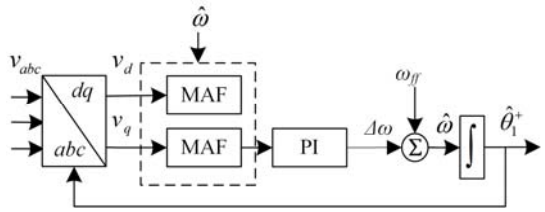

Fig. 1. Block diagram of a three-phase MAF-PLL.

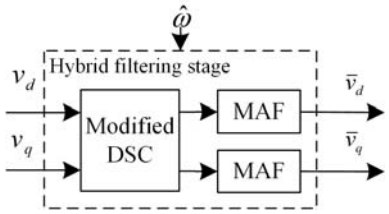

Fig. 2. Block diagram of the proposed hybrid filtering stage.

TABLE I
DOMINANT HARMONIC COMPONENTS OF GRID VOLTAGE

Harmonic order	…	-11	-5	-1	+1	+7	+13	…
$\alpha\beta$-frame (Hz)	…	-550	-250	-50	50	350	650	…
Harmonic order	…	-12	-6	-2	0	+6	+12	…
dq-frame (Hz)	…	-600	-300	-100	0	300	600	…

II. HYBRID FILTERING STAGE IN THE PROPOSED PLL

In this section, the dominant voltage sequence components of a distorted grid are analyzed first. Then, the hybrid filtering stage is presented and analyzed in detail.

A. Analysis of Voltage Sequence Component

For a three-phase power system, the dominant voltage disturbance sequence components in the stationary reference frame ($\alpha\beta$-frame) are the non-triplen odd harmonic components (e.g. $1st^-$, $5th^-$, $7th^+$, $11th^-$, $13th^+$, etc.) [27]. After applying a *Park* transformation, the dominant disturbance components become even harmonics (i.e. $2nd^-$, $6th^\pm$, $12th^\pm$, etc.) in the synchronous reference frame (dq-frame) [28]. The fundamental frequency positive sequence (FFPS) component becomes a DC component in the dq-frame. The dominant voltage sequence components in most practical applications are listed in Table I.

It should be mentioned that the frequencies of the voltage sequence components can be negative, since the value of frequency represents the rotating speed of the voltage sequence vector in the $\alpha\beta$-frame or the dq-frame. For negative sequence components (i.e. $1st^-$, $5th^-$,$11th^-$, etc.), their voltage vectors rotate counterclockwise and their frequency values are negative

(i.e., -50Hz, -250Hz, -550Hz, etc.).

B. Hybrid Filtering Stage

Fig. 2 shows a block diagram of the proposed hybrid filtering stage. $\hat{\omega}$ is the estimation of the grid frequency. Since the entire hybrid filtering stage is arranged in the inner loop after a *Park* transformation, all of the disturbances are eliminated in the *dq*-frame rather than the *αβ*-frame. MAFs (T_ω=1/600s) and Modified DSC (MDSC) are responsible for eliminating different set of disturbance components.

The s-domain transfer function of the conventional DSC in its general form is as follows:

$$DSC_n(s)=\frac{1+e^{j2\pi/n}e^{-(T/n)s}}{2} \tag{1}$$

where n is the delay factor, and T is the grid fundamental period. n is the only parameter in the conventional DSC. In the proposed hybrid filtering stage, the MDSC is expressed as follows:

$$MDSC(s)=\frac{1+e^{j2\pi/n_s}e^{-(T/n)s}}{2} \tag{2}$$

where n_s is the shift factor, and n is the delay factor. Unlike the DSC, the required filtering performance can be achieved by selecting two parameters in a more flexible way. The frequency characteristic of the DSC can be shifted by using different n_s. The time-domain implementation of the MDSC is shown in Fig.3, which is similar to the conventional DSC. In this paper, n_s and n of the MDSC are 1 and 4, respectively. The transfer function of the MDSC can be expressed as:

$$MDSC(s)=\frac{1+e^{-(T/4)s}}{2} \tag{3}$$

Hence, the time domain implementation shown in Fig.3 can be simplified as shown in Fig.4. Fig.5 shows Bode diagrams of the MDSC and the DSC_4. It can be observed that the MDSC shifts the Bode plots of the DSC_4 by n_s and that the MDSC can completely eliminate the components at ±100Hz, ±300Hz, ±500Hz, etc.

As presented in many studies [12-15], the transfer function of the MAF is as follows:

$$MAF(s)=\frac{1-e^{-T_\omega s}}{T_\omega s} \tag{4}$$

In this paper, T_ω is set to 1/600 s. Hence, the MAF used in this paper can eliminate ±600Hz, ±1200Hz, ±1800Hz, etc. The entire hybrid cascaded filtering stage can be obtained as:

$$\begin{aligned} H(s)&=MDSC(s)MAF(s)\\ &=\frac{1+e^{-(T/4)s}}{2}\frac{1-e^{-T_\omega s}}{T_\omega s} \end{aligned} \tag{5}$$

where T=0.02 is a grid period, and T_ω = 1/600s.

Fig. 6 shows the frequency response of $H(s)$. Bode diagrams of two SOGI based filtering stage are shown in Fig. 6. It can be seen that $H(s)$ can provide zero gain at the frequency of the dominant disturbances (-100H, ±300Hz, ±600Hz, etc.) as listed in Table I. $H(s)$ also provides a unity gain and zero phase delay at 0Hz (the frequency of the FFPS in the *dq*-frame). However, the SOGI based PLL can only attenuate most of these disturbances. However, it cannot eliminate them completely. The DSOGI [6] can only eliminate the -100Hz component.

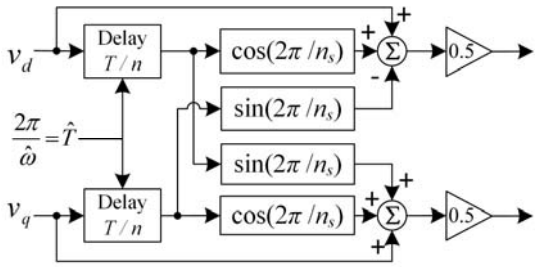

Fig. 3. Time-domain implementation of the MDSC.

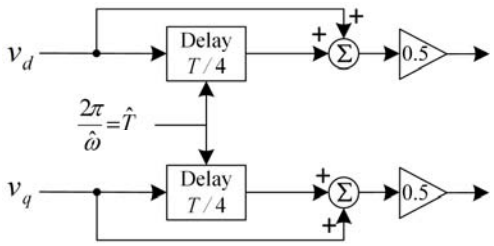

Fig. 4. Simplified implementation of the MDSC with n_s=1, n=4.

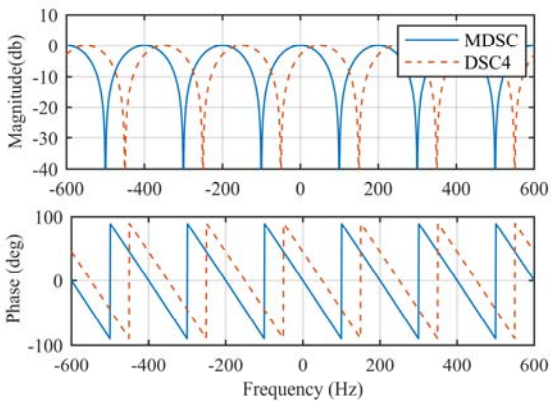

Fig. 5. Bode diagrams of the MDSC (solid lines) and the DSC_4 (dashed lines).

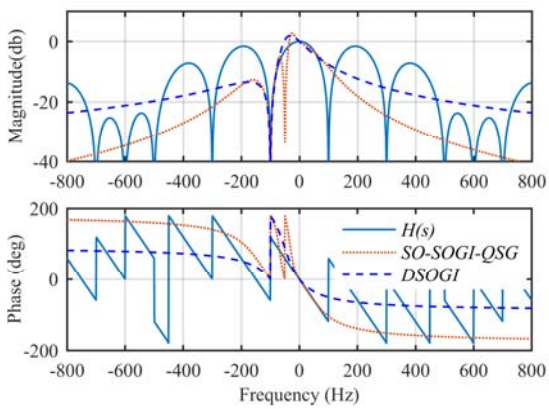

Fig. 6. Bode diagrams of the hybrid filtering stage $H(s)$.

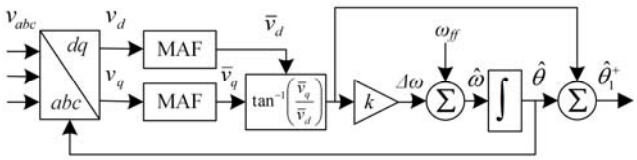

Fig. 7. Block diagram of the QT1-PLL.

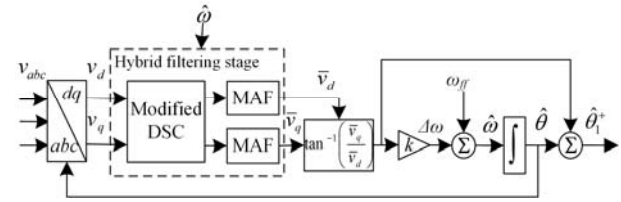

Fig. 8. Block diagram of the proposed PLL.

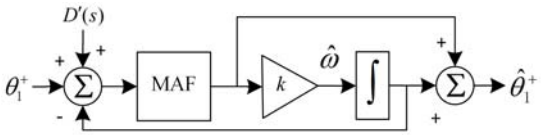

Fig. 9. Small-signal model of the QT1-PLL.

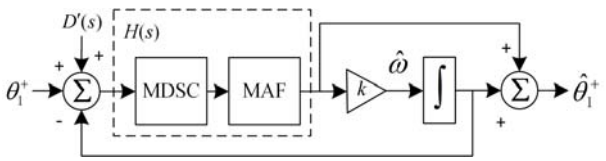

Fig.10. Small-signal model of the proposed PLL.

Although the SO-SOGI-QSG [36] can remove the -100Hz and -50Hz (dc component in the $\alpha\beta$-frame), the computational burden is doubled since the SO-SOGI-QSG is made up of two SOGI units in cascade. If other disturbances need to be eliminated, more SOGI units have to be incorporated into the SO-SOGI-QSG. Compared with other dominant disturbance components, the dc component is small and not addressed in this paper. If necessary, many existing dc-offset rejection methods [37] can be easily used. For the sake of brevity, this is not presented here.

III. The Proposed PLL and Parameter Design Guidelines

In this section, the proposed PLL structure is introduced. A small-signal model of the proposed PLL is derived. Then parameter design guidelines are given. Finally, the accuracy of the small-signal model is examined by simulation results.

A. Description of the Proposed PLL

The proposed PLL is derived from the QT1-PLL structure [18]. Fig.7 shows a block diagram of the QT1-PLL. In Fig.7. $\boldsymbol{v}_{abc}$ and ω_{ff} represent the three-phase voltage and the nominal angular frequency of the FFPS, respectively. $\hat{\omega}$ is the estimation of the grid frequency. $\hat{\theta}_1^+$ is the phase estimation of the FFPS. k is the only control parameter. All of the disturbances are eliminated in the dq-frame. By replacing the MAF in the QT1-PLL with the hybrid filtering stage presented in the previous section, the proposed PLL is obtained as shown in Fig. 8.

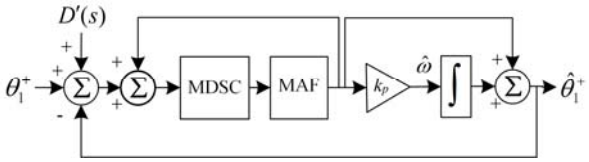

Fig. 11. Simplified model of the proposed PLL.

B. Small-signal model

The difference between the proposed PLL and the QT1-PLL is the filtering stage. Hence, a small-signal model of the proposed PLL can be conducted from the model of the QT1-PLL (as shown in Fig. 9) [18]. $D'(s)$ is the disturbance component in the dq-frame, which is listed in Table I. θ_1^+ is the phase of the FFPS. The detailed derivation of this model of the QT1-PLL can be found in [7], and is not presented here for the sake of brevity. By Substituting $H(s)$ for the MAF, the small-signal model of the proposed PLL is obtained and shown in Fig. 10. The accuracy of this model is evaluated by simulation at the end of section III.

C. Parameter Design Guidelines

The parameters of the hybrid filtering stage are already selected in section II. The time delay in the MDSC and T_ω in the MAF are 0.005s and 1/600s, respectively. k is the only parameter to be designed in this section.

By applying block diagram algebra, the small-signal model shown in Fig. 10 can be transformed into a standard form of a close-loop feedback system, as shown in Fig. 11 [18]. The corresponding open-loop transfer function is:

$$G_{ol}(s)=\frac{\hat{\theta}_1^+(s)}{\theta_1^+(s)-\hat{\theta}_1^+(s)}=\left(\frac{MDSC(s)MAF(s)}{1-MDSC(s)MAF(s)}\right)\left(\frac{s+k}{s}\right) \tag{6}$$

Hence, the phase tracking error transfer function is:

$$G_e(s)=\frac{\theta_e(s)}{\theta_1^+(s)}=\frac{\theta_1^+(s)-\hat{\theta}_1^+(s)}{\theta_1^+(s)}=\frac{1}{1+G_{ol}(s)} \tag{7}$$

where $\theta_e(s)$ is phase tracking error. According to equation (7), the phase-error Laplace transform in response to a phase step jump ($\Delta\theta$) is obtained as:

$$\Theta_e^{\Delta\theta}(s)=\frac{\Delta\theta}{s}G_e(s) \tag{8}$$

In addition, the phase-error Laplace transform in response to a frequency step change ($\Delta\omega$) is:

$$\Theta_e^{\Delta\omega}(s)=\frac{\Delta\omega}{s^2}G_e(s) \tag{9}$$

To achieve optimal dynamic performance under both phase jump and frequency step change conditions, the inverse Laplace transform is applied to (8) and (9) to evaluate the settling time of the proposed method. Variations of 2% of the

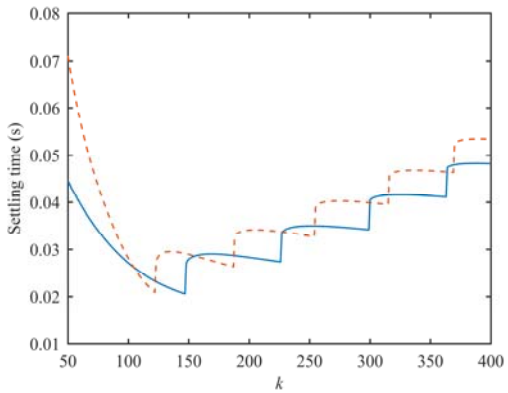

Fig. 12. 2% settling time of the proposed PLL as a function of k for both the phase jump (solid line) and the frequency step change (dashed line).

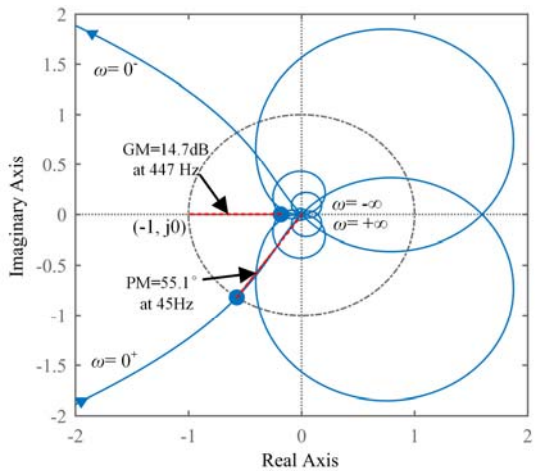

Fig. 13. Nyquist curve for $G_{ol}(s)$.

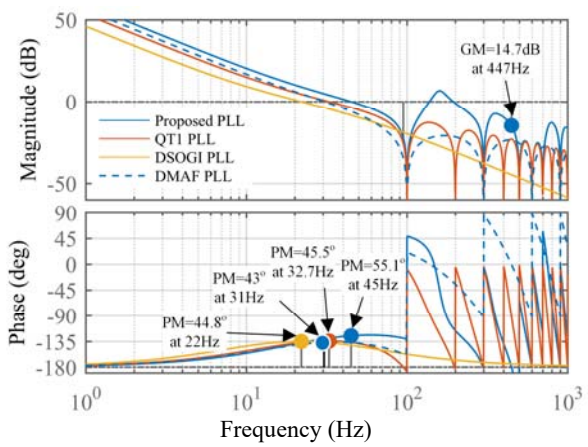

Fig. 14. Open-loop Bode diagram of the proposed PLL and three other PLLs.

settling time as a function of k are shown in Fig. 12. In this paper, k is chosen to be 124. The corresponding settling time is around one grid period. Since time delay elements are included in equation (6), the open-loop transfer function is not a minimum-phase system. Hence, the stability cannot be confirmed from the Bode diagram. The Nyquist stabilization criterion is used in this paper to judge the system stability. Fig. 13 shows the Nyquist curve for $G_{ol}(s)$. It can be observed that the Nyquist curve for $G_{ol}(s)$ does not encircling the (-1, j0) point. The corresponding feedback system of $G_{ol}(s)$ is stable. The minimum phase stability margin (PM) is 55.1° at 45 Hz. The minimum gain stability margin (GM) is 14.7 dB at 447 Hz.

Fig. 14 shows an open-loop bode diagram of the proposed PLL and three other PLLs. It can be observed that the crossover frequency of the proposed PLL is larger than that in the other PLLs. Owing to this, the proposed PLL provides a faster transient response. The phase margin of the proposed PLL is also larger. Moreover, all of the MAF based PLLs can completely eliminate the dominant disturbances in Table I. However, the DSOGI PLL can only attenuate them. It should be noted that a Bode diagram cannot judge the stability of a non-minimum-phase system. The stability of the proposed PLL is confirmed through the Nyquist curve in Fig. 13.

Although the bode plot of the proposed PLL at a high frequency is little higher than the other PLL, it is still able to attenuate high frequency noise. The capability of the noise immunity is confirmed by simulation in response to grid voltage polluted by white noise as shown in Fig.15. The white noise is 20% of the three-phase voltage, which is large enough for the simulation. It can be observed that the frequency estimation error and the phase tracking error are zero. The proposed PLL is immune to the high frequency noise.

D. Accuracy of Small-signal Model

To examine the accuracy of the small-signal model, a simulation is carried out under a phase jump of +40° and a frequency step change of +5Hz. A performance comparison between the proposed PLL and its small-signal model is depicted in Fig. 16. As shown in Fig.16, the small-signal model can precisely describe the behavior of the proposed PLL in terms of both its estimated frequency and phase tracking error.

IV. Experimental Results

In this section, experimental results are presented to verify the effectiveness of the proposed PLL. The experiments are based on a TMS320F28335 digital signal controller. A programmable arbitrary wave form generator is employed to generate 50Hz three-phase distorted voltages. The sampling frequency of the implemented PLL is 10 kHz. The Adams-Bashforth method [29] is employed to avoid the algebraic loop and to ensure the discrete accuracy of the implementation. The continuous-integrals is approximated by:

$$\frac{1}{s} \Leftrightarrow \frac{T_s}{12}\frac{23z^{-1}-16z^{-2}+5z^{-3}}{1-z^{-1}} \tag{10}$$

For comparison, several advanced PLLs based on the MAF and DSC are also implemented in experiments. The QT1-PLL [18] is implemented since the proposed PLL is based on the quasi-type-1 structure. The DMAF-PLL [15] is implemented because its filtering stage is hybrid and based on the MAF. The EGDSC-PLL [26] is implemented since its filtering stage is

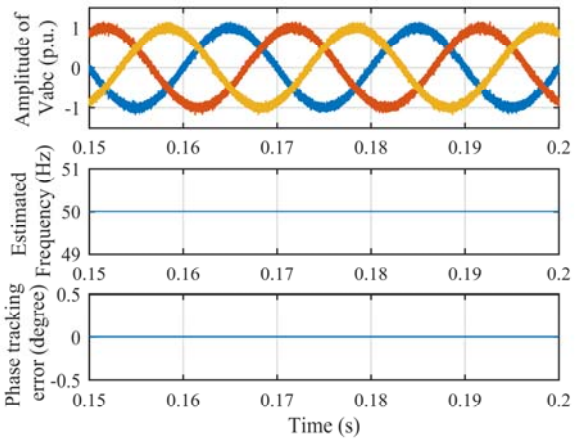

Fig. 15. Simulation results when the grid voltages are polluted by white noise.

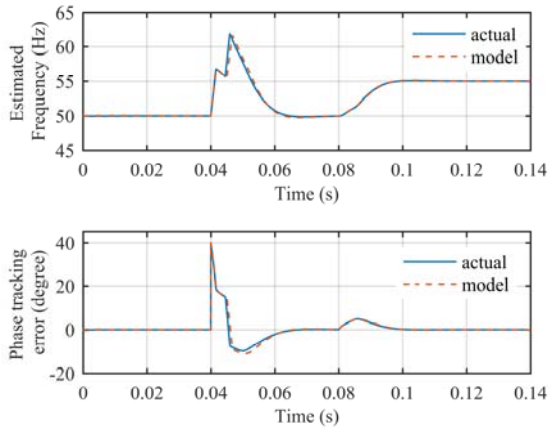

Fig. 16. Performance comparison between the proposed PLL and its small-signal model under a phase jump of +40° at 0.04s and a frequency step jump of +5 Hz at 0.08s.

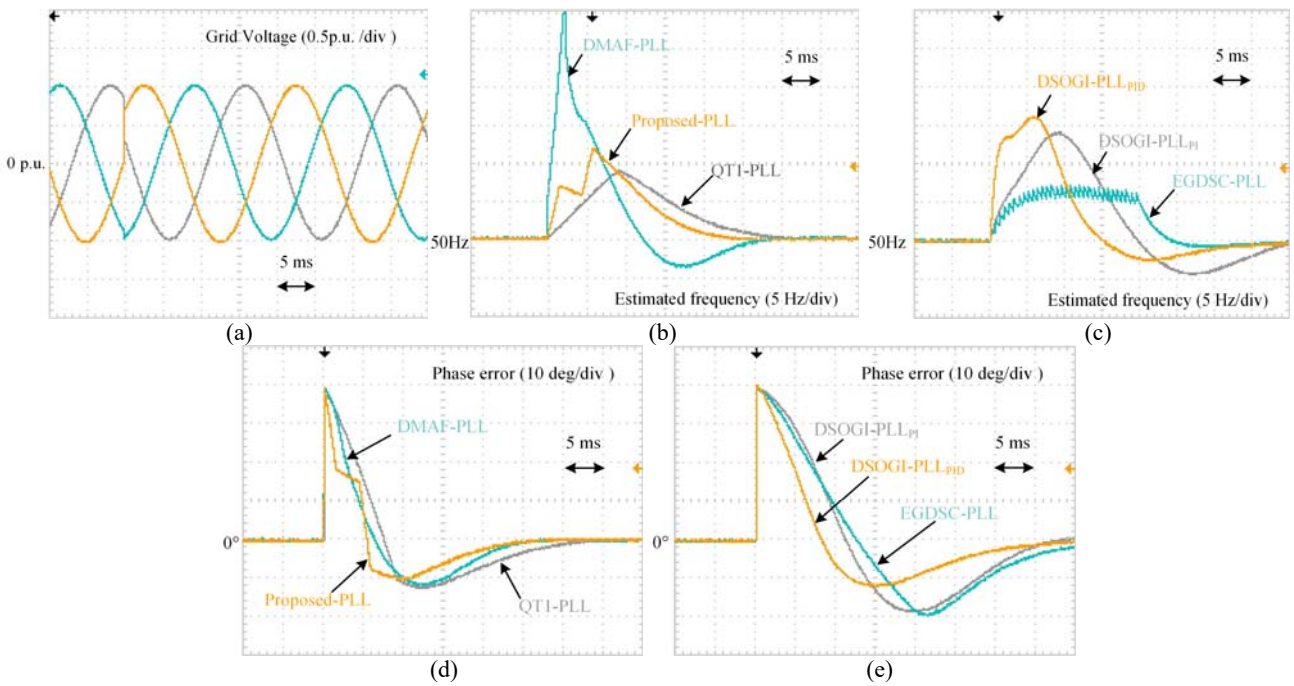

Fig. 17. Experimental results in response to a phase jump of 40°. (a) Grid voltages. (b) Estimated frequency of the proposed PLL, QT1-PLL and DMAF-PLL. (c) Estimated frequency of EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$. (d) Phase error of the proposed PLL, QT1-PLL and DMAF-PLL. (e) Phase error of EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$.

based on the DSC. Since the SOGI based PLL is a mature technique in PLLs, the DSOGI-PLL$_{PI}$ [6] and DSOGI-PLL$_{PID}$ [10] are also implemented. All of these PLLs were published in the past three years. To be fair, all of the MAFs in PLLs are adaptive.

A. Phase Jump

Fig. 17 shows experimental results when the input voltage undergoes a phase jump of +40°. It is observed that the settling time of the proposed PLL is around 1.2 cycles of the nominal frequency, which is shorter than that of the other PLLs'. The DMAF also provides satisfactory dynamic response. However, the estimated frequency of the DMAF has an overshoot of over 30 Hz owing to the differential operation in its filtering stage. This may violate the frequency limit in some grid codes [30]. This may cause the incorrect disconnection of equipment from the grid [31]. The settling times of the QT1-PLL and the EGDSC-PLL are 31ms and over 40ms, respectively. The settling time of the DSOGI-PLL$_{PID}$ and the DSOGI-PLL$_{PI}$ are around 40ms. According to statements in the German standard [32], the Spanish grid code [33] and other grid codes [34] [35], the estimation of voltage phase and frequency should be carried out within 25ms to fulfill the restrictive requirement in terms of dynamic response. Thus, the QT1-PLL, EGDSC-PLL and two SOGI based PLLs are not eligible under such conditions.

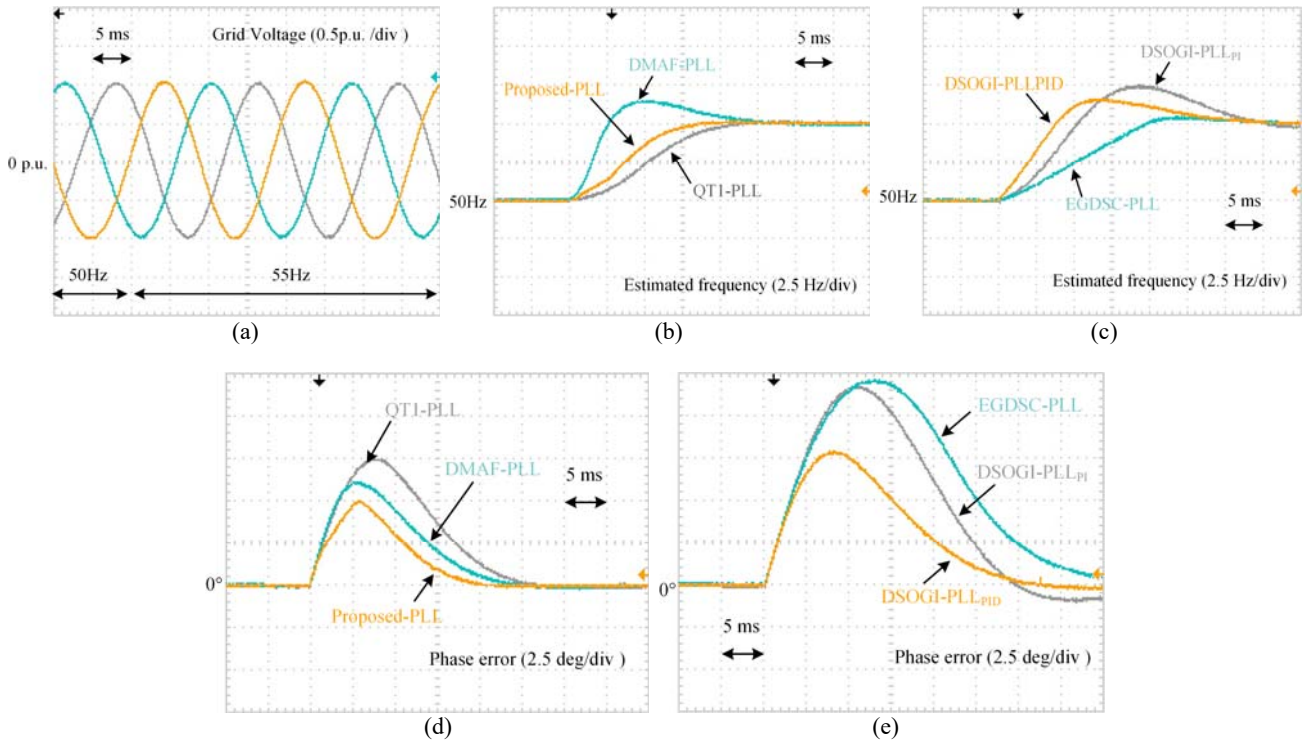

Fig. 18. Experimental results when the grid voltage undergoes a frequency step change of +5Hz: (a) Grid voltages. (b) Estimated frequency of the proposed PLL, QT1-PLL and DMAF-PLL. (c) Estimated frequency of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$. (d) Phase error of the proposed PLL, QT1-PLL and DMAF-PLL. (e) Phase error of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$.

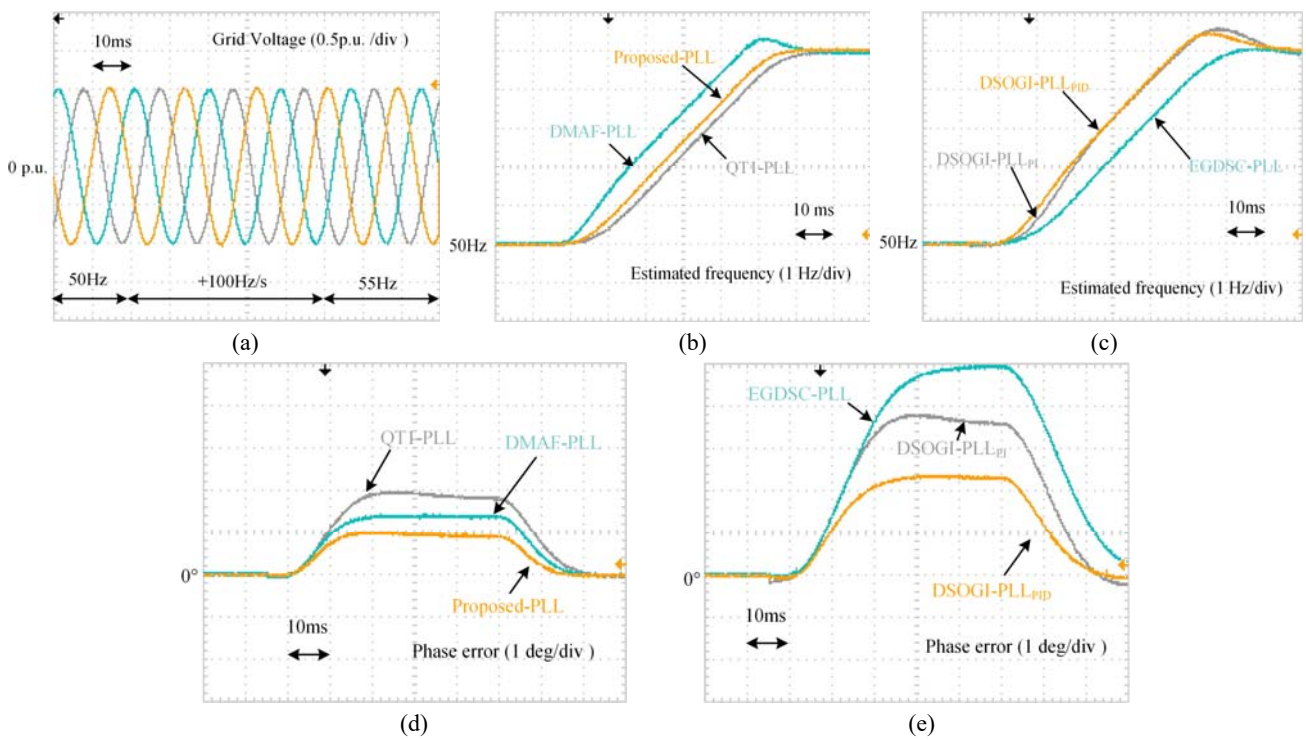

Fig. 19. Experimental results when the grid voltage undergoes a frequency ramp change of +100Hz/s: (a) Grid voltages. (b) Estimated frequency of the proposed PLL, QT1-PLL and DMAF-PLL. (c) Estimated frequency of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$. (d) Phase error of the proposed PLL, QT1-PLL and DMAF-PLL. (e) Phase error of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$.

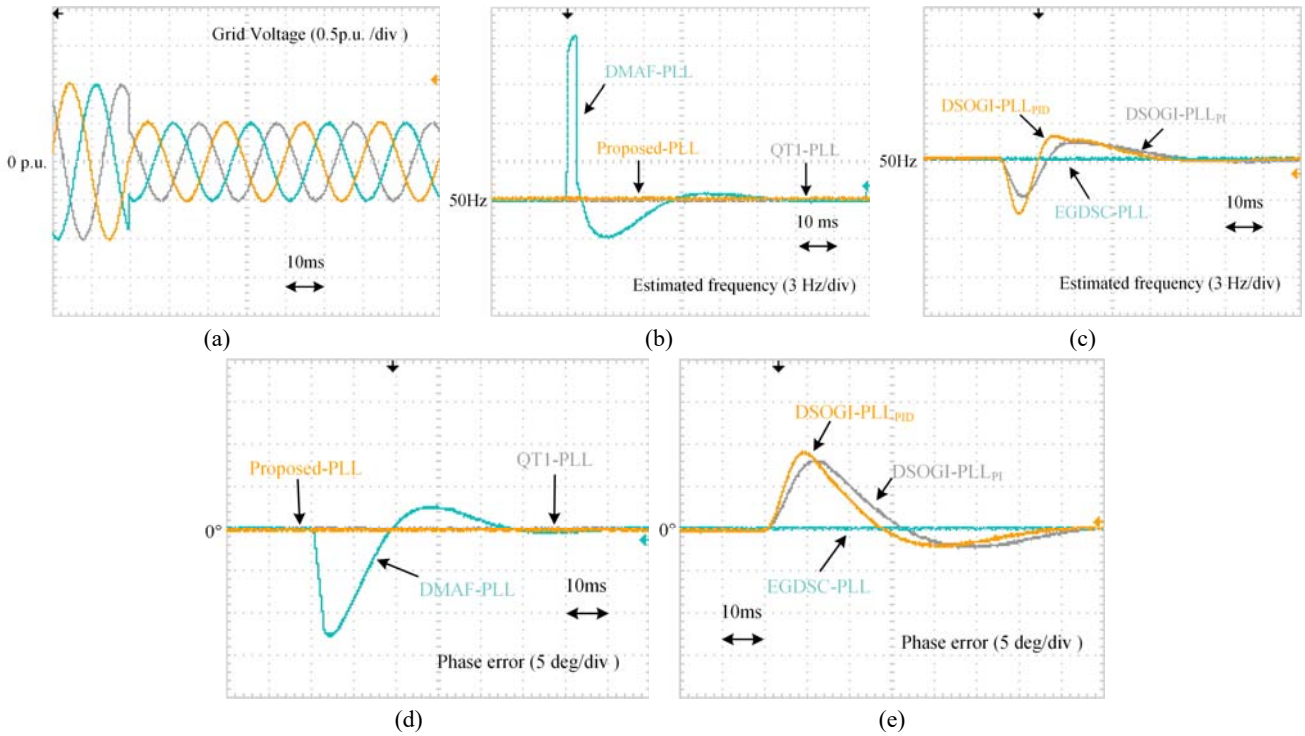

Fig. 20. Experimental results when the grid voltage undergoes voltage sag of 0.5 p.u.: (a) Grid voltages. (b) Estimated frequency of the proposed PLL, QT1-PLL and DMAF-PLL. (c) Estimated frequency of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$. (d) Phase error of the proposed PLL, QT1-PLL and DMAF-PLL. (e) Phase error of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$.

B. Frequency Step Change

Fig. 18 shows experimental results when the input voltage undergoes a frequency step change from 50Hz to 55Hz. As shown in Fig.18 (b), the proposed PLL tracks the frequency of the grid voltage in 17ms which is the shortest time among the other PLLs. Furthermore, the phase error of the proposed PLL decays to zero in 20ms. The DMAF and QT1-PLL also provide good dynamic frequency tracking performance. The settling time of the EGDSC-PLL in the phase error is over 40ms, which cannot satisfy the grid code requirements. In terms of frequency overshoot, the DMAF and EGDSC-PLL have +1.6Hz and +0.5Hz peak frequency deviations. On the other hand, the proposed PLL and QT1-PLL do not have frequency overshoots. In this test, the transient responses of two SOGI based PLLs in the estimated frequency and phase error are slower than the other methods. Moreover, the frequency overshoot of these two PLLs are over 2Hz.

C. Frequency Ramp Change

The performance of the PLLs under frequency a ramp change for 50ms with a ramp rate of +100Hz/s is also evaluated in Fig. 19. The frequency of the grid voltages increases from 50Hz. After 50ms, the frequency becomes 55Hz.

It can be observed that the proposed PLL has the least phase-tracking error of 1° during the frequency ramp change. The phase-tracking errors of the DMAF-PLL and QT1-PLL are 1.4° and 1.9°, respectively. On the other hand, the phase-tracking error of the other three PLLs are larger. The EGDSC-PLL has the largest phase error at over 5°.

D. Voltage Sag

Fig. 20 illustrates the performance of the PLLs under a utility voltage sag of 0.5 p.u. Due to the operating of the arc tangent, the estimated frequency and phase error of the proposed PLL, the QT1-PLL and the EGDSC-PLL are not affected during the voltage sag condition. The dependence of the amplitude of the voltage is removed by the arc tangent operation. The DMAF has a +13Hz overshoot in its estimated frequency which may violate various grid codes. The SOGI based PLLs also have a frequency overshoot of about 5Hz. The experimental results can be found in Table III.

E. Unbalanced and Distorted Grid Voltages

Fig. 21 evaluates the detection accuracy of the PLLs when the grid voltage is unbalanced and distorted. The polluted grid voltage undergoes a frequency step change of +5Hz. The parameters of the grid voltages are summarized in Table II. Since the MAF and MDSC used in these PLLs is adaptive, the proposed PLL can completely eliminate oscillations under the nominal frequency (50Hz) and 55Hz. The DMAF-PLL and QT1-PLL can also achieve a zero steady-state phase-tracking error. Since several DSCs are used in the EGDSC-PLL and they are not adaptive, a 2Hz and 1° oscillation occur in the estimated frequency and phase-error, respectively. A solution

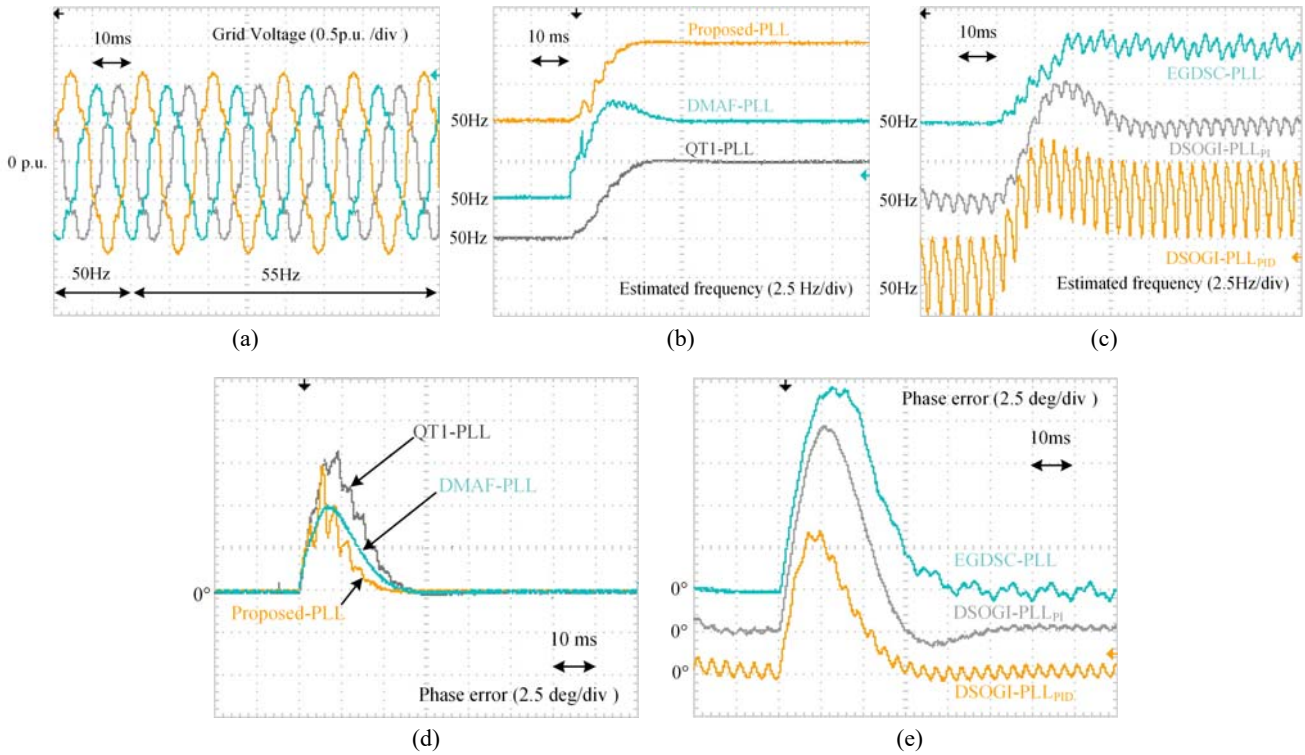

Fig. 21. Experimental results when the grid voltage is unbalanced and distorted with a frequency step change of +5Hz: (a) Grid voltages. (b) Estimated frequency of the proposed PLL, QT1-PLL and DMAF-PLL. (c) Estimated frequency of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$. (d) Phase error of the proposed PLL, QT1-PLL and DMAF-PLL. (e) Phase error of the EGDSC-PLL, DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$.

TABLE II
PARAMETERS OF THE GRID VOLTAGES

Voltage component (in the $\alpha\beta$-frame)	**Amplitude (p.u.)**
Fundamental positive sequence	1
Fundamental negative sequence	0.1
5th harmonic negative sequence	0.1
7th harmonic positive sequence	0.05
11th harmonic negative sequence	0.05
13th harmonic positive sequence	0.05

to remove these oscillation is to make the DSCs adaptive at the cost of increasing the computational burden. The SOGI based PLLs also suffer from this drawback. Since the SOGI filtering technique can only attenuate but not eliminate disturbances, the phase errors are much larger at both nominal and off-nominal frequencies. This weakness do not exist in other PLLs.

F. Summary of Experimental Results

All of the experimental results are summarized in Table III. By observing these results, the performance of all six PLLs are assessed in three aspects: transient response, filtering capability and peak frequency deviation.

The proposed PLL provides a satisfactory dynamic performance. Its settling time is shorter than the other five PLLs. It can also completely eliminate the dominant disturbance components. The phase tracking performance is immune to voltage sags. Compared with the other PLLs', a tie peak frequency deviation under a +40° phase jump is also acceptable.

The settling time of the DMAF-PLL is longer than the proposed PLL. On the other hand, it is shorter than the other methods. However, when the grid voltages are under a voltage sag, it takes the DMAF-PLL 2 cycles to track the phase again. Another drawback is the fact that a peak frequency deviation under a +40° phase jump is too large for grid-connected applications. This may be caused by a differential operation in its filtering stage.

The QT1-PLL has the smallest peak frequency deviation. Its performance also cannot be affected by voltage sag. However, its transient response is comparatively slow.

Compared with other PLLs, the performances of the DSOGI-PLL$_{PID}$ and DSOGI-PLL$_{PI}$ are unsatisfactory in terms of dynamic performance and filtering capability. Their transient responses are also too slow. Moreover, they are not able to eliminate all of the dominant harmonic components in Table I, which is a critical defect for grid-connected applications.

TABLE III
SUMMARY OF THE RESULTS

	QT1-PLL	DMAF-PLL	EGDSC-PLL	DSOGI-PLL$_{PI}$	DSOGI-PLL$_{PID}$	Proposed PLL
+40° **phase jump**						
2% settling time	≈ 1.5 cycles	≈ 1.25 cycles	≈ 2.1 cycles	≈ 2.4 cycles	≈ 1.75 cycles	≈ **1.2 cycles**
Peak phase-error	12.2° (30.6%)	11.5° (28.8%)	19.5° (33%)	19° (46.8%)	11.4° (28.5%)	**9.7° (24%)**
Peak frequency deviation	-8.9 Hz	-33.8 Hz	**-7.2 Hz**	-14 Hz	-16.1 Hz	-11.7 Hz
+5 Hz **frequency step change**						
2% settling time of the estimated frequency	≈ 1.6 cycles	≈ 1.3 cycles	≈ 2 cycles	≈ 2.6 cycles	≈ 1.74 cycles	**≈ 0.9 cycles**
Peak phase-error	7.6°	6.1°	12.2°	12.5°	7.9°	**5°**
Peak frequency deviation	**0Hz (0%)**	1.6 Hz (32%)	0.5Hz (10%)	2.5 Hz (50%)	1.6 Hz (32%)	**0Hz (0%)**
+100Hz/s **frequency ramp change**						
Phase-error	1.9°	1.4°	>5°	4°	2.3°	**1°**
0.5 p.u. **voltage sag**						
1° settling time of the phase-error	**0 cycle**	≈ 2 cycles	**0 cycle**	≈ 3.3 cycles	≈ 2.7 cycles	**0 cycle**
Peak phase-error	**0°**	-12.7°	**0°**	8°	9.2°	**0°**
Peak frequency deviation	**0 Hz**	13 Hz	**0 Hz**	-3 Hz	-4.4 Hz	**0 Hz**
Unbalance and distortion at 55 Hz						
Peak-to-peak phase-error	**0°**	**0°**	1°	0.2°	0.7°	**0°**
Peak-to-peak frequency error	**0 Hz**	**0 Hz**	2 Hz	1.1 Hz	4.5 Hz	**0 Hz**
Phase margin	45°	43°	**≈55°**	42.6°	**≈55°**	**≈55°**

V. CONCLUSIONS

In this paper, a hybrid filtering stage based PLL is proposed to estimate the frequency and phase of grid voltage under unbalanced and distorted grid conditions. By replacing the MAF in the QT1-PLL with the proposed hybrid filtering stage, which consists of the MDSC and MAF in cascade, the dynamic performance of the proposed PLL is improved without deteriorating the disturbance rejection capability. The effectiveness of the proposed PLL is evaluated through experimental results. The performance is compared with recently published advanced PLLs. Comparative results show that the proposed PLL provides the fastest transient response and good filtering capability. In addition, it is insensitive to voltage amplitude change.

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REFERENCES

[1] L.-Y. Yang, C.-L. Wang, J.-H. Liu, and C.-X. Jia, "A novel phase locked loop for grid connected converters under non-ideal grid conditions," *Journal of Power Electronics*, Vol. 15, No. 1, pp. 216-226, Jan. 2015.

[2] Z. Luo, M. Su, Y. Sun, Z. Liu, and M. Dong, "First-order generalized integrator based frequency locked loop and synchronization for three-phase grid-connected converters under adverse grid conditions," *Journal of Power Electronics*, Vol. 16, No. 5, pp. 1939-1949, Sep. 2016.

[3] Y. Li, D. Wang, W. Han, S. Tan, and X. Guo, "Performance improvement of quasi-type-1 pll by using a complex notch filter," *IEEE Access*, Vol. 4, pp. 6272-6282, Oct. 2016.

[4] H.-J. Choi, S.-H. Song, S.-G. Jeong, J.-Y. Choi, and I. Choy, "Enhanced dynamic performance during voltage disturbance," *Journal of Power Electronics*, Vol. 11, No. 3, pp. 369-374, May 2011.

[5] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Design and tuning of modified power-based pll for single phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3639-3650, Aug. 2012.

[6] P. Rodriguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *Proc. IEEE Power Electron. Spec. Conf.*, pp. 1-7, 2006.

[7] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, Vol. 22, No. 2, pp. 584-592, Mar. 2007.

[8] P. Rodriguez, A. Luna, I. Etxeberria, J. R. Hermoso, and R. Teodorescu, "Multiple second order generalized integrators for harmonic synchronization of power converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, pp. 2239-2246, 2009.

[9] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1194-1204, Apr. 2011.

[10] S. Golestan, M. Monfared, and F. D. Freijedo, and J. M. Guerrero, "Performance improvement of a prefiltered synchronous-reference-frame pll by using a PID-type loop filter," *IEEE Trans. Power Electron.*, Vol. 61, No. 7, pp. 3469-3479, July. 2014.

[11] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 765-778, Feb. 2013.

[12] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes and J. Doval-Gandoy, "PLL with MAF-based prefiltering stage: small-signal modeling and performance enhancement," *IEEE Trans. Power Electron.*, Vol. 31, No. 6, pp. 4013-4019, June. 2016.

[13] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, M. Monfared, "Moving average filter based phase-locked loop: performance analysis and design guidelines," *IEEE Trans. Power Electron.*, Vol. 29, No. 6, pp. 2750-2763, June. 2014.

[14] S. Golestan, J. M. Guerrero, A. M. Abusorrah, "MAF-PLL with phase-lead compensator," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 6, pp. 3691-3695, June. 2015.

[15] Jinyu Wang, Jun Liang, Feng Gao, Li Zhang, and Zhoudi Wang, "A method to improve the dynamic performance of moving average filter-based pll," *IEEE Trans. Power Electron.*, Vol. 30, No. 10, pp. 5978-5990, Oct. 2015.

[16] L. Hadjidemetriou, E. Kyriakides, F. Blaabjerg, "An adaptive tuning mechanism for phase-locked loop algorithm for faster time performance of interconnected renewable energy sources," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 2, pp. 1792-1804, Apr. 2015**.**

[17] L. Hadjidemetriou, E. Kyriakides, F. Blaabjerg, "A robust synchronization to enhance the power quality of renewable energy systems," *IEEE Trans. Ind. Electron*., Vol. 62, No. 8, pp. 4858-4868, Aug. 2015.

[18] S. Golestan, F. D. Freijedo, A. Vidal, J. M. Guerrero, and J. Doval Gandoy, "A quasi-type-1 phase-locked loop structure," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6264-6270, Dec. 2014.

[19] S. Golestan, J. M. Guerrero, A. M. Abusorrah, Y. Al-Turki, "Hybrid synchronous/stationary reference-frame-filtering based pll," *IEEE Trans. Ind. Electron.,* Vol. 62, No. 8, pp. 5018-5022, Aug. 2015.

[20] S. Golestan, J. M. Guerrero, Ana Vidal, A. G. Yepes, J. Doval-Gandoy, F. D. Freijedo, "Small-signal modeling, stability analysis and design optimization of single-phase delay-based plls," *IEEE Trans. Power Electron.*, Vol. 31, No. 5, pp. 3517-3527, May. 2016.

[21] S.Golestan, M. Ramezani, J. M. Guerrero, M. Monfared, "dq-frame cascaded delayed signal cancellation-based pll: analysis, design, and comparison with moving average filter-based pll," *IEEE Trans. Power Electron.*, Vol. 30, No. 3, pp. 1618-1632, Mar. 2015.

[22] Y. F. Wang and Y. W. Li, "Three-phase cascaded delay signal cancellation pll for fast selective harmonic detection," *IEEE Trans. Ind. Electron.,* Vol. 60, No. 4, pp. 1452-1463, Apr. 2013.

[23] Y. F. Wang and Y. W. Li, "Grid synchronization pll based on cascaded delay signal cancellation," *IEEE Trans. Power Electron.*, Vol. 26, No. 7, pp. 1987-1997, Jul. 2011.

[24] S. Golestan, A. Vidal, A. G. Yepes, J. M. Guerrero, J. C. Vasquez and J. Doval-Gandoy, "A true open-loop synchronization technique," *IEEE Trans. Ind. Inform.,* Vol. 12, No. 3, pp. 1093-1103, Jun. 2016

[25] Qicheng Huang and K. Rajashekara, "An improved delayed signal cancellation pll for fast grid synchronization under distorted and unbalanced grid condition," in *2016 IEEE Industry Applications Society Annual Meeting*, pp. 1-7, 2016.

[26] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero, J. Doval-Gandoy, "An efficient implementation of generalized delayed signal cancellation pll," *IEEE Trans. Power Electron.*, Vol. 31, No. 2, pp. 1085-1094, Feb. 2016.

[27] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 765-778, Feb. 2013.

[28] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Trans. Ind. Electron.,* Vol. 59, No. 6, pp. 2718-2731, Jun. 2012.

[29] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. 37th PESC*, pp. 1-6, 2006.

[30] M. Tsili and S. Papathanassiou, "A review of grid code technical requirements for wind farms," *IET Renew. Power Gener.*, Vol. 3, No. 3, pp. 308-332, Sep. 2009.

[31] Alvaro Luna, Joan Rocabert, J. Ignacio Candela, Juan Romon Hermoso, Remus Teodorescu, Frede Blaabjerg, Pedro Rodriguez, "Grid voltage synchronization for distributed generation systems under grid faults conditions," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 4, pp. 3414-3425, Jul. 2015.

[32] e-on, "Grid code-High and extra high voltage," Bayreuth, Germany. Apr. 2006. [Online]. Available: https://www.bayernwerk.de/cps/rde/xbcr/bayernwerk/NAR_englisch.pdf.

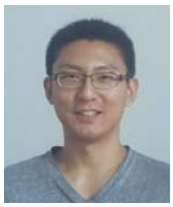
[33] *PO-12.3 Requisitos de Respuesta Frente a Huecos de Tension de las Instalaciones Eolicas*, Comisión Nacional de Energía, Madrid, Spain, Oct. 2006.

[34] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Std. 1547-2003, 2003.

[35] *The Grid Code: Revision 31*, National Grid Electricity Transmission, Warwick, U.K., Oct. 2008, no. 3. [Online]. Available: http://www2. nationalgrid.com/uk/industry-information/electricity-codes/grid-code/the-grid-code/

[36] Z. Xin, X. Wang, Z. Qin, M. Lu, P. C. Loh, and F. Blaabjerg, "An improved second-order generalized integrator based quadrature signal generator," *IEEE Trans. Power Electron.,* Vol. 31, No. 12, pp. 8068-8073, Dec. 2016.

[37] S. Golestan, J. M. Guerrero, and G. B. Gharehpetian, "Five approaches to deal with problem of dc offset in phase-locked loop algorithm: design considerations and performance evaluations," *IEEE Trans. Power Electron.,* Vol. 31, No. 1, pp. 648-661, Jan. 2016.



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