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Half-bridge Cascaded Multilevel Inverter Based Series Active Power Filter

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Abstract

A new single phase half-bridge cascaded multilevel inverter based series active power filter (SAPF) is proposed. The main parts of the inverter are presented in detail. With the proposed inverter topology, any compensation voltage reference can be easily obtained. Therefore, the inverter acts as a harmonic source when the reference is a non-sinusoidal signal. A 31-level inverter based SAPF with the proposed topology, is manufactured and the voltage harmonics of the load connected to the point of common coupling (PCC) are compensated. There is no need for a parallel passive filter (PPF) since the main purpose of the paper is to represent the compensation capability of the SAPF without a PPF. It is aimed to compensate the voltage harmonics of the load fed by a non-sinusoidal supply using the proposed inverter. The validity of the proposed inverter based SAPF is verified by simulation as well as experimental study. The system efficiency is also measured in this study. Both simulation and experimental results show that the proposed multilevel inverter is suitable for SAPF applications.

Key words: Active power filter, Half-bridge cascaded, Harmonic compensation, Multilevel inverter, Power quality

I. INTRODUCTION

Power quality deterioration, due to harmonics, occurs in electric transmission and distribution systems due to the widespread use of power electronic devices and non-linear loads. Transmission losses, transformer and neutral-conductor overheating, power factor correction capacitor overloading, power component damage and voltage quality degradation are only a few of the problems that harmonics may cause [1]. Therefore, harmonics are one of the most important power quality problems, and research on this topic has intensified in last decades.

Non-linear loads draw harmonic currents from a sinusoidal supply. This results in distortion of the supply voltage waveform at the PCC due to source impedance. Traditionaly, PPFs have been used to suppress harmonic currents. However, they are inadequate and have adverse influences. For example, their performance is strongly affected by the network impedance and they may produce resonance, which increases the distortions. In addition, they are also bulky, and have fixed compensating characteristic since they are designed for a specific frequency [2], [3]. In order to overcome these drawbacks, active filtering solutions have been proposed for harmonic suppression. Active power filters (APFs), as an active solution, can eliminate all harmonics, and the filtering effect of APFs is not affected by the system parameters.

APFs are classified as follows: parallel (or shunt) active power filters (PAPFs) and SAPFs. Most of the APFs that have been introduced until now are of parallel type. However, there are still shortcomings. They are comparatively more expensive due to large ratings of about 30%–60% of the load, they cannot improve the filter characteristics when system resonance occurs and they are difficult to use in high voltage systems [4]-[8]. Their performance is better in current harmonics generating loads than in voltage harmonics generating loads. SAPFs are more effective for compensating voltage harmonics. In recent developments, series hybrid active power filters (SHAPFs) have become very popular since they extend multi-functionality and help in reducing the inverter capacity of SAPFs [9]-[14]. In particular, solutions for harmonic voltage compensation are critical because loads acting as harmonic voltage sources, such as copiers, fax machines, fluorescent lamps, air conditioners, etc., have continued to increase [9].

In recent years, APFs based on the topologies of multilevel inverters have been studied to obtain lower harmonic

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distortion levels. In addition, an output waveform with required harmonics can be produced by multilevel inverters. Thus, there are APFs based on different multilevel inverter topologies in the literature. These topologies are classified as diode-clamped multilevel inverters [15], multilevel inverters with flying capacitor [16] and H-bridge cascaded multilevel inverters [17]-[20]. Since the H-bridge cascaded multilevel inverter (HCMLI) topology achieves the same level of output voltage by using the lowest number of semiconductor switching devices, it is preferred more than others [21]-[23]. In addition, high power and voltage applicability, reduced dv/dt ratio on switching devices, lower switching losses and better electromagnetic interference are the other advantages of this topology. The topologies of HCMLIs can be classified as symmetric and asymmetric. If the values of the dc voltage sources in the cascaded cells are equal, the inverter is called symmetric. The inverter is called asymmetric if at least one of the dc voltage sources in the cascaded cells is different from the others. With the same number of semiconductor switching devices, the asymmetric HCMLI can achieve a higher magnitude and level at the output voltage. The HCMLI topologies used in APF applications differs from each other such as symmetrical HCMLI (Cascaded-1, isolated dc sources in the H-bridges are equal) [17], [18], asymmetrical HCMLI (Cascaded-2, isolated dc sources in the H-bridges are scaled in power of 2) [19], and asymmetrical HCMLI with an interfacing transformer (Cascaded-3, turn ratio of the transformers are scaled in power of 3) [20]. The proposed cascaded multilevel inverter topology is also asymmetric and it is more advantageous than the asymmetric HCMLI topology in terms of the number of semiconductor switching devices. Easy generation of switching signals and simplicity of control are the other advantages of the proposed inverter.

In this study, a single phase asymmetric half-bridge cascaded multilevel inverter based SAPF is proposed. The proposed inverter topology has all of the positive aspects of H-bridge cascaded multilevel inverters. In Section 2(B), a comparison of the multilevel inverter topologies used in active power filtering applications depending on the number of switching devices has been made in detail. It can be seen that the proposed topology is the most advantageous topology in terms of the number of switching devices.

Furthermore, the proposed topology has some other advantages over the multilevel inverter topologies used in APF applications in terms of switching losses. These advantages are detailed below.

In the literature, it can be been seen that PWM inverters are conventionally used in active power filter applications. In such inverters, switching signals are generated by employing PWM with switching frequencies of 15-23 kHz [2], [3], [6], [7], [11], [14]. PWM inverters operating at such high frequencies can cause high-order harmonics and additional switching losses [10]. The switching frequency in the proposed inverter is much lower than those of PWM inverters. The proposed multilevel inverter topology consists of 4 level modules, and the switching devices on each of the level modules have different switching frequencies. To obtain a reference signal with a frequency of 150 Hz at the inverter output, the most significant module operates at a frequency of 300 Hz while the other three modules operate at frequencies of 900 Hz, 1.8 kHz and 3.6 kHz respectively. Since the switching frequency is a parameter that directly affects the switching losses, the proposed inverter topology has lower switching losses. In addition, filter circuits are used at the outputs of the PWM inverters to make the output voltage sinusoidal [2], [3], [11], [14]. Since the filter circuits used in such topologies causes additional losses, the system efficiency is reduced. In the proposed inverter topology, there is no need for a filter circuit at the output of the inverter. This ensures that the proposed inverter topology achieves a higher system efficiency than the PWM inverter topologies.

In this paper, a novel multilevel inverter topology has been proposed to use in SAPF applications. The proposed topology and its operation principle are presented in Section II. An experimental setup has been prepared to demonstrate the performance of the proposed inverter topology in SAPF applications. The configuration for the experimental setup is shown in Section II. The experimental setup is realized in a simulation study. The simulation results are presented in Section III. In Section IV, the detailed parameters of the experimental setup are presented and experimental results are given. Additionally, the value of the system efficiency is presented for both simulation and experimental studies.

II. DESCRIPTION OF THE PROPOSED SYSTEM

A. System Configuration

Fig. 1 shows a block diagram of the experimental setup used for simulation and experimental studies. The experimental setup consists of a series resistor R_s, a non-linear load fed by a sinusoidal source V_s, and a 31-level inverter based SAPF connected to the PCC with a resistive load. The non-linear load acting as harmonic voltage source is a single phase diode rectifier with an RC load at the dc side. The nonlinear load is used to generate harmonic current at the PCC. The harmonic voltage on R_s due to the generated harmonic current provides a voltage with harmonic components at the PCC in the experimental environment. Therefore, the harmonic components of the load voltage are eliminated by the proposed multilevel inverter based SAPF. In addition to the experimental setup, voltage and current sensors are available to measure the voltage and current at the PCC. A Zero-Crossing Detector (ZCD) is designed to synchronize with the voltage source V_s phase angle, and it is placed into the experimental setup.

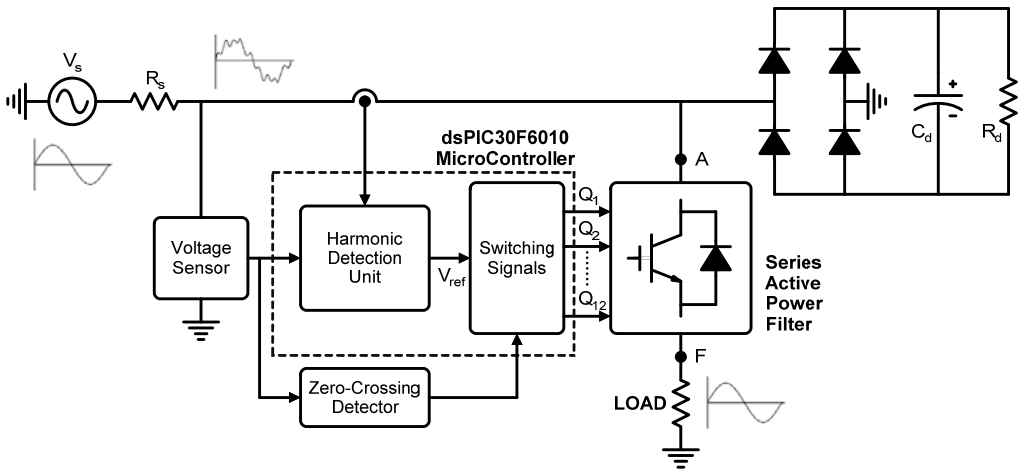


Fig. 1. Block diagram of the experimental setup for simulation and experimental studies.

B. Multilevel Inverter

The proposed SAPF has a single-phase asymmetric half-bridge cascaded multilevel inverter. The scheme of the multilevel inverter is shown in Fig. 2. The inverter is composed by two main parts.

These parts are called as Level Module (LM) and H-Bridge Module (HM). In Fig. 2, there is a 31-level inverter with four LMs. To expand the system and increase the output voltage levels of the inverter, more LMs connected in series are used.

An LM comprises a dc source and two semiconductor switching devices. The voltage of the dc source V_d in LM 1 is determined by the level of the inverter and the required maximum value of the output voltage.

$$V_d = \frac{2.V_{max}}{n-1} \tag{1}$$

where V_{max} is the required maximum value of the output voltage, and n is the level of the inverter. n can be computed as:

$$n = 2^{(m+1)} - 1 \tag{2}$$

where m is the number of LMs used in the inverter. The voltage of the dc sources in the other LMs (V_{LM}) can be defined as:

$$V_{LM_j} = 2^{(j-1)}.V_d \qquad j = 1, 2, 3, \ldots, m \tag{3}$$

Since the voltage of the dc sources in the LMs are not equal, the proposed multilevel inverter has an asymmetric structure. The voltages of the dc sources in the LMs are scaled in power of 2. This balance between the dc sources needs to be preserved. Voltage balance control is a major problem in multilevel inverter based APFs. To overcome voltage unbalance, different control strategies have been developed in the literature. The two lowest dc capacitor voltages have been controlled in [24] to balance all of the capacitor voltages in a converter with the smallest voltage cell operating in PWM. In [25], a three-phase HCMLI has been controlled using direct current control to obtain equal

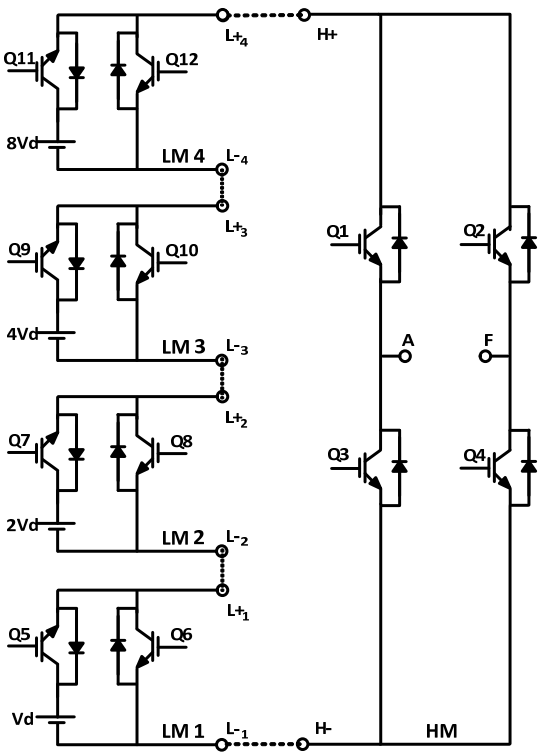


Fig. 2. Scheme of the proposed multilevel inverter.

phase-to-phase voltages and dc capacitor voltages. In [26], two different charge balance control algorithms have been proposed for a HCMLI based APF with a capacitor in the first H-bridge cell and dc voltage sources in the others. A set point has been defined for dc link voltage control and a conditional switching procedure has been used in [27], which runs any transformation and measurement of dc values. There are many other studies on voltage balance and control strategies in the literature. In this study, the voltages of the dc sources are observed and recorded during operation. Then, an adjustment is done when necessary.

A detailed simulation study has been carried out to observe the effect of the dc source voltages in each of the modules on

TABLE I
THD VALUES UNDER VOLTAGE UNBALANCE

Change in DC Voltage Sources				Set 1	Set 2	Set 3
ΔV1	ΔV2	ΔV3	ΔV4	THD (%)		
0%	0%	0%	0%	1.52	1.76	2.80
0%	0%	0%	-15%	1.91	1.77	3.34
0%	0%	-15%	0%	2.12	2.84	3.35
0%	-15%	0%	0%	1.69	2.19	3.19
-15%	0%	0%	0%	1.53	1.89	2.93
-5%	-5%	-5%	-5%	1.70	2.05	3.00
-10%	-10%	-10%	-10%	2.26	2.82	3.85
0%	-5%	-10%	-15%	2.22	2.41	3.59
0%	-5%	+10%	-15%	2.28	2.49	4.17
-3%	-5%	-9%	-13%	2.11	2.36	3.47
0%	-9%	-4%	-14%	1.99	2.08	3.42
-4%	0%	-12%	-7%	2.04	2.51	3.28
-6%	-7%	0%	-11%	1.81	1.94	3.30

the performance of the proposed SAPF. According to this, the values of the dc voltage sources in the modules are changed at certain ratios to create voltage unbalance. The total harmonic distortion (THD) values of the load voltage obtained from simulations of 12 different voltage unbalance cases are tabulated in Table I. In the first line of Table I, the THD values are given for the three different circuit parameter sets shown in Table IV, where there is no voltage unbalance in the dc sources, i.e., the source voltages are 6V, 12V, 24V and 48V. This line is the reference point of the simulations. For example, for the case on line 12, the value of the voltage sources of each module is reduced by 4%, 0%, 12% and 7%, respectively, to create an unbalance. The THD value is 2.04% for Set 1. In the case of voltage unbalance, the value of the THD is increased. However, in all of the cases for the three different circuit parameter sets it is below 5% meeting IEEE-519 Standard. This demonstrates the suitability of the proposed inverter for SAPF applications, even in the case of voltage unbalance at a certain rate.

The HM, which is the constant part of the inverter, is connected to the series LMs as shown in Fig. 2. The effects of the HM and LMs on the number of semiconductor switching devices r is expressed as:

$$r = 2m + 4 \tag{4}$$

Depending on the number of LMs, the value of n obtained from Equ. (2) is the maximum level of the inverter. Accordingly, up to 31-level can be achieved by four LMs. However, any required number of level such as 19, 25 or 29 can also be obtained by four LMs. If the number of LMs m is rearranged from Equ. (2) depending on the value of n and substituted into Equ. (4), Equ. (5) is obtained. Thus, the number of switching devices is easily calculated as a function of the inverter level n.

$$r = 2\log_2(n+1) + 2 \tag{5}$$

TABLE II
NUMBER OF SWITCHING DEVICES FOR AN N-LEVEL SINGLE PHASE MULTILEVEL INVERTER

Topology	Number of Switches	Clamping diodes	Flying capacitors
Diode-clamped	2(n-1)	(n-1)(n-2)	0
Flying-capacitor	2(n-1)	0	(n-1)(n-2)/2
Cascaded-1	2(n-1)	0	0
Cascaded-2	$4\log_2(n+1)-4$	0	0
Cascaded-3	$4\log_3(n)$	0	0
Proposed	$2\log_2(n+1)+2$	0	0

In Table II, the generalized formulas for the number of semiconductor switching devices of various multilevel inverter topologies in the literature are compared with the proposed inverter topology. All of the inverter topologies in the table are used in active power filter applications and the generalized formulas depends on n-level single phase multilevel inverters.

As can be seen in Table II, 60 switching devices and 870 clamping-diodes for the diode-clamped inverter; 60 switching devices and 435 flying-capacitors for the flying-capacitor inverter; 60 switching devices for Cascaded-l; and 16 switching devices for Cascaded-2 are needed to obtain 31-level output voltage waveforms. With Cascaded-3, 27-level for the output voltage can be achieved by 12 switching devices, while 81-level can be achieved by 16 switching devices. The proposed inverter topology can provide a 31-level output voltage waveform by using only 12 switching devices, and it can provide a 127-level output by using only 16 switching devices. The comparison made for the six inverter topologies in Table II can be summarized as follows:

1) The proposed inverter topology uses the least number of switching devices for a determined number of level. The number of switching devices is a parameter that directly affects the switching losses. Therefore, a lower number of switching devices reduces the switching losses in the continuous current. In addition, a lower number of switching devices significantly reduces the costs for medium and high voltage levels.
2) If it is considered to design a multilevel inverter in Table II with a specified number of switching devices, for example 16 switching devices, the diode-clamped, flying-capacitor and Cascaded-1 topologies can provide a 9-level output voltage waveform. Cascaded-2 and Cascaded-3 topologies can provide a 31-level and an 81-level output voltage waveform, respectively. With the proposed inverter topology, a 127-level output voltage waveform can be achieved with the same number of switching devices. Therefore, when the same

number of switching devices is taken into consideration, the proposed inverter topology achieves a better output voltage waveform for active power filter applications.

By increasing the number of LMs, any required number of level can be easily obtained by the proposed inverter since it has a simple and modular structure.

C. Operational Principle

An output voltage waveform with a lower THD can be easily generated with the proposed multilevel inverter as previously mentioned. Furthermore, the proposed multilevel inverter has the ability to produce any voltage with harmonic components. With this feature, it acts as a harmonic source. Initially, the measured analog voltage and current are converted by means of the analog-to-digital converter (ADC) in the microcontroller. Then the harmonic components of the PCC voltage are detected by the harmonic detection unit. A control strategy in the frequency domain based on a Fourier analysis is used to determine the fundamental harmonic in the harmonic detection unit. When the fundamental harmonic voltage is subtracted from the converted voltage, the inverse of the remaining voltage represents the reference. The obtained reference voltage is expressed as shown in Equ. (6). In Fig. 3, a sample reference voltage waveform is shown.

$$V_{ref} = \sum_{h=2}^{\infty} V_h \sin(h\omega t + \varphi_h) \quad (6)$$

After determining the reference V_{ref}, it is simple to find the switching signals. The instantaneous values of the reference voltage for each sampling are substituted in Equ. (6) to calculate S values in Equ. (7) for $j = 1,2,3,\ldots,m$. The instantaneous values of S are then substituted into Equ. (8)-(9) so that the switching signals ($Q_{2j+3}(t)$, $Q_{2j+4}(t)$) can be easily determined for the level modules.

$$S_{2j+3}(t) = \left[\frac{V_{ref}(t) - (V_{ref}(t) \bmod 2^{j-1})}{2^{j-1}}\right] mod\ 2 \quad (7)$$

$$Q_{2j+3}(t) = \begin{cases} 0, & (V_1 \geq 0 \wedge \sum_{h=2}^{\infty} V_h \geq 0) \\ 0, & (V_1 < 0 \wedge \sum_{h=2}^{\infty} V_h < 0) \\ S_{2j+3}(t), & (V_1 \geq 0 \wedge \sum_{h=2}^{\infty} V_h < 0) \\ S_{2j+3}(t), & (V_1 < 0 \wedge \sum_{h=2}^{\infty} V_h \geq 0) \end{cases} \quad (8)$$

$$Q_{2j+4}(t) = \begin{cases} \overline{S_{2j+3}(t)}, & (V_1 \geq 0 \wedge \sum_{h=2}^{\infty} V_h \geq 0) \\ \overline{S_{2j+3}(t)}, & (V_1 < 0 \wedge \sum_{h=2}^{\infty} V_h < 0) \\ 0, & (V_1 \geq 0 \wedge \sum_{h=2}^{\infty} V_h < 0) \\ 0, & (V_1 < 0 \wedge \sum_{h=2}^{\infty} V_h \geq 0) \end{cases} \quad (9)$$

In order to correctly calculate the switching signals, the instantaneous values of the reference voltage V_{ref} must be correctly obtained. Therefore, the scanning time Δt should be chosen small enough. The scan time is the time interval between two consecutive values of t. The maximum value of the scanning time depends on the fundamental frequency and the number of LMs. How to find this value is given in Equ. (10). It is crucial that the sample time t_{sample} be chosen so that it is very small with respect to the maximum value of the scan time t_{max} [28], [29].

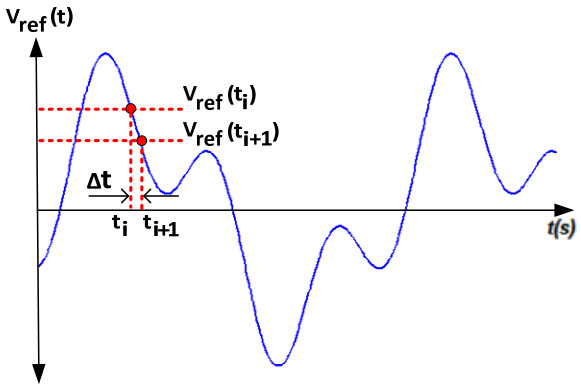


Fig. 3. Sample reference voltage waveform.

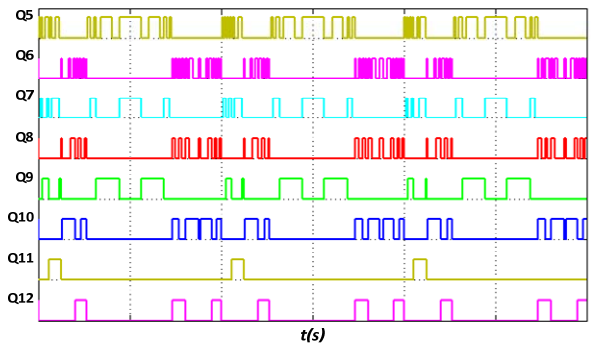


Fig. 4. Switching signals for the reference voltage.

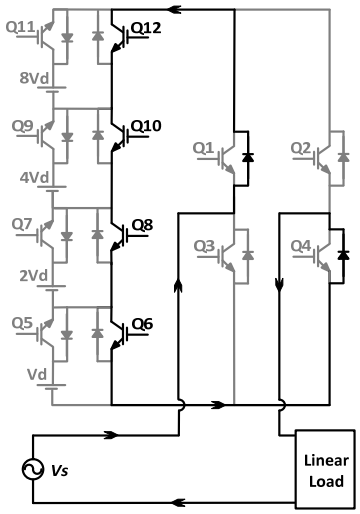
$$t_{max} = sin^{-1}\left(\frac{1}{2^{(m+1)}-2}\right).(2.\pi.f_f)^{-1} \quad (10)$$

$$t_{sample} = \Delta t = t_{i+1} - t_i \quad (11)$$

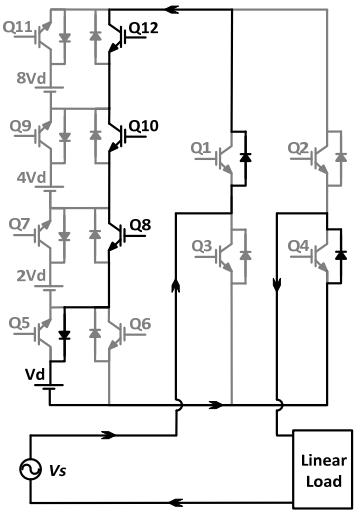
$$t_{sample} \ll t_{max} \quad (12)$$

In Fig. 4, switching signals are shown for the eight switching devices of the level modules. These are the switching signals to obtain the reference voltage shown in Fig. 3. After extracting the reference voltage, it is very easy to obtain switching signals in the proposed inverter topology. The values of the dc sources used in the level modules vary as the exponents of 2. This situation is shown in Equ. (3) and in Fig. 2. In other words, binary representation of the absolute value of the reference voltage obtained instantaneously after the harmonic detection process, gives the switching signals of the level modules. The easy acquisition of switching signals simplifies the structure of the control system. The simplicity of the control system is one of the most important advantages of the proposed inverter topology, which makes it attractive for use in SAPF applications.

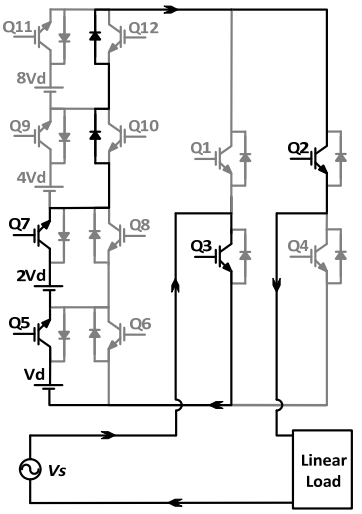
The switching signals required for all of the output voltage levels in a 31-level SAPF application are tabulated in Table III. In addition, the states of the switching devices for some of the output voltage levels in the proposed inverter topology are shown in Fig. 5. For example, to obtain a voltage level of -6.V_d under the situation of (V_1<0 and $\sum V_h$<0), D_2, D_3, Q_6, D_7, D_9 and Q_{12} need to be used as shown in Fig. 5(e).



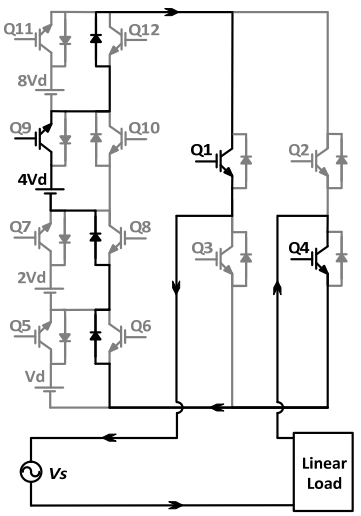
(a) $V_1 \geq 0$, $\sum V_h \geq 0$ ($V_{inverter}=0$).



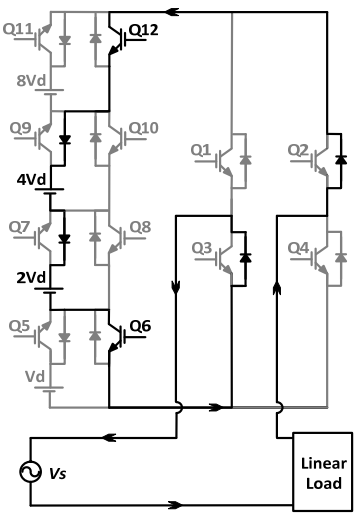
(b) $V_1 \geq 0$, $\sum V_h \geq 0$ ($V_{inverter}= -V_d$).



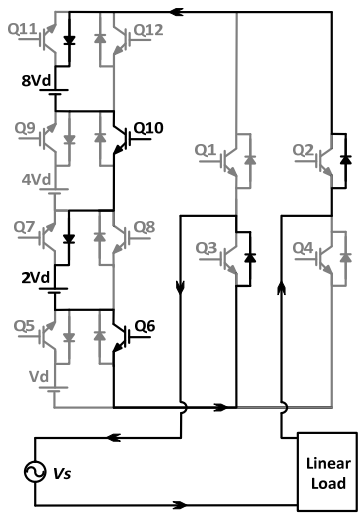
(c) $V_1 \geq 0$, $\sum V_h < 0$ ($V_{inverter}=3V_d$).



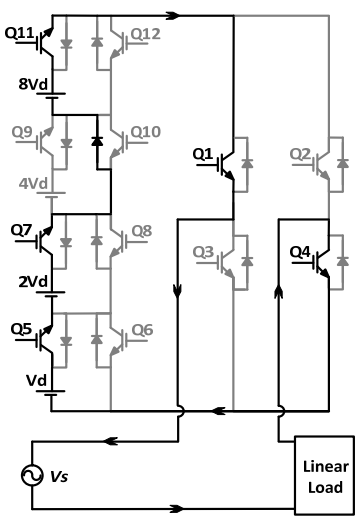
(d) $V_1 < 0$, $\sum V_h \geq 0$ ($V_{inverter}=4Vd$).



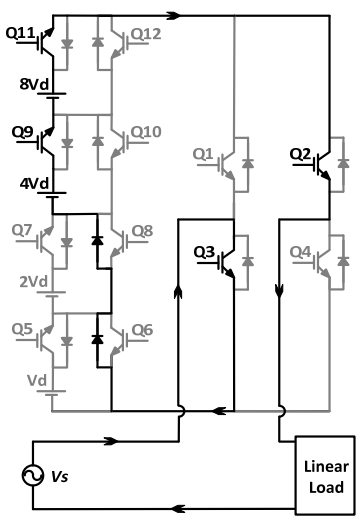
(e) $V_1 < 0$, $\sum V_h < 0$ ($V_{inverter}=-6Vd$).



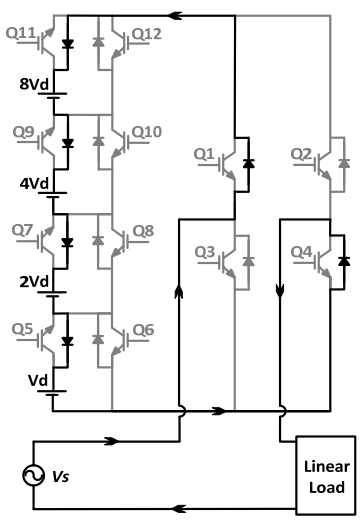
(f) $V_1 < 0$, $\sum V_h < 0$ ($V_{inverter}=-10Vd$).



(g) $V_1 < 0$, $\sum V_h \geq 0$ ($V_{inverter}=11V_d$).



(h) $V_1 \geq 0$, $\sum V_h < 0$ ($V_{inverter}=12V_d$).



(i) $V_1 \geq 0$, $\sum V_h \geq 0$ ($V_{inverter}=-15V_d$).

Fig. 5. Various output levels of the proposed single phase half-bridge cascaded 31-level inverter.

TABLE III
SWITCHING SITUATIONS FOR A 31-LEVEL INVERTER BASED SAPF

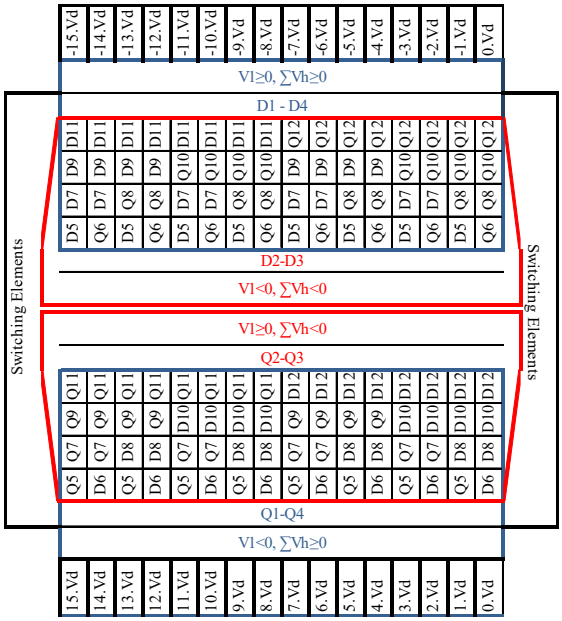


TABLE IV
CIRCUIT PARAMETER VALUES FOR THE SIMULATION AND EXPERIMENTAL STUDIES

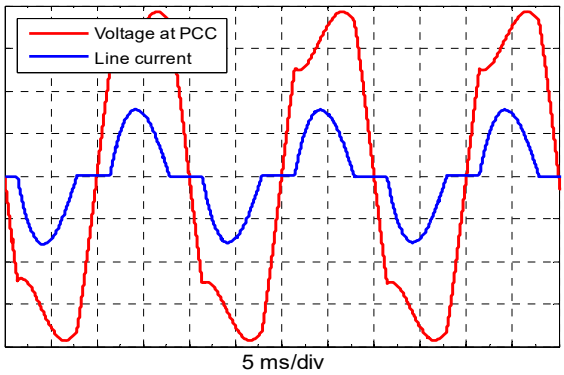
Circuit parameters of the system		
Set 1	Set 2	Set 3
R_s = 16 Ω	R_s = 96 Ω	R_s = 192 Ω
R_d = 48 Ω	R_d = 192 Ω	R_d = 192 Ω
C_d = 204 µF	C_d = 204 µF	C_d = 204 µF
Load = 192 Ω	Load = 192 Ω	Load = 576 Ω

III. SIMULATION STUDY

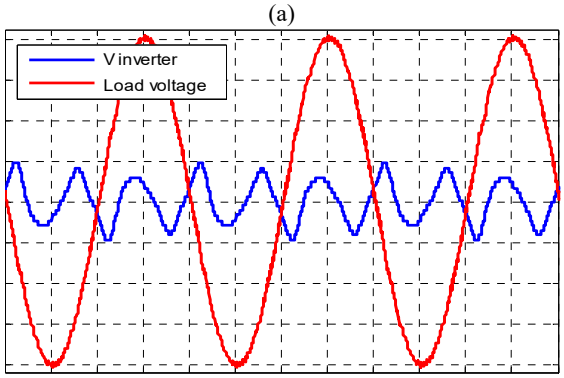
The previously discussed single phase half-bridge cascaded multilevel inverter based SAPF is simulated for the arrangement shown in Fig. 1. The SAPF simulation model is tested for compensating the load voltage harmonics at the PCC with different harmonic distortion levels using three circuit parameter values. The circuit parameter values are displayed in Table IV. To supply a high distorted voltage at the PCC, a resistor (R_s) is connected in series with the voltage source V_s.

The harmonic components of the voltage at the PCC are detected by the SAPF harmonic detection unit. The reference voltage function is constituted related to the detected harmonic components and the switching signals are generated. Simulations are carried out for three different circuit parameter values.

Fig. 6(a), Fig. 7(a) and Fig. 8(a) show waveforms of the PCC voltage and line current before compensation. Waveforms of the load voltage and inverter voltage after compensation are shown in Fig. 6(b), Fig. 7(b) and Fig. 8(b). Below in Section IV, the THD values of the load voltage before and after compensation are displayed in Table V.

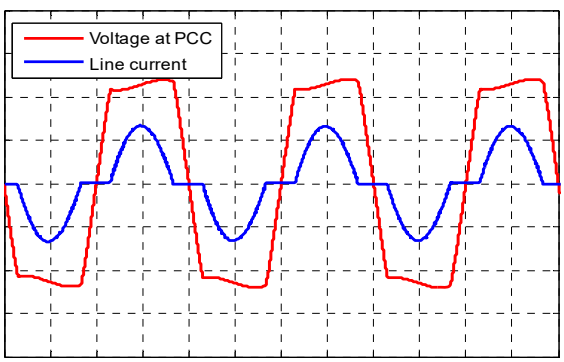


(a)

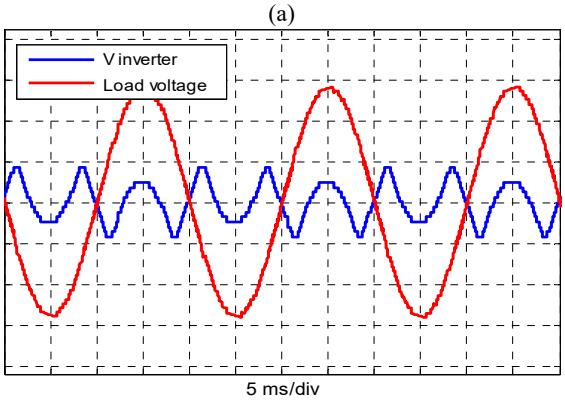


(b)

Fig. 6. Simulation results for Set 1: (a) PCC voltage and line current before compensation (50 V/div, 5 A/div); (b) Inverter and load voltage after compensation (50 V/div).

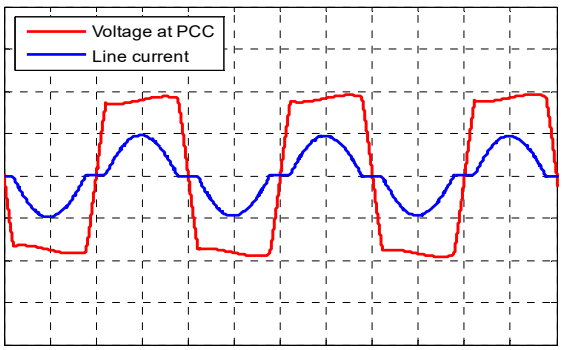


(a)

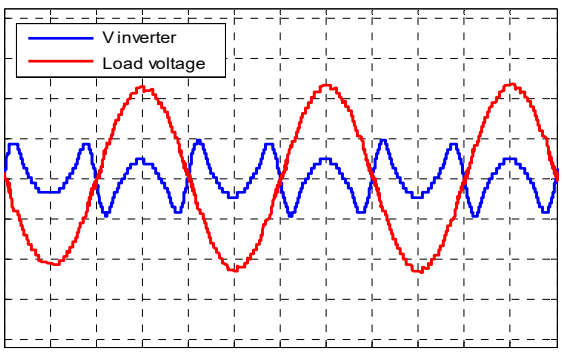


(b)

Fig. 7. Simulation results for Set 2: (a) PCC voltage and line current before compensation (50 V/div, 1 A/div); (b) Inverter and load voltage after compensation (50 V/div).



(a)



(b)

Fig. 8. Simulation results for Set 3: (a) PCC voltage and line current before compensation (50 V/div, 1 A/div); (b) Inverter and load voltage after compensation (50 V/div).

IV. Experimental Verification

To demonstrate the validity of the proposed inverter based SAPF, a prototype is developed on the basis of the system configuration shown in Fig. 1. A photograph of experimental setup is given in Fig. 9. The inverter in the photograph has six level modules. However, four of them are used to constitute a 31-level inverter. The prototype is implemented for a 220 V, 50 Hz, single-phase system. The single phase half-bridge cascaded multilevel inverter consists of Mitsubishi IGBT modules and drivers with base boards. The digital controller dsPIC30F6010 is a 16-bit microcontroller from Microchip for high performance applications. A Zero-Crossing Detector (ZCD) is designed to generate a synchronized pulse related to the voltage source V_s phase angle.

The SAPF experimental setup is tested for compensating the voltage harmonics of a load connected to the PCC with the same circuit parameter sets used in the simulation study, and results are presented in Fig. 10, Fig. 11 and Fig. 12. Waveforms of the PCC voltage and line current before compensation are given in Fig. 10(a), Fig. 11(a) and Fig. 12(a). Waveforms of the load voltage and proposed inverter voltage after compensation are shown in Fig. 10(b), Fig. 11(b) and Fig. 12(b). The THD values of the load voltage before and after compensation are displayed in Table V.

It is clear that the THD value of the load voltage is reduced

TABLE V
THD Values of the Load Voltage

		Simulation	Experimental
Set 1	Before compensation	18.47%	18.39%
	After compensation	1.52%	1.53%
Set 2	Before compensation	24.25%	24.12%
	After compensation	1.76%	2.44%
Set 3	Before compensation	30.70%	30.17%
	After compensation	2.80%	2.60%

TABLE VI
System Efficiency of the SAPF

	Simulation	Experimental
Set 1	98.86%	96.20%
Set 2	98.24%	94.57%
Set 3	98.68%	94.18%

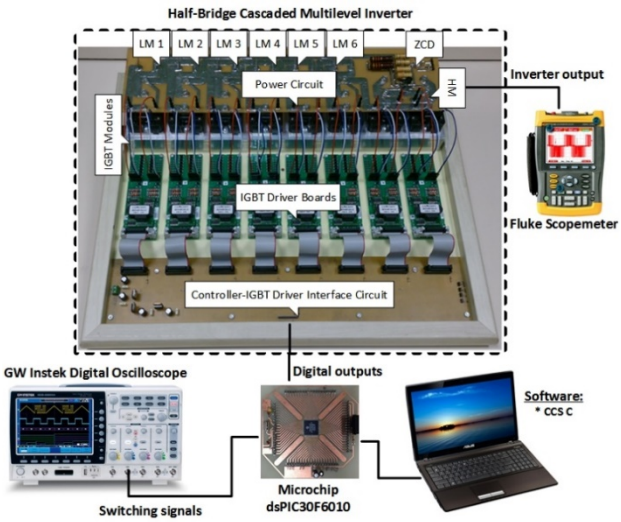


Fig. 9. Photograph of the experimental prototype.

significantly for all of the parameter sets. A comparison between the THD values before and after the compensation can be easily done for the simulation and experimental studies. For example, the distorted load voltage is equal to the PCC voltage before compensation. The distortion level from the simulation and experimental studies can be seen respectively in Fig. 6(a) and Fig. 10(a) for the circuit parameter values of Set1. After compensation, the THD value of load voltage is significantly decreased from 18.47% to 1.52% for the simulation study and from 18.39% to 1.53% for the experimental study. For all of the circuit parameter values, the load voltage is nearly sinusoidal as seen in the (b)-subfigures of Fig. 6, Fig. 7 and Fig. 8 for the simulation, and in the (b)-subfigures of Fig. 10, Fig. 11 and Fig. 12 for the experiments.

In Section I, the parameters affecting system efficiency are mentioned. Using a lower number of semiconductor switching devices than the other topologies while obtaining the same output level, switching in low frequencies and freedom from the necessity of output filters are the parameters that lead to a very high system efficiency. In

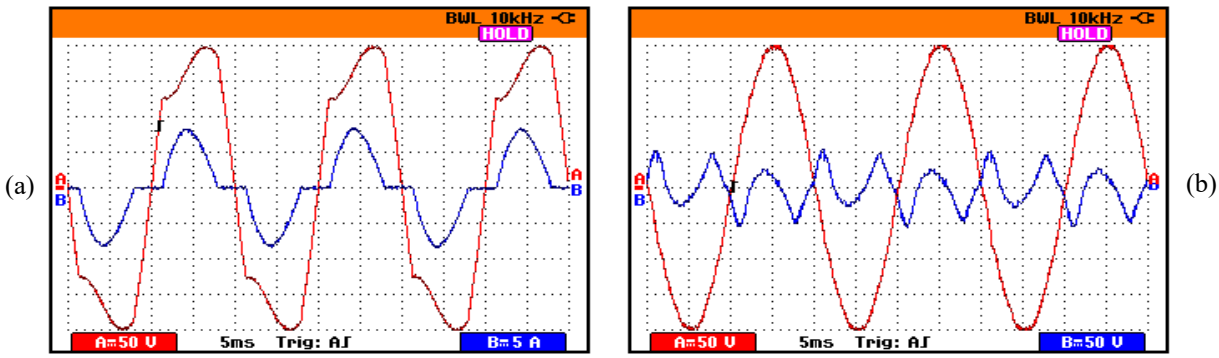


Fig. 10. Experimental results for Set 1: (a) PCC voltage and line current before compensation; (b) Inverter and load voltage after compensation.

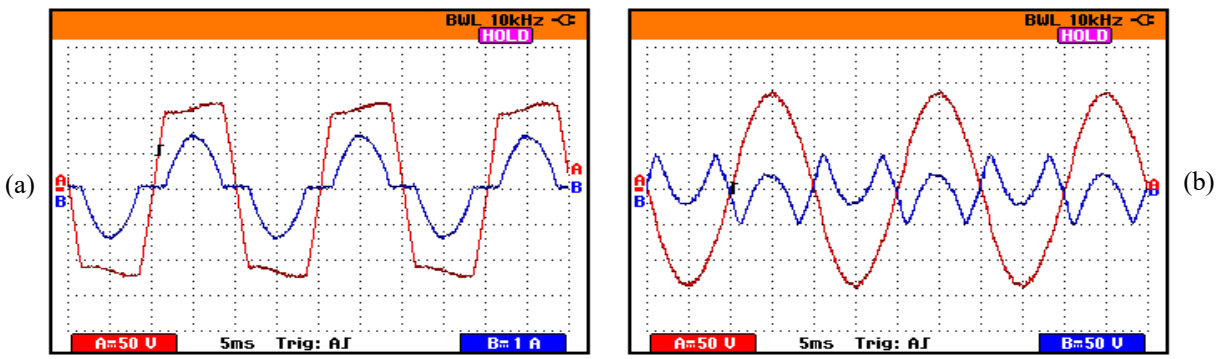


Fig. 11. Experimental results for Set 2: (a) PCC voltage and line current before compensation; (b) Inverter and load voltage after compensation.

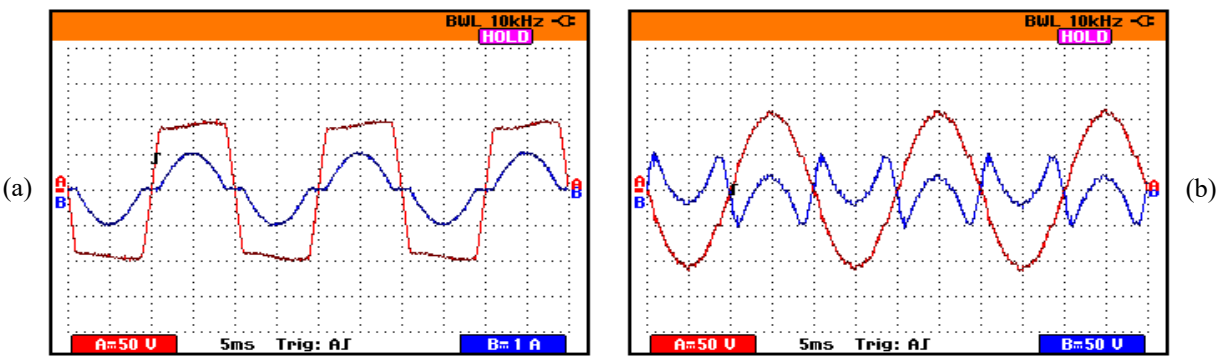


Fig. 12. Experimental results for Set 3: (a) PCC voltage and line current before compensation; (b) Inverter and load voltage after compensation.

Table VI, the system efficiency of the proposed asymmetric half-bridge cascaded multilevel inverter based SAPF is given through simulation and experimental study using the circuit parameter sets.

V. CONCLUSIONS

This paper proposes a single phase half-bridge cascaded multilevel inverter based SAPF. The multilevel inverter topology and operation principle are introduced. With the proposed topology, the number of output levels can be easily increased. The switching signals of the semiconductor devices used in the inverter are also obtained by a simple method.

A SAPF with the proposed inverter topology is simulated under different harmonic distortion levels of the PCC. The aim of the simulation is to compensate the voltage harmonics of a load connected to the PCC.

In addition to the simulations, a prototype of the proposed SAPF is designed. Using this prototype, experimental studies are carried out. A Microchip dsPIC30F6010 is used in this prototype since it is a commercially available and inexpensive microcontroller.

The results of the proposed system are summarized as follows:

- Depending on the number of switching devices, the proposed multilevel inverter topology is the most advantageous topology since the smallest number of switching devices for a determined number of level is required. When the number of switching devices is used for comparison, the proposed multilevel inverter topology achieves a better output voltage waveform for active power filter applications.
- The lower number of switching devices significantly reduces the switching losses in the continuous current, which makes the system efficiency higher.
- In medium and high voltage applications, the lower number of switching devices significantly reduces the inverter cost.
- In SAPF applications, the switching frequency of the proposed multilevel inverter is much lower than that of PWM inverters. Since the switching frequency is a parameter that directly affects the switching losses, the proposed inverter topology based SAPF has lower switching losses and a higher system efficiency.
- Filter circuits are used at the output of the PWM inverters to make the output voltage more sinusoidal. With the proposed multilevel inverter topology, there is no need for a filter circuit. Since filter circuits are not used, additional losses are removed. This ensures that the proposed inverter topology achieves a higher system efficiency than PWM inverter topologies.
- In the proposed multilevel inverter based SAPF, the switching signals are obtained by a simple control strategy. The easy acquisition of switching signals simplifies the structure of the control system which makes it attractive for use in SAPF applications.
- Results obtained from experimental studies confirm the simulation study. The voltages of the load at the PCC with high THD values of 18.39%, 24.12% and 30.17% are compensated by the proposed multilevel inverter based SAPF. After compensation, the THD values are respectively experimentally reduced to 1.53%, 2.44% and 2.60%. In both the simulation and experimental studies, the THD values of the load voltage are reduced to below 5% limits. This ensures that the proposed SAPF brings the THD values of highly distorted voltages into compliance with the IEEE-519 Standard.
- The system efficiency of the prototype is tabulated with the simulation results under three different circuit parameter sets. The experimental results verify the high values of the system efficiency in the simulations. The calculated efficiency values from the simulations are 98.86 %, 98.24% and 98.68%, while they are measured at 96.20%, 94.57% and 94.18% in the experiments.

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