JPE 17-4-3

https://doi.org/10.6113/JPE.2017.17.4.874
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Improved Control Strategy for T-type Isolated DC/DC Converters

Dong Liu†, Fujin Deng**, Yanbo Wang*, and Zhe Chen*

†,*Department of Energy Technology, Aalborg University, Aalborg, Denmark
**School of Electrical Engineering, Southeast University, Nanjing, China

Abstract

T-type isolated DC/DC converters have recently attracted attention due to their numerous advantages, including few components, low cost, and symmetrical operation of transformers. This study proposes an improved control strategy for increasing the efficiency of T-type isolated DC/DC converters. Under the proposed strategy, the primary circulating current flows through the auxiliary switches (metal–oxide–semiconductor field-effect transistors) instead of their body diodes in free-wheeling periods. Such feature can reduce conduction losses, thereby improving the efficiency of T-type isolated DC/DC converters. The operation principles and performances of T-type isolated DC/DC converters under the proposed control strategy are analyzed in detail and verified through the simulation and experimental results.

Key words: DC/DC converter, T-type, Zero-voltage switching (ZVS)

I. INTRODUCTION

High-power isolated DC/DC converters with high efficiency and high reliability are widely studied in the field of modern power electronics because of their known advantages of galvanic isolation and high voltage conversion rate, which make them applicable to electric vehicles, telecommunications, solar systems, fuel cell systems, and DC transmission systems [1]-[7].

The most popular and useful topologies of isolated DC/DC converters are the two-level zero-voltage switching (ZVS) DC/DC converters, including half-bridge (HB) ZVS DC/DC converters and full-bridge ZVS DC/DC converters with phase-shift control [8]-[12], which feature high power density, easy control strategy, and simple circuit structure. The three-level (TL) ZVS isolated DC/DC converter was proposed for high input voltage applications because voltage stresses on the power switches are only half of the input voltage and voltage stress on the transformer can be reduced in comparison with two-level ZVS DC/DC converters. Therefore, low-voltage stress switches with small on-state resistance can improve the efficiency of TL ZVS DC/DC converters [13]-[22]. Numerous studies on TL DC/DC converters have focused on extending the soft switching range [16], [17], reducing the circulating currents [18], [19], balancing the two input voltages [20], [21], and reducing the ripple currents on the input capacitors [22].

T-type converters are another type of TL converter that can also produce three voltage levels, and thus, have become popular in single or three-phase inverters [23–26]. However, only a few studies have discussed T-type isolated DC/DC converters. In [27], a dual active bridge isolated DC/DC converter with a TL T-type leg and a corresponding modulation strategy were proposed. T-type isolated DC/DC converters with asymmetrical duty ratio control were proposed in [28] and [29] for high power and high efficiency applications. Compared with conventional diode-clamped TL isolated DC/DC converters, T-type isolated DC/DC converters feature fewer components and a simpler circuit structure. Table I shows the comparison results of the numbers of primary circuit components of HB T-type isolated DC/DC converters and conventional HB diode-clamped TL isolated DC/DC converters [13]. T-type converters are derived from two-level converters, and thus, the main power switches in T-type converters must withstand input voltage. At present, conventional diode-clamped TL DC/DC converters are widely used in high input voltage applications [16]-[22] because their power switches are only required to

Manuscript received Jan. 22, 2017; accepted Apr. 18, 2017
Recommended for publication by Associate Editor Chun-An Cheng.
†Corresponding Author: dli@et.aau.dk
Tel: +45-25724264, Aalborg University
*Department of Energy Technology, Aalborg University, Denmark
** School of Electrical Engineering, Southeast University, China

TABLE I
COMPARISON OF NUMBERS OF PRIMARY CIRCUIT COMPONENTS

Component	HB diode-clamped TL isolated DC/DC converter [13]	HB T-type isolated DC/DC converter
Power Switch	4	4
Clamping Diode	2	0
Flying Capacitor	1	0
Input Capacitor	2	2

withstand half of the input voltage. However, with the development of silicon carbide (SiC) power devices, TL T-type DC/DC converters will be suitable for high input voltage applications because the drain–source breakdown voltage of SiC power devices is considerably higher than that of silicon (Si) power devices [30]. In addition, the isolation transformer of a T-type isolated DC/DC converter exhibits a symmetrical operation, which differs from that of an asymmetrical HB ZVS DC/DC converter whose transformer operates with DC current and flux offset [31].

In the present work, an improved control strategy is proposed to improve the efficiency of T-type isolated DC/DC converters. In conventional control strategies, the primary current flows through the body diodes of switches. By contrast, the primary current under the proposed control strategy flows through auxiliary switches, i.e., metal–oxide–semiconductor field-effect transistors (MOSFETs), in free-wheeling periods. Therefore, the proposed control strategy can effectively boost the efficiency of converters. In addition, the proposed control strategy can achieve ZVS, which can reduce switching losses. The operation principles and performances of T-type isolated DC/DC converters under the proposed control strategy are analyzed in detail. The proposed control strategy is also verified through the simulation and experimental results.

The rest of this paper is organized as follows. Section II presents an analysis of the operation principles of the proposed control strategy in detail. Section III discusses the analysis of the characteristics and performances of T-type isolated DC/DC converters under the proposed control strategy. Section IV cites the simulation and experimental results to verify the proposed control strategy. Finally, Section V describes the main contributions of this work.

II. OPERATION PRINCIPLES OF THE PROPOSED CONTROL STRATEGY

Fig. 1 shows the circuit structure of a T-type isolated DC/DC converter. At the primary side, C_1 and C_2 are two input capacitors that split the input voltage V_{in} into V_1 and V_2. S_1–S_4 are the power switches. D_1–D_4 are the diodes of S_1–S_4. C_{s1}–C_{s4} are the parasitic capacitors of S_1–S_4. T_r is the transformer. L_r is the leakage inductor of the transformer T_r. At the secondary side, D_{r1}–D_{r4} are four output rectifier diodes. L_o and C_o are the output filter inductor and capacitor,

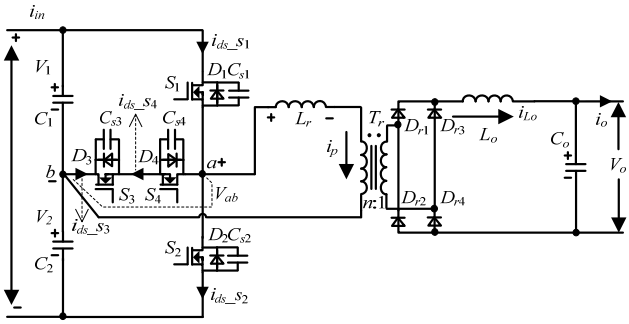


Fig. 1. Circuit structure of a T-type isolated DC/DC converter.

respectively. In Fig. 1, V_{in} is the input voltage; V_{ab} is the voltage between points a and b; i_p is the primary current of the transformer; i_{Lo} is the current flowing through the output filter inductor; V_o and i_o are the output voltage and current, respectively; and n is the turns ratio of the transformer T_r. i_{ds_S1}, i_{ds_S2}, i_{ds_S3}, and i_{ds_S4} are the currents flowing through (S_1, D_1), (S_2, D_2), (S_3, D_3), and (S_4, D_4), respectively. In the T-type isolated DC/DC converter, S_1 and S_2 are the main switches that withstand the input voltage, whereas S_3 and S_4 are the auxiliary switches that withstand only half of the input voltage. Hence, a low-voltage stress switch (MOSFET) can be used for S_3 and S_4 even in high-voltage applications.

Several assumptions are derived to simplify the theoretical analysis. 1) All the switches and diodes are ideal. 2) S_1 and S_2 have the same parasitic capacitor, and thus, $C_{s1} = C_{s2} = C_{j1}$. S_3 and S_4 have the same parasitic capacitor, and thus, $C_{s3} = C_{s4} = C_{j2}$. 3) The two input capacitors C_1 and C_2 are sufficiently large to be considered two voltage sources with the value of $V_{in}/2$. 4) The output filter inductor L_o is sufficiently large to be considered a constant current source.

Fig. 2 shows the operation principles of a conventional control strategy [28] and the proposed control strategy. In this figure, d_{rv1}–d_{rv4} are the driving signals of switches S_1–S_4; d_1 is the duty cycle of switches S_1 and S_2; i_{S1}, i_{S2}, i_{S3}, and i_{S4} are the currents flowing through switches S_1–S_4; i_{D1}, i_{D2}, i_{D3}, and i_{D4} are the currents flowing through diodes D_1–D_4; and d_{loss} is the duty cycle loss in one switching period.

1) *Conventional control strategy*, as shown in Fig. 2(a): The duty ratios of auxiliary swithes S_3 and S_4 are constant, and their values are both 0.5 if dead time is neglected. The output voltage V_o is controlled by adjusting the duty ratios of the main swithes S_1 and S_2 (d_1).

2) *Proposed control strategy*, as shown in Fig. 2(b): The driving signals of the switch pairs (S_2, S_3) and (S_1, S_4) are complementary. Therefore, time overlaps exist between the driving signals of auxiliary switches S_3 and S_4, as highlighted in Fig. 2(b). The output voltage V_o is also controlled by adjusting the duty ratios of main switches S_1 and S_2 (d_1).

The main difference between the two control strategies is the flow of currents through S_3, S_4 and D_3, D_4 (i_{S3}, i_{S4} and i_{D3}, i_{D4}), as highlighted in Fig. 2. In the conventional control strategy, the primary current i_p flows through the body diodes

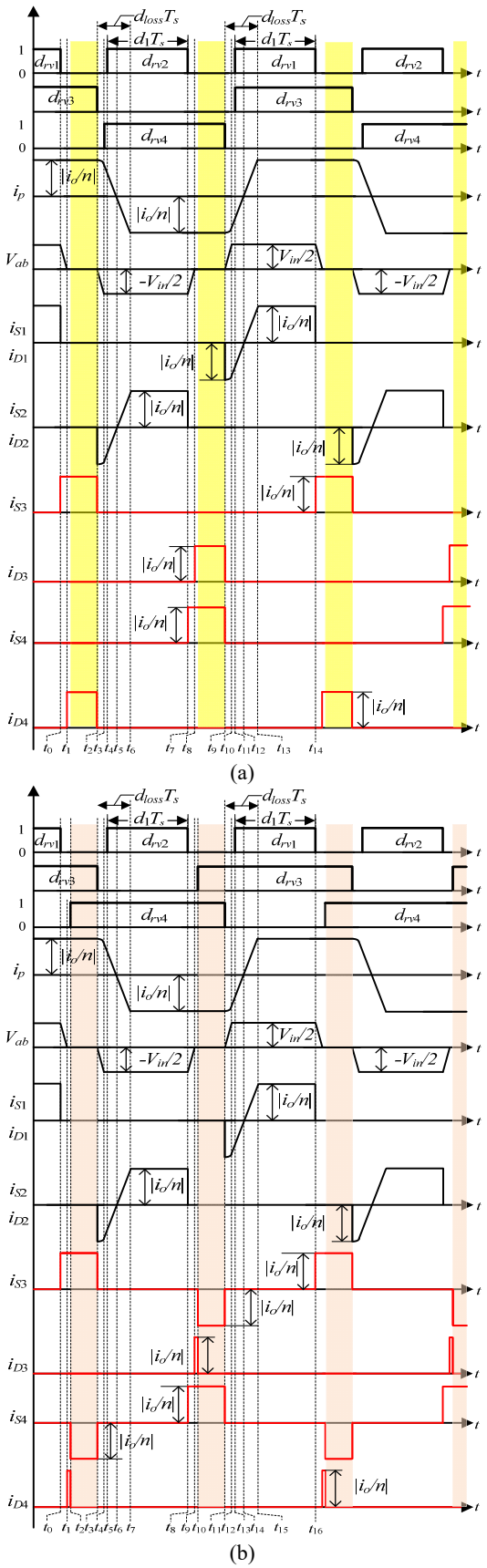


Fig. 2. Operation principles with main waveforms. (a) Conventional control strategy in [28]. (b) Proposed control strategy.

D_3 and D_4 in the free-wheeling periods, as highlighted in Fig. 2(a). Under the proposed control strategy, the primary current i_p mainly flows through switches S_3 and S_4 instead of body diodes D_3 and D_4 in the free-wheeling periods, as highlighted in Fig. 2(b). In general, the power losses of the switch (MOSFET) are smaller than those of the body diode when the same currents flow through them [32]. Consequently, the proposed control strategy effectively reduces conduction losses and improves the efficiency of the converter compared with the conventional control strategy.

Fig. 3 shows the equivalent circuits to explain the operation principles of the T-type isolated DC/DC converter under the proposed control strategy shown in Fig. 2(b).

Stage 0 [before t_0]: During this period, switches S_1 and S_3 are at the on-state. Thus, voltage V_{ab} is equal to $V_{in}/2$, and input power transfers to the load from D_{r1} and D_{r4}. In this stage, the primary current i_p is i_o/n.

Stage 1 [t_0–t_1]: Switch S_1 is turned off at t_0. Then, output current i_o is reflected onto the primary side. In this case, primary current i_p remains i_o/n to charge C_{s1} and discharge C_{s2} and C_{s4}. Therefore, the voltage of C_{s1} (V_{Cs1}) increases, whereas the voltages of C_{s2} (V_{Cs2}) and C_{s4} (V_{Cs4}) decrease.

Stage 2 [t_1–t_2]: V_{Cs1} increases to $V_{in}/2$ at t_1, and V_{Cs2} and V_{Cs4} decrease to $V_{in}/2$ and 0 V, respectively. Then, body diode D_4 conducts, thereby clamping V_{Cs4} at 0 V. During this stage, V_{ab} is maintained at 0 V, and i_p remains i_o/n and flows through S_3, D_4, L_r, and T_r. Therefore, the current on body diode D_4 (i_{D4}) is i_o/n.

Stage 3 [t_2–t_3]: Switch S_4 is turned on at zero voltage at t_2. Then, primary current i_p starts to flow through S_3, S_4, L_r, and T_r. During this stage, primary current i_p and voltage V_{ab} remain i_o/n and 0 V, respectively.

Stage 4 [t_3–t_4]: Switch S_3 is turned off at t_3. Then, the voltages of C_{s1} (V_{Cs1}) and C_{s3} (V_{Cs3}) increase, the voltage of C_{s2} (V_{Cs2}) decreases, and voltage V_{ab} starts to decrease. Primary current i_p starts to decrease and is insufficient to provide output current i_o. Thus, output rectifier diodes D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct simultaneously, thereby clamping both the primary and secondary voltages of the transformer at 0 V. Therefore, voltage V_{ab} is fully applied to L_r. During this stage, L_r resonates with C_{s1}, C_{s2}, and C_{s3}.

Stage 5 [t_4–t_5]: V_{Cs1} and V_{Cs3} increase to V_{in} and $V_{in}/2$, respectively, at t_4; and V_{Cs2} decreases to 0 V. Then, body diode D_2 begins to conduct, thereby clamping V_{Cs2} at 0 V. Voltage V_{ab} decreases to $-V_{in}/2$. During this stage, 1) the primary current i_p flows through C_2, D_2, L_r, and T_r, in which case the current on the body diode D_2 (i_{D2}) is equal to i_p. In addition, 2) output rectifier diodes D_{r1}, D_{r2}, D_{r3}, and D_{r4} continue to conduct, and thus, the voltage on L_r is $-V_{in}/2$, and i_p decreases linearly.

Stage 6 [t_5–t_6]: Switch S_2 is turned on at zero voltage at t_5, and primary current i_p goes through C_2, S_2, L_r, and T_r. During this stage, primary current i_p continues to decrease linearly.

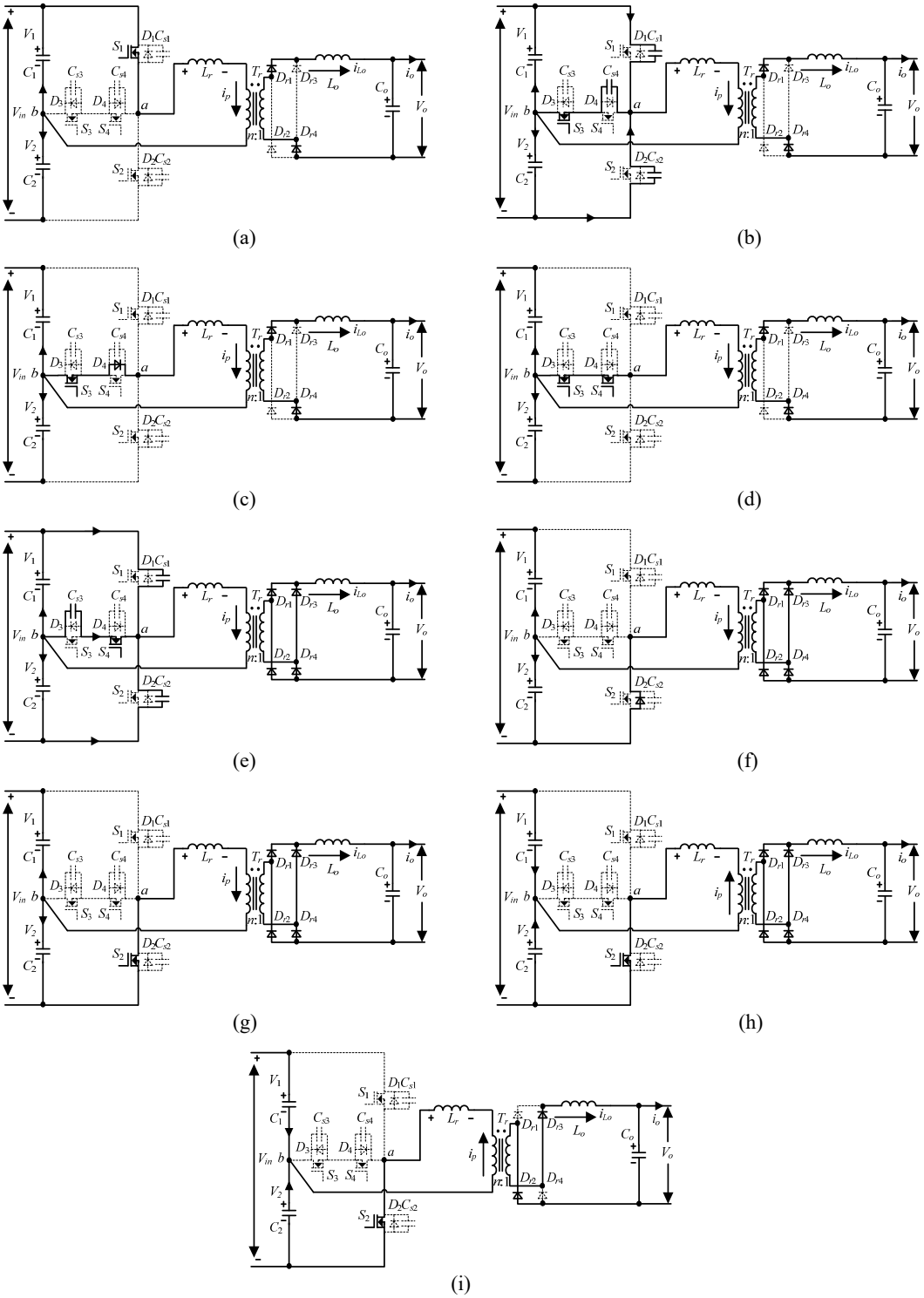


Fig. 3. Equivalent circuits under the proposed control strategy. (a) [before t_0]. (b) [t_0–t_1]. (c) [t_1–t_2]. (d) [t_2–t_3]. (e) [t_3–t_4]. (f) [t_4–t_5]. (g) [t_5–t_6]. (h) [t_6–t_7]. (i) [t_7–t_8].

Stage 7 [t_6–t_7]: Primary current i_p decreases to 0 A at t_6, which indicates that the current direction of i_p changes. The voltage on L_r remains $-V_{in}/2$. Therefore, i_p still decreases linearly.

Stage 8 [t_7–t_8]: Primary current i_p decreases at t_7 to the negative reflected output current whose value is $-i_o/n$. Then, D_{r1} and D_{r4} are turned off, and input power begins to transfer to the load from D_{r2} and D_{r3}.

Switch S_2 is turned off at t_8. The second half cycle [t_8–t_{16}] starts. The following analysis is similar to that of the first half cycle [t_0–t_8], which is not repeated in this section.

III. CHARACTERISTIC ANALYSIS OF THE PROPOSED CONTROL STRATEGY

A. Voltage Stresses of Switches

In the T-type isolated DC/DC converter under the proposed control strategy, main switches S_1 and S_2 withstand the full input voltage (V_{in}), but auxiliary switches S_3 and S_4 are only required to withstand half of the input voltage ($V_{in}/2$). Hence, the low-voltage stress switch (MOSFET) can be selected for auxiliary switches S_3 and S_4.

B. Duty Cycle Loss

In Fig. 2(b), the periods [t_3–t_7] and [t_{11}–t_{15}] are the times of the duty cycle losses in one switching period. In general, the periods [t_3–t_4] and [t_{11}–t_{12}] are sufficiently short to be neglected; thus, [t_3–t_7] and [t_{11}–t_{15}] can be calculated by

$$t_7 - t_3 = t_{15} - t_{11} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in}}. \quad (1)$$

In accordance with (1), the duty cycle loss d_{loss} shown in Fig. 2(b) can be obtained as

$$d_{loss} = \frac{t_7 - t_3}{T_s} = \frac{t_{15} - t_{11}}{T_s} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}. \quad (2)$$

C. Output Characteristic

When duty cycle loss is considered, the average output voltage V_o can be calculated by

$$V_o = \frac{V_{in}}{n} \cdot (d_1 - d_{loss}) = \frac{V_{in}}{n} \cdot (d_1 - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}). \quad (3)$$

In accordance with (3), the duty ratio d_1 shown in Fig. 2 can be expressed by

$$d_1 = \frac{V_o \cdot n}{V_{in}} + \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}. \quad (4)$$

D. Currents through Switches and Body Diodes

1) Conventional Control Strategy: In the conventional control strategy shown in Fig. 2(a), the root mean square (RMS) values of the currents through switches S_3 and S_4, namely, $i_{S3\_rms\_con}$ and $i_{S4\_rms\_con}$, can be given by

$$i_{S3\_rms\_con} = i_{S4\_rms\_con} = \frac{i_o}{n} \cdot \sqrt{(0.5 - d_1)}. \quad (5)$$

When (4) is substituted into (5), (5) can be rewritten as

$$i_{S3\_rms\_con} = i_{S4\_rms\_con} = \frac{i_o}{n} \cdot \sqrt{(0.5 - \frac{V_o \cdot n}{V_{in}} - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s})}. \quad (6)$$

In practical operations, the periods [t_0–t_1] and [t_7–t_8] shown in Fig. 2(a) are significantly short. If these periods are neglected, then the average values of the currents flowing through body diodes D_3 and D_4, namely, $i_{D3\_avg\_con}$ and $i_{D4\_avg\_con}$, can be given by

$$i_{D3\_avg\_con} = i_{D4\_avg\_con} = \frac{i_o}{n} \cdot (0.5 - d_1). \quad (7)$$

When (4) is substituted into (7), (7) can be rewritten as

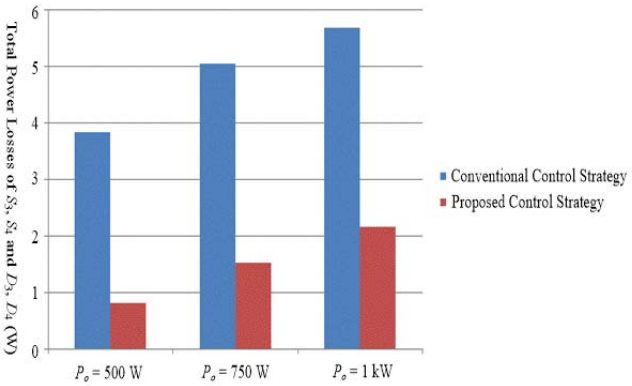


Fig. 4. Theoretical calculation results for the total power losses of S_3, S_4 and D_3, D_4 when V_{in} = 400 V and V_o = 50 V.

$$i_{D3\_avg\_con} = i_{D4\_avg\_con} = \frac{i_o}{n} \cdot (0.5 - \frac{V_o \cdot n}{V_{in}} - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}). \quad (8)$$

2) Proposed Control Strategy: In the proposed control strategy shown in Fig. 2(b), the periods [t_0–t_2] and [t_8–t_{10}] are dead times and typically short. If these dead times are neglected, then the RMS values of the currents flowing through switches S_3 and S_4, namely, $i_{S3\_rms\_pro}$ and $i_{S4\_rms\_pro}$, can be given by

$$i_{S3\_rms\_pro} = i_{S4\_rms\_pro} = \frac{i_o}{n} \cdot \sqrt{(1 - 2 \cdot d_1)}. \quad (9)$$

When (4) is substituted into (9), (9) can be rewritten as

$$i_{S3\_rms\_pro} = i_{S4\_rms\_pro} = \frac{i_o}{n} \cdot \sqrt{(1 - \frac{2 \cdot V_o \cdot n}{V_{in}} - \frac{8 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s})}. \quad (10)$$

The dead times [t_0–t_2] and [t_8–t_{10}] are typically short in practical operations; hence, the average values of the currents flowing through body diodes D_3 and D_4 are extremely small, as shown in Fig. 2(b). Therefore, in the proposed control strategy, the circulating currents mainly flow through switches S_3 and S_4 instead of body diodes D_3 and D_4 in free-wheeling periods.

From (5)-(10) and the circuit parameters of the experimental prototype in the Appendix, the theoretical calculation results for the total power losses of switches S_3 and S_4 and their body diodes D_3 and D_4 (MOSFETs) [33] are presented in Fig. 4, which also shows the results with various output powers, including 500 W, 750 W, and 1 kW. As shown in Fig. 4, the total power losses of switches S_3 and S_4 and their body diodes D_3 and D_4 (MOSFETs) under the proposed control strategy are considerably lower than those under the conventional control strategy.

E. ZVS Achievement Conditions

1) Main Switches S_1 and S_2: The energy stored in the leakage inductance (and the resonant inductor, if added to the circuit) is used to achieve the zero-voltage switch-on for main switches S_1 and S_2. Then, (11) should be satisfied to achieve the zero-voltage switch-on of switches S_1 and S_2.

$$\frac{1}{2}L_r\cdot\left(\frac{i_o}{n}\right)^2 \ge \frac{1}{2}\cdot C_{s2}\cdot\left(\frac{V_{in}}{2}\right)^2+\frac{1}{2}\cdot C_{s3}\cdot\left(\frac{V_{in}}{2}\right)^2+\frac{1}{2}\cdot C_{s1}\cdot\left(V_{in}^2-\left(\frac{V_{in}}{2}\right)^2\right)$$
$$=\frac{1}{2}\cdot C_{j1}\cdot V_{in}^2+\frac{1}{8}\cdot C_{j2}\cdot V_{in}^2 \tag{11}$$

In accordance with (11), the leakage inductance L_r should satisfy (12) to realize the zero-voltage switch-on of main switches S_1 and S_2 under a certain output power.

$$L_r \ge \frac{n^2\cdot V_{in}^2\cdot(4\cdot C_{j1}+C_{j2})}{4\cdot i_o^2} \tag{12}$$

2) Auxiliary Switches S_3 and S_4: The zero-voltage switch-on of auxiliary switches S_3 and S_4 are mainly determined by the reflected current from the output filter inductor. In general, the output filter inductance is sufficiently large to enable switches S_3 and S_4 to achieve zero-voltage switch-on even at a light load. For example, energy E_1 is required to discharge parasitic capacitors C_{s2} and C_{s4}, and charge parasitic capacitor C_{s1} to ensure the zero-voltage switch-on of switch S_4. The expression is as follows:

$$E_1 \ge \frac{1}{2}\cdot C_{s1}\cdot\left(\frac{V_{in}}{2}\right)^2+\frac{1}{2}\cdot C_{s4}\cdot\left(\frac{V_{in}}{2}\right)^2+\frac{1}{2}\cdot C_{s2}\cdot\left(V_{in}^2-\left(\frac{V_{in}}{2}\right)^2\right)$$
$$=\frac{1}{2}\cdot C_{j1}\cdot V_{in}^2+\frac{1}{8}\cdot C_{j2}\cdot V_{in}^2 \tag{13}$$

IV. Simulation and Experimental Verification

A. Simulation Verification

A simulation model is built in PLECS® to verify the proposed control strategy. The model parameters are listed in the Appendix. In the simulation, the input voltage V_{in} is 400 V, the output voltage V_o is 50 V, and the output power P_o is 500 W. Figs. 5(a) and 5(b) show the simulation results under the conventional control strategy in [28] and the proposed control strategy, respectively. In the figures, i_{ds_S1} and i_{ds_S2} are the currents flowing through (S_1, D_1) and (S_2, D_2), i_{S3} and i_{S4} are the currents flowing through switches S_3 and S_4, and i_{D3} and i_{D4} are the currents flowing through body diodes D_3 and D_4 of S_3 and S_4.

As shown in the highlighted areas in Fig. 5(a), primary current i_p flows through body diodes D_3 and D_4 in the free-wheeling periods under the conventional control strategy. By contrast, under the proposed control strategy, primary current i_p goes through switches S_3 and S_4 in the free-wheeling periods, as shown in the highlighted areas in Fig. 5(b). Such characteristic can effectively reduce conduction losses and improve the efficiency of converters.

B. Experimental Verification

A 1 kW experimental prototype is established to verify the proposed control strategy. The circuit parameters of the prototype are listed in the Appendix. Fig. 6 shows the hardware of the established experimental prototype, which is controlled by dSPACE in the experiments. In the following experiments, a single PI control loop is designed to control the output voltage V_o by adjusting the duty ratio d_1 shown in Fig. 2.

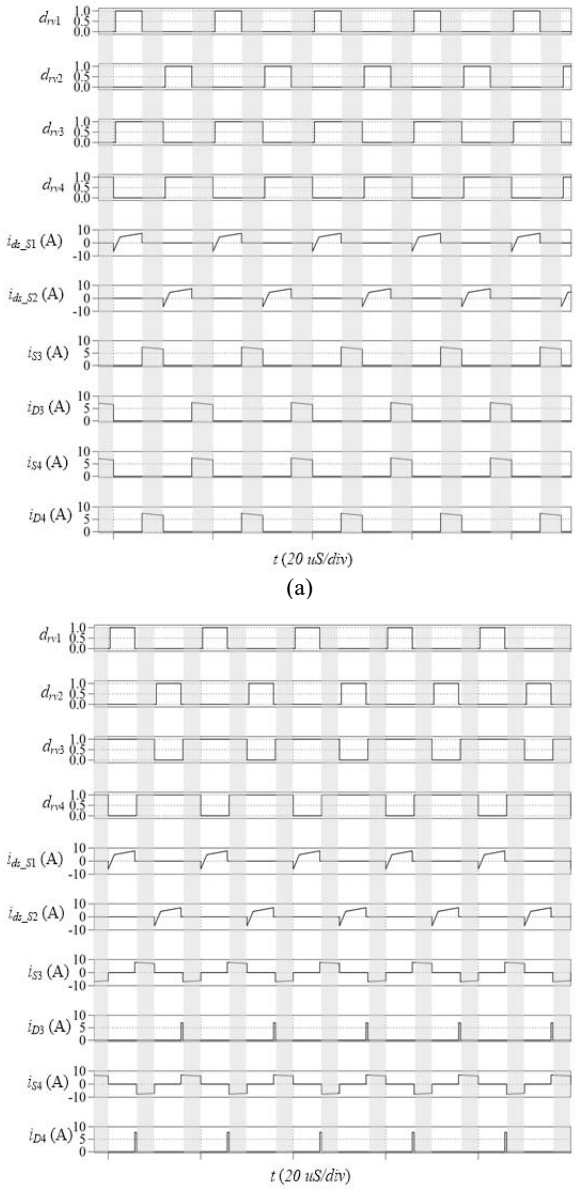


Fig. 5. Simulation results when V_{in} = 400 V, V_o = 50 V, and P_o = 500 W. (a) Conventional control strategy in [28]. (b) Proposed control strategy.

Fig. 7 shows the experimental results, including V_{in}, V_o, V_{ab}, and i_p, under the proposed control strategy when the output power P_o is 1 kW, the input voltage V_{in} is 400 V, and the output voltage V_o is 50 V.

Figs. 8 and 9 show the comparison between the conventional control strategy in [28] and the proposed control strategy. In this work, i_{ds_S3} and i_{ds_S4} are the currents of (S_3, D_3) and (S_4, D_4), respectively. i_{ds_S3} and i_{ds_S4} are highly

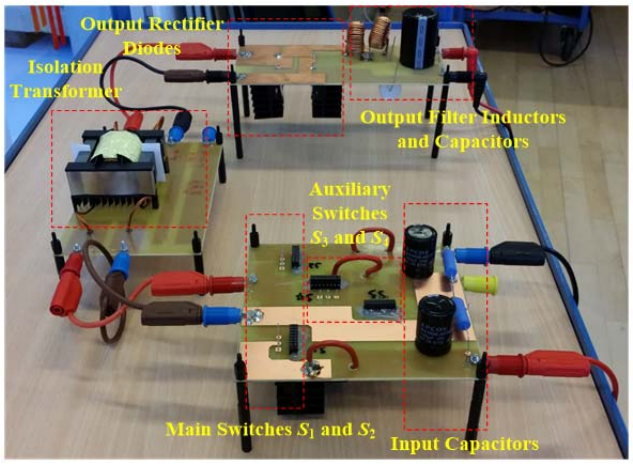


Fig. 6. Hardware of the established experimental prototype.

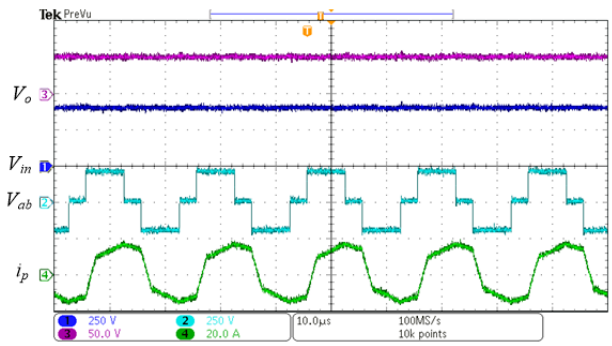


Fig. 7. Experimental results, including V_{in}, V_o, V_{ab}, and i_p, under the proposed control strategy when V_{in} = 400 V, V_o = 50 V, and P_o = 1 kW.

similar, and thus, only i_{ds_S4} is presented in this paper for explanation. Figs. 8 and 9 indicate the following. 1) The values of i_{ds_S2} are the same in the two control strategies. 2) Under the conventional control strategy, i_{ds_S4} flows through body diode D_4 in the free-wheeling periods, as highlighted in Figs. 7(a) and 8(a), because S_4 is turned off. 3) Under the proposed control strategy, i_{ds_S4} flows through switch S_4 in the free-wheeling periods, as highlighted in Figs. 7(b) and 8(b), because S_4 is turned on. The analysis in 2) and 3) indicates that the efficiency of converters improves more evidently under the proposed control strategy than under the conventional control strategy because the power loss of the switch is smaller than that of its body diode when the same currents flow through them.

Figs. 10–11 show the achieved ZVS conditions of the T-type isolated DC/DC converter under the proposed control strategy. Fig. 10 shows the primary current i_p, primary voltage V_{ab}, driving signal Vgs_S_1, and drain–source voltage $V_{ds}\_S_1$ of the main power switch S_1, which realizes ZVS at 500 W and 1 kW.

In Fig. 10, the energy from the leakage inductance of the transformer is provided for main switch S_1 to achieve the zero-voltage switch-on. Fig. 11 shows the primary current i_p,

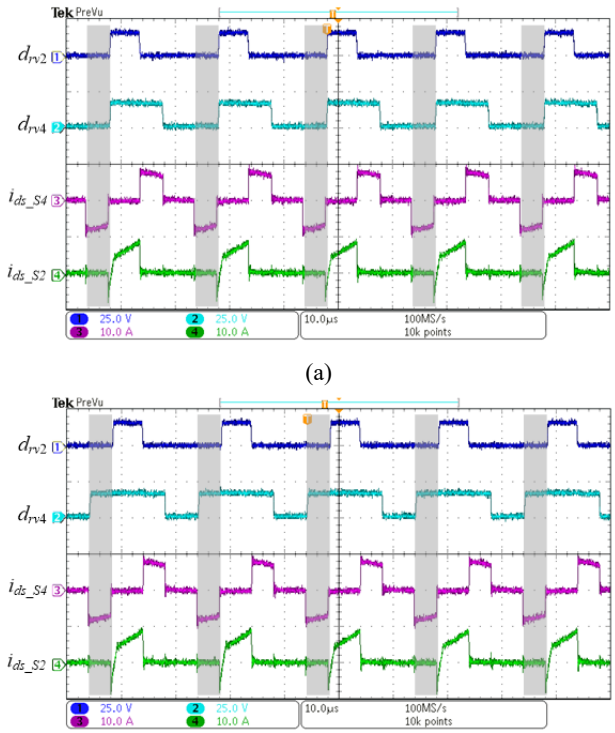


Fig. 8. Experimental results when V_{in} = 400 V, V_o = 50 V, and P_o = 500 W. (a) Conventional control strategy in [28]. (b) Proposed control strategy.

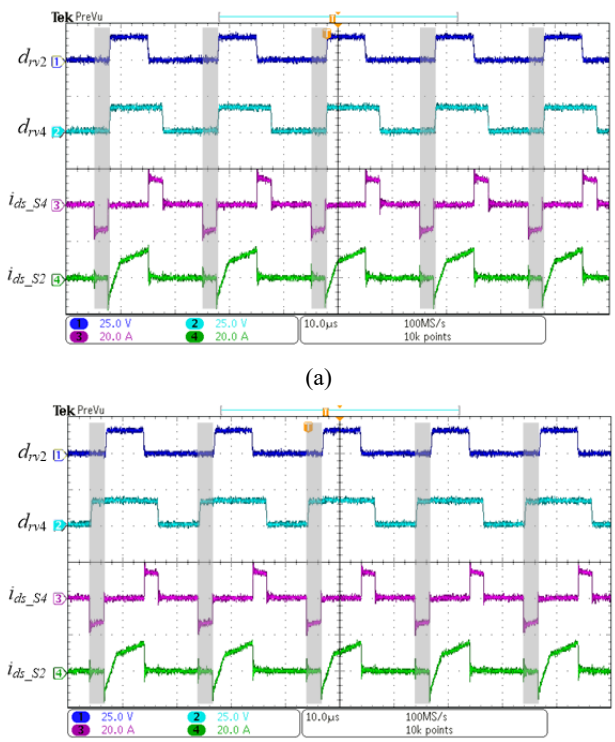
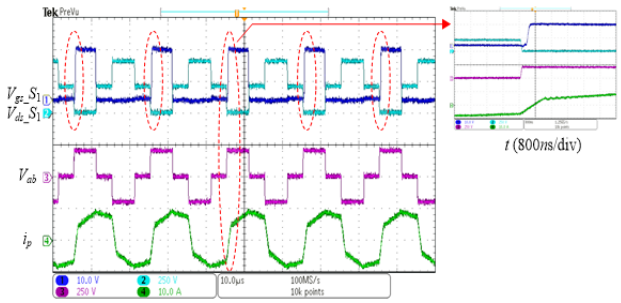
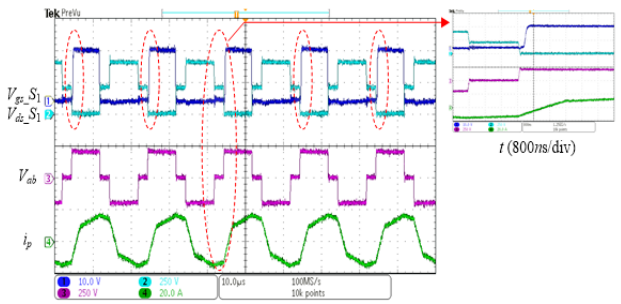


Fig. 9. Experimental results when V_{in} = 400 V, V_o = 50 V, and P_o = 1 kW. (a) Conventional control strategy in [28]. (b) Proposed control strategy.

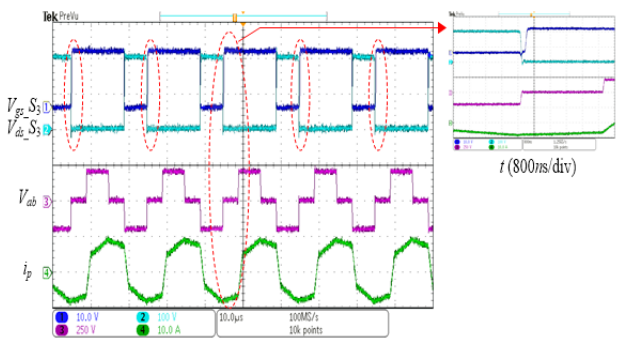


(a)

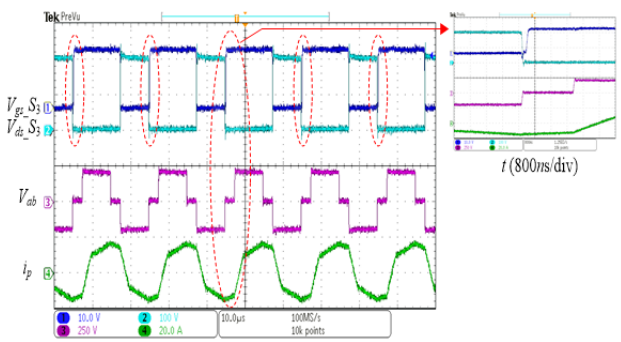


(b)

Fig. 10. Achieved ZVS conditions for switch S_1 when V_{in} = 400 V and V_o = 50 V. (a) At 500 W. (b) At 1 kW.



(a)



(b)

Fig. 11. Achieved ZVS conditions for switch S_3 when V_{in} = 400 V and V_o = 50 V. (a) At 500 W. (b) At 1 kW.

primary voltage V_{ab}, driving signal $V_{gs}\_S_3$, and drain–source voltage $V_{ds}\_S_3$ of auxiliary power switch S_3, which realizes ZVS at 500 W and 1 kW. In Fig. 11, the energy from both the output filter inductance and leakage inductance of the

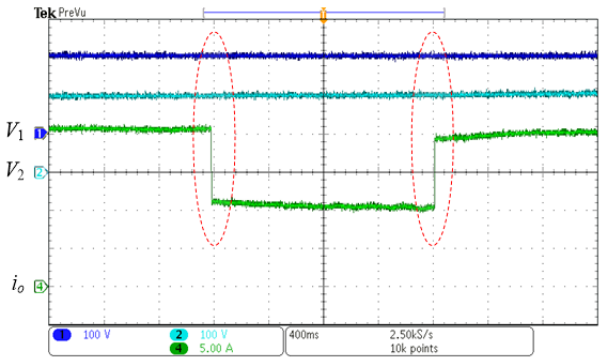


Fig. 12. Dynamic performance under load changes when V_{in} = 400 V and V_o = 50 V.

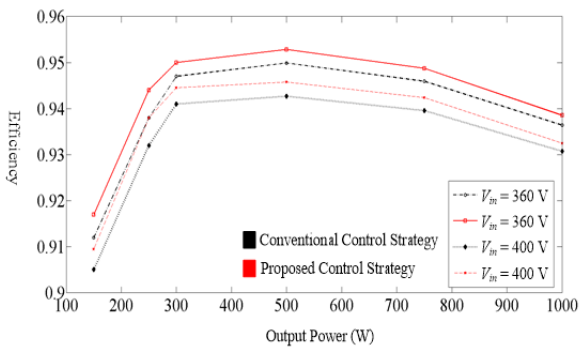


Fig. 13. Efficiency curves with various input voltages when V_o = 50 V.

transformer is provided for auxiliary switch S_3 to achieve zero-voltage switch-on. The achieved ZVS conditions of switches S_2 and S_4 are similar to those of switches S_1 and S_3, respectively, which are not repeated in this paper.

Fig. 12 shows the dynamic performance of the proposed control strategy. In this figure, the output load changes from 1 kW to 500 W and finally returns to 1 kW when the input voltage V_{in} is 400 V and the output voltage V_o is 50 V. As shown in Fig. 12, the voltages of the two input capacitors V_1 and V_2 are all kept constant under the proposed control strategy when load changes.

Fig. 13 shows the efficiency curves with the various input voltages when the output voltage V_o is 50 V. The maximum efficiency under the proposed control strategy is over 95%. As shown in Fig. 13, the efficiencies of the proposed control strategy are higher than those of the conventional control strategy. This outcome is consistent with the result of the theoretical analysis. Fig. 14 shows the calculated power loss distribution when input voltage V_{in} is 400 V, output voltage V_o is 50 V, and output power P_o is 1 kW. The conduction loss of the auxiliary switches is decreased because of the reduced conduction losses in the free-wheeling periods under the proposed control strategy. Such reduction improves the efficiency of converters. The increased efficiency under the proposed control strategy becomes particularly evident with increasing input power.

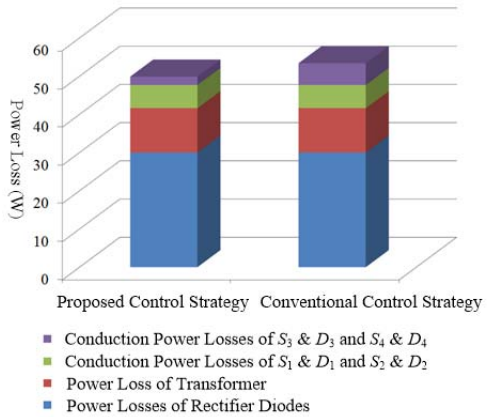


Fig. 14. Calculated power loss distribution when V_{in} = 400 V, V_o = 50 V, and P_o = 1 kW.

V. CONCLUSIONS

An improved control strategy is proposed to enhance the efficiency of T-type isolated DC/DC converters. Under the proposed control strategy, the primary current flows through the auxiliary switches (MOSFETs) instead of their body diodes in the free-wheeling periods. In addition, ZVS can be realized under the proposed control strategy, in which the achieved ZVS conditions are the same as those under the conventional control strategy. The conduction losses of the auxiliary switches are reduced, and the efficiency of converters can be effectively increased under the proposed control strategy compared with the conventional control strategy. The operation principles and performances of the proposed control strategy are analyzed in detail. Finally, the effectiveness and feasibility of the proposed control strategy are verified through the simulation and experimental results.

APPENDIX

TABLE II
PARAMETERS OF THE SIMULATION MODEL AND EXPERIMENTAL PROTOTYPE

Component	Description
Main Switches S_1 and S_2	IPW60R041C6
Auxiliary Switches S_3 and S_4	IRFP4868PBF
Output Rectifier Diodes D_{r1}–D_{r4}	MBR40250TG
Turns Ratio of the Transformer T_r (n)	20:12
Leakage Inductance L_r (uH)	24
Input Capacitors C_1 and C_2 (uF)	100
Output Filter Inductor L_o (uH)	140
Output Filter Capacitor C_o (uF)	470
Switching Frequency (kHz)	50
Dead Time (nS)	400

REFERENCES

[1] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, Vol. 19, No. 5, pp. 1184-1194, Sep. 2004.

[2] M. Yilmaz and P. T. Krein, "Review of the impact of vehicle-to-grid technologies on distribution systems and utility interfaces", *IEEE Trans. Power Electron.*, Vol. 28, No. 12, pp. 5673-5689, Dec. 2013.

[3] S. Y. Kim, H. S. Song, and K. Nam, "Idling port isolation control of three-port bidirectional converter for EVs", *IEEE Trans. Power Electron.*, Vol. 27, No. 5, pp. 2495-2506, May 2012.

[4] T. Hirose and H. Matsuo, "Standalone hybrid wind-solar power generation system applying dump power control without dump load", *IEEE Trans. Ind. Electron.*, Vol. 59, No. 2, pp. 988-997, Feb. 2012.

[5] H. Wu, P. Xu, H. Hu, Z. Zhou, and Y. Xing, "Multiport converters based on integration of full-bridge and bidirectional DC-DC topologies for renewable generation systems", *IEEE Trans. Ind. Electron.*, Vol. 61, No. 2, pp. 856-869, Feb. 2014.

[6] Z. Liang, R. Guo, J. Li, and A. Q. Huang, "A high-efficiency PV module integrated DC/DC converter for PV energy harvest in FREEDM systems," *IEEE Trans. Power Electron.*, Vol. 26, No. 3, pp. 897-909, Mar. 2011.

[7] D. Liu, F. Deng, and Z. Chen, "Five-level active-neutral-point-clamped DC/DC converter for medium voltage DC grids," *IEEE Trans. Power Electron.*, Vol. 32, No. 5, pp. 3402-3412, May 2017.

[8] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC-DC converter based on dual-phase-shift control for DC distribution application", *IEEE Trans. Power Electron.*, Vol. 28, No. 4, pp. 1711-1727, Apr. 2013.

[9] C. Mi, H. Bai, C. Wang, and S. Gargies, "Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter," *IET Power Electron.*, Vol. 1, No. 4, pp. 507-517, Dec. 2008.

[10] U. Prasanna and A. Rathore, "Extended range ZVS active-clamped current-fed full-bridge isolated DC/DC converter for fuel cell applications: Analysis, design and experimental results," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 7, pp. 2661-2672, Jul. 2013.

[11] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 7, pp. 2745-2760, Jul. 2012.

[12] F. Sedaghati, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Extended configuration of dual active bridge DC-DC converter with reduced number of switches," *IET Power Electron.*, Vol. 8, No. 3, pp. 401-416, Mar. 2015.

[13] F. Canales, P. Barbosa, and F. C. Lee, "A zero-voltage and zero-current switching three-level DC/DC converter," *IEEE Trans. Power Electron.*, Vol. 17, No. 6, pp. 898-904, Nov. 2002.

[14] X. Ruan, B. Li,Q. Chen, S. C. Tan, and C.K. Tse, "Fundamental considerations of three-level DC-DC converters: Topologies, analyses, and control," *IEEE Trans. Circuits Syst. I, Reg. Papers.*, Vol. 55, No. 11, pp. 3733-3743, Dec. 2008.

[15] B. Lin and C. Chao, "Analysis of an interleaved three-level ZVS converter with series-connected transformers," *IEEE Trans. Power Electron.*, Vol. 28, No. 7, pp. 3088-3099, Jul. 2013.

[16] Y. Shi, and X. Yang, "Wide range soft switching PWM three-level DC-DC converters suitable for industrial applications," *IEEE Trans. Power Electron.*, Vol. 29, No.

2, pp. 603-616, Feb. 2014.
[17] Y. Jang, and M. Jovanovic, "A new three-level soft-switched converter," *IEEE Trans. Power Electron*., Vol. 20, No. 1, pp. 75-81, Jan. 2005.
[18] W. Li, S. Zong, F. Liu, H. Yang, X. He, and B. Wu, "Secondary-side phase-shift-controlled ZVS DC/DC converter with wide voltage gain for high input voltage applications," *IEEE Trans. Power Electron*., Vol. 28, No. 11, pp. 5128-5139, Nov. 2013.
[19] Z. Guo, K. Sun, and D. Sha, "Improved ZVS three-level DC-DC converter with reduced circulating loss," *IEEE Trans. Power Electron*., Vol. 31, No. 9, pp. 6394-6404, Dec. 2015.
[20] X. Yu, K. Jin, and Z. Liu, "Capacitor voltage control strategy for half-bridge three-level DC/DC converter," *IEEE Trans. Power Electron*., Vol. 29, No. 4, pp. 1557-1561, Apr. 2014.
[21] B. Lin and S. Zhang, "Analysis and implementation of a three-level hybrid DC-DC converter with the balanced capacitor voltages," *IET Power Electron*., Vol. 9, No. 3, pp. 457-465, Mar. 2016.
[22] D. Liu, F. Deng, Z. Gong, and Z. Chen, "Input-parallel output-parallel (IPOP) three-level (TL) DC/DC converters with interleaving control strategy for minimizing and balancing capacitor ripple currents," *IEEE J. Emerg. Sel. Topics Power Electron*., to be published. DOI: 10.1109/JESTPE.2017.2649221.
[23] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications", *IEEE Trans. Power Electron*., Vol. 28, No. 2, pp. 899-907, Feb. 2013.
[24] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Reliability improvement of a T-type three-level inverter with fault-tolerant control strategy," *IEEE Trans. Power Electron*., Vol. 30, No. 5, pp. 2660-2673, May 2015.
[25] G. H. Aghdam, "Optimised active harmonic elimination technique for three-level T-type inverters," *IET Power Electron*., Vol. 6, No. 3, pp. 425-433, Mar. 2013.
[26] P. Alemi, S.-Y. Jeong, and D.-C. Lee, "Active damping of LLCL filters using PR control for grid-connected three-level T-type converters," *Journal of Power Electronics*, Vol. 15, No. 3, pp. 786-795, May 2015.
[27] G. E. Sfakianakis, J. Everts, H. Huisman, T. Borrias, C. G. E. Wijnands, and E. A. Lomonova, "Charge-based ZVS modulation of a 3-5 level bidirectional dual active bridge DC-DC converter," *in Proc. Energy Conversion Congress and Exposition*, 2016.
[28] D. G. Bandeira, S. A. Mussa, and I. Barbi, "A ZVS-PWM T-type isolated DC-DC converter," in *Proc. 1th Annu. Southern Power Electron*, Nov/Dec. 2015.
[29] D. G. Bandeira and I. Barbi, "A T-type isolated zero voltage switching DC-DC converter with capacitive output," *IEEE Trans. Power Electron.*, to be published.
[30] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron*., Vol. 29, No. 5, pp. 2155-2163, May 2014.
[31] I. O. Lee and G. W. Moon, "A new asymmetrical half-bridge converter with zero DC-offset current in transformer," *IEEE Trans. Power Electron*., Vol. 28, No. 5, pp. 2297-2306, May 2013.
[32] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Design considerations and performance evaluations of synchronous rectifications in flyback converters," *IEEE Trans. Power Electron*., Vol. 13, No. 3, pp. 538-546, May 1998.
[33] D. Graovac, M. Purschel, and A. Kiep, "MOSFET power losses calculation using the data-sheet parameters," *Infineon Technol*., Dresden,Germany, Jul. 2006, Appl. note.

Dong Liu obtained a B.Eng. and an M.Sc. in electrical engineering from South China University of Technology, Guangdong, China, in 2008 and 2011, respectively. He is currently pursuing a Ph.D. in the Department of Energy Technology, Aalborg University, Denmark. From 2011 to 2014, he was an R&D engineer in Emerson Network Power Co., Ltd., Shenzhen, China. His main research interests include renewable energy technology, multilevel converters, and DC/DC converters.

Fujin Deng obtained a B.Eng. in electrical engineering from China University of Mining and Technology, Jiangsu, China, in 2005; an M.Sc. in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008; and a Ph.D. in energy technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012. He joined Southeast University, Nanjing, China in 2017 and is currently a professor in the university's School of Electrical Engineering. From 2013 to 2015 and from 2015 to 2017, he was a postdoctoral researcher and an assistant professor, respectively, in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His main research interests include wind power generation, multilevel converters, high-voltage direct current technology, DC grid, and offshore wind farm–power systems dynamics.

Yanbo Wang obtained an M.S. in electrical engineering from the Electrical Engineering School, Southwest Jiaotong University, Chengdu, China, in 2011. He is currently pursuing a Ph.D. in the Department of Energy Technology, Aalborg University, Denmark. His research interests include harmonic analysis and mitigation in power electronic-fed power systems, distributed power generation systems, microgrids, power system state estimation, and stability analysis.

Zhe Chen obtained a B.Eng. and an M.Sc. in electrical engineering from Northeast China Institute of Electric Power Engineering, Jilin City, China; an MPhil in power electronics from Staffordshire University, England; and a Ph.D. in power and control from the University of Durham, England. Dr. Chen is a full professor at the Department of Energy Technology, Aalborg University, Denmark. He is the head of the Wind Power System Research Program at the Department of Energy Technology, Aalborg University and the Danish principal investigator for wind energy at the Sino–Danish Center for Education and Research. His research areas are power systems, power electronics, and electric machines; and his current research interests are wind energy and modern power systems. He has led many research projects and has over 400 technical publications with more than 10000 citations and an h-index of 44 (Google Scholar). Dr. Chen is an associate editor of the IEEE Transactions on Power Electronics, a fellow of the Institution of Engineering and Technology (London, UK), and a chartered engineer in the UK.