

An Interleaving Scheme for DC-link Current Ripple Reduction in Parallel-Connected Generator Systems

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Abstract

This paper presents an interleaving scheme for parallel-connected power systems to reduce the DC-link current ripple. A paralleled generator system generates current ripple by the Pulse Width Modulation (PWM) of each generator side converter. The current ripple in the DC-link degrades the efficiency of the whole generator system and decreases the lifetime of the DC-link capacitors. To mitigate these issues, the expression of the DC-link current is derived by a double-integral Fourier analysis while considering the modulation schemes. Optimized interleaving angles for the parallel generator system are obtained based on an analysis to minimize the dominant current harmonics component. Finally, the proposed interleaving scheme reduces the RMS value of the DC-link current ripple. Simulation and experimental results verify the effectiveness of the proposed interleaving scheme.

Key words: Double-integral Fourier analysis, DC-link current ripple, Interleaving scheme, Parallel-connected generator systems

I. INTRODUCTION

The capacity of power converters has increased rapidly with the increased energy demand of generator systems. Many studies have been presented on the design of high voltage and high current converters [1]-[6]. One solution is the parallel connection of multiple lower power units [7]. Without the current pressure increase of a single switching device, parallel operation can effectively increase the total current. In addition, converter capacity can also be extended by using available power semiconductors.

When N power devices are connected in parallel, the rated current of each power device can be reduced to 1/N. Instead of a simple diode rectifier, a back-to-back power converter with a generator-side inverter can be applied in generator systems due to several advantages such as a high power factor, a high efficiency and bidirectional power flow capability [8]-[10]. However, when the N-parallel power converters consist of two-level back-to-back converters, as

shown in Fig. 1, a summation of the currents harmonics from each converter generates current ripple for a common DC-link capacitor. The current harmonics are generated as a result of the PWM switching in each generator side converter. The current ripple causes an increase of the internal temperature, and a decrease of the capacitor lifetime. In addition, it also aggravates the reliability and power loss of the generator system. Therefore, a DC-link current ripple reduction scheme is necessary in N-parallel connected generator systems.

As mentioned earlier, the DC-link current in a parallel system is generated by a summation of the current harmonics from the connected converters. Under this circumstance, the phase-shifted switching cycles lead to variations of the current ripple. Thus, using an interleaving method with an optimal angle can effectively reduce the current ripple [11], [12]. Refs. [13]-[18] discussed the performance of an interleaving scheme in a parallel system, and Ref. [16] provided examples of 3-parallel-connected photovoltaic modules. Furthermore, Ref. [17] verifies the performance of an interleaving scheme with a current ripple analysis in a parallel voltage-source converter system. In addition, Ref. [18] applied an interleaving scheme to a hybrid electric vehicle, while considering the operation mode of the motor.

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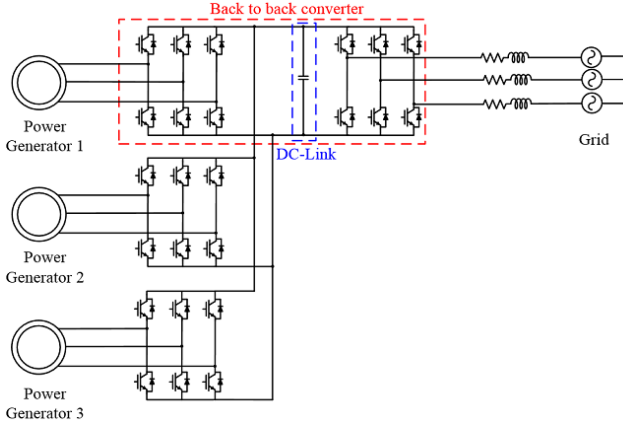


Fig. 1. 3-parallel-connected generator topology.

However, the authors did not provide experimental results. Although many methods have been proposed for DC-link current ripple reduction in various applications, there is not much discussion or analysis of generator applications. In addition, wind generators systems [2], hydropower generators systems [19], engine generators systems [20] and so on are commonly used generator applications that use a permanent magnet synchronous generator (PMSG) with a back-to-back topology. However, there is no research on the DC-link current ripple reduction method when it is connected in parallel. As a result, a current ripple reduction method that considers the characteristics of the generator needs to be researched.

The Fourier series [21], sampling theory [22], and double-integral Fourier analysis [23] are general methods for PWM switched waveform analysis. Among these methods, the double-integral Fourier is accurate and relatively simple for analyzing the PWM characteristics in the frequency domain by providing a strict mathematical method. Due to these advantages, the double Fourier approach is commonly used to obtain an exact analysis of harmonics components.

In this paper, Sinusoidal PWM (SPWM), Space Vector PWM (SVPWM), and Discontinuous PWM (DPWM) are considered as modulation schemes, and they are analyzed by the double-integral Fourier analysis method with consideration of the characteristics of the generator control system. Together with the above analysis, the optimal interleaving angle is determined for the PWM carrier waves. The DC-link current ripple is reduced in an N-paralleled converter system by conducting an interleaving scheme with the calculated optimal angle. The effectiveness of the proposed interleaving scheme is analyzed based on a 3-parallel-connected generator system with PMSGs.

This paper is organized as follows. Section II analyzes the current harmonics for each of the PWM switching schemes. Section III presents an interleaving scheme with the selection of the optimized angle. Section IV and V discuss simulation and experimental results to verify the performance of the proposed scheme. Section VI concludes the paper.

II. DC-LINK CURRENT HARMONICS ANALYSIS

This section briefly analyzes the current harmonics generated by the PWM switching of generator side converters. In order to analyze the current harmonics of each PWM scheme under the same conditions, the converter AC line currents are assumed to be purely sinusoidal for the harmonics analysis of the DC current waveform [17]. The double-integral Fourier series is employed in this paper to analyze the current harmonics. The analysis is mainly carried out for the system shown in Fig. 1, which consists of 3-parallel-connected generators with a common DC-link.

The DC-link current from generator side converter1 is expressed as:

$$i_{dcl}(t) = i_a(t)S_a(t) + i_b(t)S_b(t) + i_c(t)S_c(t) \quad (1)$$

where, the $i(t)$ is the phase current and $S(t)$ is the switching function for each of the phase legs. The switching function is expressed as:

$$S(t) = \begin{cases} 1, & \text{if top switch is turn-on} \\ 0, & \text{if bottom switch is turn-on} \end{cases} \quad (2)$$

For PWM switched waveforms, the most effective approach is the double-integral Fourier form, instead of the conventional integral form [23]. The double-integral Fourier is presented as:

$$\begin{aligned} C_{mn} &= A_{mn} + jB_{mn} \\ &= \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} F(x, y) e^{j(mx+ny)} dx dy \\ (x &= \omega_c t + \theta_c, y = \omega_o t + \theta_o) \end{aligned} \quad (3)$$

where A_{mn} and B_{mn} are amplitudes of the harmonics m (of the switching frequency) and n (of the modulating frequency). In addition, ω_c and θ_c are the angular frequency and initial phase of the carrier waveform, while ω_o and θ_o are the angular frequency and initial phase of the reference waveform, respectively. $F(x, y)$ is the switched waveform for one fundamental cycle. This equation separates the integration of the switched waveform across the whole fundamental period, so that the two parts can be separately evaluated to determine the harmonics co-efficient.

The switching function for a complete time varying switched waveform can be defined in the sinusoidal harmonics form as:

$$\begin{aligned} S(t) &= \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos(ny) + B_{0n} \sin(ny)] \\ &\quad + \sum_{m=1}^{\infty} [A_{m0} \cos(mx) + B_{m0} \sin(mx)] \\ &\quad + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [A_{mn} \cos(mx + ny) + B_{mn} \sin(mx + ny)] \quad (4) \end{aligned}$$

A time varying switched waveform can be represented by a summation of the DC component and the fundamental harmonics of the reference waveform, the carrier harmonics

of the carrier waveforms, and the sideband harmonics of both the reference and carrier waveforms as shown in the above equation.

The DC-link current generated by generator side converter1 can be redefined in the frequency domain as:

$$i_{dc1}(m,n) = i_a(m,n) \otimes S_a(m,n) + i_b(m,n) \otimes S_b(m,n) + i_c(m,n) \otimes S_c(m,n) \quad (5)$$

where, $i_a(m,n)$, $i_b(m,n)$, and $i_c(m,n)$ are Fourier transforms of the phase currents, $S_a(m,n)$, $S_b(m,n)$, and $S_c(m,n)$ are Fourier transforms of the switching functions, and \otimes is the convolution operator.

The DC-link current in the Fourier transform can be obtained from Eq. (4) and the three-phase currents. Consequently, the DC-link current in the time domain can be obtained by an inverse Fourier transform of Eq. (5).

A number of papers [17], [26] have introduced methods to calculate the current harmonics in i_{dc} . In particular, the power factor is one of the most important values in terms of the harmonics components distribution. However, the power factor in a generator system is almost equal to 1. Consequently, this paper does not consider the power factor.

A. Current Harmonics Analysis for SPWM

The switching function is determined by the PWM scheme. When the generator side converter conducts the SPWM switching, the DC-link current can be expressed as Eq. (6) when neglecting the phase current harmonics, by using the double-integral Fourier series analysis.

$$i_{dc1}(t) = A_{00} + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [A_{mn} \cos(mx + ny) + B_{mn} \sin(mx + ny)] \quad (6)$$

The double-integral Fourier coefficients in Eq. (6) of the DC-link current are defined as Eqns. (7)-(9).

$$A_{00} = \frac{3M}{4} I_{peak} \cos \varphi \quad (7)$$

$$A_{mn} = \frac{I_{peak}}{m\pi} \cos\left([m+n]\frac{\pi}{2}\right) [1 + 2\cos(n\frac{2\pi}{3})] \cos \varphi \times [J_{n+1}(m\frac{\pi}{2}M) - J_{n-1}(m\frac{\pi}{2}M)] \quad (8)$$

$$B_{mn} = \frac{I_{peak}}{m\pi} \cos\left([m+n]\frac{\pi}{2}\right) [1 + 2\cos(n\frac{2\pi}{3})] \sin \varphi \times [J_{n+1}(m\frac{\pi}{2}M) + J_{n-1}(m\frac{\pi}{2}M)] \quad (9)$$

where, M is the modulation index ($0 < M < 1$), I_{peak} is the peak value of the phase current, φ is the displacement angle, and $J_n(x)$ is the n -th Bessel function [23]-[25].

The displacement angle φ is considered to be 0 in the generator system since the power factor is almost 1. The DC-link current Eq. (6) can be expressed as follows [17]:

$$i_{dc1} = \frac{3M}{4} I_{peak} + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} A_{mn} \cos(mx + ny) \quad (10)$$

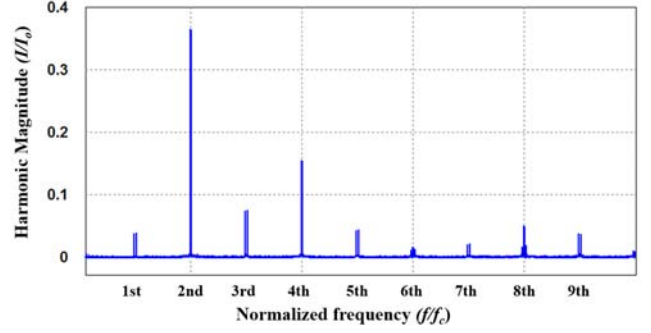


Fig. 2. DC-link current harmonics (SPWM).

$$A_{mn} = \frac{I_{peak}}{m\pi} \cos\left([m+n]\frac{\pi}{2}\right) [1 + 2\cos(n\frac{2\pi}{3})] \times [J_{n+1}(m\frac{\pi}{2}M) - J_{n-1}(m\frac{\pi}{2}M)] \quad (11)$$

From Eqns. (10) and (11), the possible dominant harmonics component is assumed to exist among the pairs of (m, n) as $(1, -3)$, $(1, 3)$, and $(2, 0)$.

By substituting Eqns. (10) and (11) into the pairs of (m, n) , the amplitudes of the possible dominant ac-harmonics component for the DC-link current are calculated as Eqns. (12) and (13), respectively.

$$|i_{dc1}(1,3)| = |i_{dc1}(1,-3)| = \frac{3I_{peak}}{\pi} \left| J_4\left(\frac{\pi}{2}M\right) - J_2\left(\frac{\pi}{2}M\right) \right| \quad (12)$$

$$|i_{dc1}(2,0)| = \frac{3I_{peak}}{2\pi} |J_1(\pi M)|. \quad (13)$$

In Eq. (12), since the values of J_4 and J_2 are similar, the amplitudes of $i_{dc1}(1, 3)$ and $i_{dc1}(1, -3)$ are very small. Consequently, the dominant harmonics component is $i_{dc1}(2, 0)$, which is the second-order switching harmonics component.

Fig. 2 shows the normalized DC-link current harmonics by using a Fast Fourier Transform (FFT) of the PSIM simulation, with the x-axis being the order of the switching frequency and the y-axis being the magnitude of the harmonic. Where f_c is the frequency of the carrier waveform and I_o is peak value of the phase current. The figure also shows that the dominant current harmonics component is located in the second-order switching frequency.

B. Current Harmonics Analysis for SVPWM

In order to analyze a complex PWM scheme, the numerical integral is conducted in this section. The DC-link current can be represented as a piecewise function. The SVPWM scheme has six sectors during a fundamental cycle. The double integral Fourier analysis can be applied to the DC-link current in each of the sectors. Table I shows the integral limits of the six sectors. These integral limits can be applied to Eq. (3) for the analysis of the current harmonics. For example, the double-integral Fourier analysis applied to the DC-link current in sector I is indicated as:

TABLE I
DOUBLE-FOURIER INTEGRAL LIMITS FOR SVPWM

y	Rising edge of x	Falling edge of x
$0 < y < \frac{\pi}{3}$	$-\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]$	$\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]$
$\frac{\pi}{3} < y < \frac{2\pi}{3}$	$-\frac{\pi}{2}[1 + \frac{3M}{2}\cos y]$	$\frac{\pi}{2}[1 + \frac{3M}{2}\cos y]$
$\frac{2\pi}{3} < y < \pi$	$-\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})]$	$\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})]$
$\pi < y < \frac{4\pi}{3}$	$-\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]$	$\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]$
$\frac{4\pi}{3} < y < \frac{5\pi}{3}$	$-\frac{\pi}{2}[1 + \frac{3M}{2}\cos y]$	$\frac{\pi}{2}[1 + \frac{3M}{2}\cos y]$
$\frac{5\pi}{3} < y < 2\pi$	$-\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})]$	$\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})]$

TABLE II
DOUBLE-FOURIER INTEGRAL LIMITS FOR DPWM

y	Rising edge of x	Falling edge of x
$-\frac{\pi}{6} < y < \frac{\pi}{6}$	$-\pi$	π
$\frac{\pi}{6} < y < \frac{\pi}{2}$	$-\pi \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})$	$\pi \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})$
$\frac{\pi}{2} < y < \frac{5\pi}{6}$	$-\pi[1 + \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})]$	$\pi[1 + \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})]$
$\frac{5\pi}{6} < y < \frac{7\pi}{6}$	0	0
$\frac{7\pi}{6} < y < \frac{3\pi}{2}$	$-\pi[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]$	$\pi[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]$
$\frac{3\pi}{2} < y < \frac{11\pi}{6}$	$-\pi \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})$	$\pi \frac{\sqrt{3}M}{2}\cos(y + \frac{\pi}{6})$

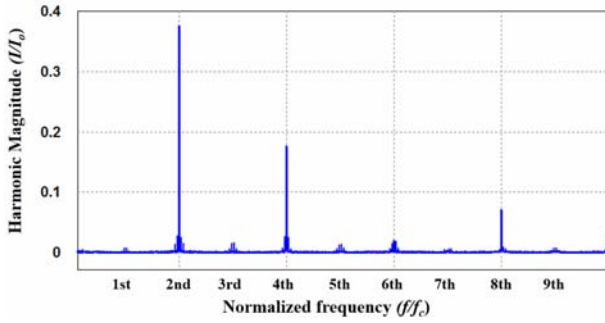


Fig. 3. DC-link current harmonics (SVPWM).

$$C_{mn1} = \frac{1}{2\pi^2} \int_0^{\frac{\pi}{3}} \int_{-\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]}^{\frac{\pi}{2}[1 + \frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})]} i_{dc1} e^{j(mx+ny)} dx dy \quad (14)$$

The double-integral Fourier analysis in a fundamental cycle can be achieved by adding all of the results of each sector as:

$$C_{mn} = \sum_{i=1}^6 C_{mni} \quad (15)$$

According to the results of the analysis for the SVPWM, the dominant current harmonics component is located at the second-order switching frequency. Simulation results for the DC-link current harmonics on the frequency domain have been obtained, as shown in Fig. 3. In this figure, the dominant current harmonics component is the second-order switching frequency, which is the same as the results with the numerical analysis.

C. Current Harmonics Analysis for DPWM

DPWM schemes are an effective modulation technique that can be employed to reduce switching losses. Three

different types of DPWM can be identified in the literature: 120° DPWM, 60° DPWM, and 30° DPWM. A 60° DPWM can reduce the switching frequency by retaining the switch state as turn ON or turn OFF during a 60° period when the magnitude of the phase voltage is largest. This paper uses the 60° DPWM scheme. Table II shows the double-Fourier integral limits for the 60° DPWM scheme. Because of the discontinuous period, the integral limits of the rising edge and falling edge maintain constant values during a 60° period. When the generator side converter conducts the DPWM scheme, the DC-link current harmonics can be numerically analyzed in a way that is similar to that of the SVPWM by using Table II.

The example of the numerical analysis for DPWM can be expressed as:

$$C_{mn1} = \frac{1}{2\pi^2} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \int_{-\pi}^{\pi} i_{dc1} e^{j(mx+ny)} dx dy \quad (16)$$

The dominant current harmonics component for the DPWM scheme is variable, and it depends on the modulation index. Based on a numerical analysis, the first-order switching frequency possesses dominant current harmonics components for most cases. Fig. 4 shows simulation results of the DC-link current harmonics for the DPWM scheme. This figure shows that the dominant current harmonics component is the first-order switching frequency. Because the dominant current harmonics component in the DPWM is different from that for both the SPWM and the SVPWM, the proposed optimal interleaving angle for the system is changed.

III. PROPOSED INTERLEAVING SCHEME FOR DC-LINK CURRENT RIPPLE REDUCTION

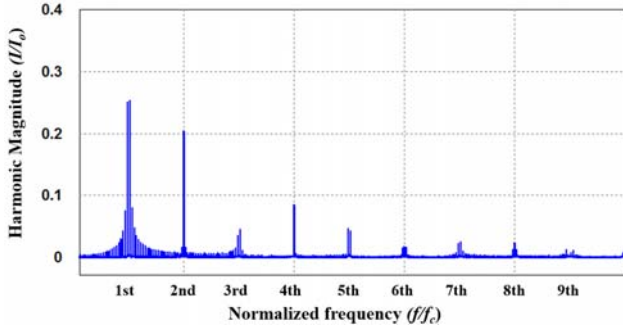


Fig. 4. DC-link current harmonics (DPWM).

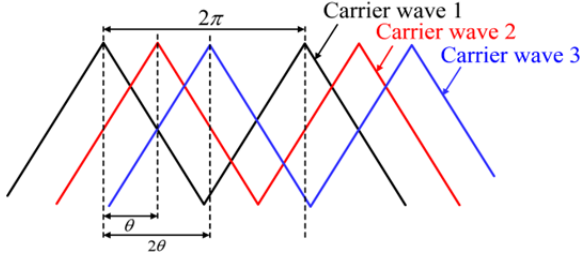


Fig. 5. Definition of the interleaving angle.

The use of an interleaving scheme for parallel systems can decrease the current ripple flowing through the DC-link capacitor. The interleaving (i.e. phase-shifting) PWM switching cycle of individual generator side converters at an optimal angle can reduce the total current ripple due to PWM switching at the ac terminal. This section proposes an optimal interleaving angle for parallel-connected generator systems based on a DC-link current harmonics analysis. Fig. 5 shows the definition of the interleaving angle θ ($0 < \theta < 2\pi$). Since

the interleaving scheme shifts the phase angle of the carrier wave form, the angle of the carrier wave for each of the converters can be expressed as:

$$\theta_{c2} = \theta_{c1} + \theta \quad (17)$$

$$\theta_{c3} = \theta_{c1} + 2\theta \quad (18)$$

Considering the even distribution of the output currents from each of the converters, the DC-link current harmonics from each of the converters with the interleaving scheme can be defined as:

$$i_{dc3_h}(m,n) = i_{dc2_h}(m,n)e^{jm\theta} = i_{dc1_h}(m,n)e^{jm2\theta} \quad (19)$$

The current i_{dc} flowing through the capacitor can be expressed as a summation of the DC-link current from each of the converters, as shown in Eq. (20).

$$i_{dc} = i_{dc1} + i_{dc2} + i_{dc3} \quad (20)$$

From Eqns. (19) and (20), the amplitude of the total DC-link current ripple from the generator side converters with the interleaving scheme can be represented as:

$$\begin{aligned} |i_{dc_h}| &= |i_{dc1_h}(m,n) + i_{dc2_h}(m,n) + i_{dc3_h}(m,n)| \\ &= |i_{dc1_h}(m,n)(1 + e^{jm\theta} + e^{jm2\theta})| \\ &= |i_{dc1_h}(m,n)| |1 + e^{jm\theta} + e^{jm2\theta}| \end{aligned} \quad (21)$$

Eq. (21) shows that making the $|1 + e^{jm\theta} + 2e^{jm2\theta}|$ term equal to 0 can eliminate specific DC-link current harmonics. This term can be determined by the interleaving angle θ . In this paper, the optimal interleaving angle is defined as an angle that can eliminate the dominant DC-link current harmonics. As mentioned earlier, since the dominant current harmonics component is located at a different frequency, the optimal interleaving angle is also different depending on the PWM scheme. The optimal angle can be normalized, as shown in Eq. (22):

$$\begin{aligned} |(1 + e^{jm\theta} + e^{jm2\theta})| &= \sqrt{(1 + \cos m\theta + \cos 2m\theta)^2 + (\sin m\theta + \sin 2m\theta)^2} \\ &= \sqrt{3 + 2(\cos m\theta + \cos 2m\theta)} \\ &= \sqrt{3 + 2(\cos^2 m\theta + 2\cos m\theta - 1)} \end{aligned} \quad (22)$$

As a result, the selected DC-link current harmonics component can be cancelled with $\cos m\theta = -1/2$, which can be obtained by shifting the carrier waveform by about θ ($=2\pi/3m$). Based on the analysis in section II, the optimal interleaving angle for SPWM and SVPWM is $\pi/3$, since the dominant current harmonics component with these PWM schemes is located in the second-order switching frequency ($m=2$). Similarly, the interleaving angle for the DPWM scheme, which usually has the dominant current harmonics component in the first-order switching frequency ($m=1$) is $2\pi/3$ according to Eq. (22). This method to decrease the current ripple can be applied to an N-parallel system in a similar way.

The DC-link current ripple is expressed with an RMS value that can be calculated as [27]:

$$\text{RMS } i_{dc} = \sqrt{\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} i_{dc}^2(m,n)} \quad (23)$$

Fig. 6 shows the actualization process of the interleaving scheme of 3-parallel-connected generator systems with a decreased DC-link current ripple. First, the parallel-connected PMSGs are controlled with the reference q -axis current to generate power. Furthermore, the grid side converter controls the voltage of the DC-link with a constant value for the power factor control of the system.

The current controller creates the references of the modulation voltage signal. Then they are used to control the generator side converter switching, using the considered PWM schemes (SPWM, SVPWM, and DPWM). The carrier waves used in the PWM schemes are determined by the proposed interleaving scheme. Thus, this simple method achieves a reduced current ripple in the DC-link for a parallel system.

IV. SIMULATION RESULTS

Simulations are performed using the PSIM software tool to demonstrate the validity of the proposed method. Table III

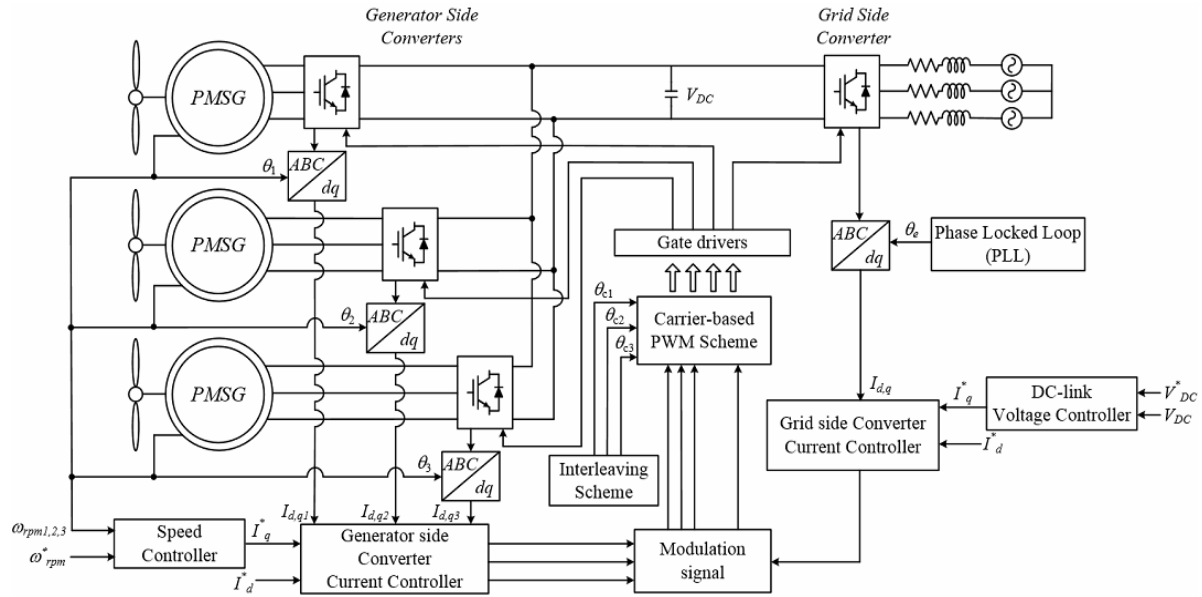


Fig. 6. Block diagram of the 3-parallel generator system control using the proposed scheme.

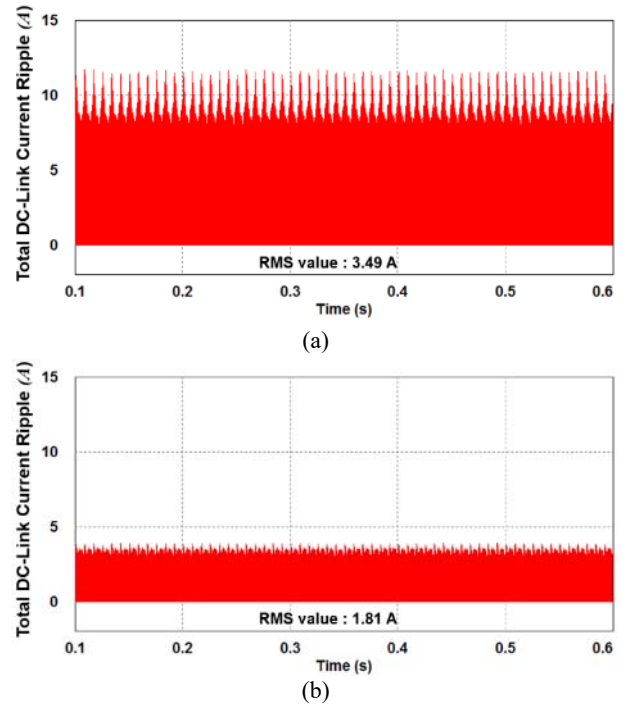
TABLE III GENERATOR SPECIFICATIONS	
R_s	0.158 Ω
L_d	1.55 mH
L_q	1.76 mH
P (Pole)	8
Rated power	5.5 kW
Rated speed	1750 rpm
Rated torque	2.02 N·m
Rated current	13.5 A _{rms}

shows the PMSG specification and parameters.

The sampling time for the system control is 100 μ s, and the switching frequency of the converter is set to 10 kHz in accordance with the experimental setting. The q -axis currents of the PMSGs are controlled to 3 A with constant speed loads, which are controlled to 750 rpm, to generate power.

To focus on the effectiveness of the interleaving scheme on parallel-connected generators, the grid side converter is replaced by 300 V which is a voltage source with parallel connected 10 Ω as a load.

Fig. 7 shows simulated waveforms of the DC-link current for the SPWM both with and without the interleaving scheme. The results show that the interleaving scheme with an optimal angle reduces the RMS value of the DC-link current ripple from 3.49 A to 1.81 A. Table IV summarizes the simulation results for the interleaving scheme with various angles. The RMS value of the DC-link current ripple decreases dramatically with an optimal angle for the SPWM, $\pi/3$. Thus, the proposed scheme is affordable for the SPWM. In addition, Table V and Table VI show simulation results of the interleaving scheme for

Fig. 7. DC-link current ripple waveforms with SPWM: (a) without an interleaving scheme and (b) with $\pi/3$ interleaving.

various angles with the SVPWM and DPWM schemes. For the SVPWM, the RMS value of the DC-link current ripple is the most effective when the $\pi/3$ interleaving scheme is applied for a 3-parallel system because the dominant current harmonics component is located in the second-order switching frequency. For the DPWM, the $2\pi/3$ interleaving scheme effectively reduces the RMS value of the DC-link current ripple. This means that the proposed interleaving control is also effective with the DPWM switching scheme.

TABLE IV
CURRENT RIPPLE RESULTS ON THE DC-SIDE FOR SPWM

Interleaving Angle	DC-link Current Ripple
0	3.49 A
$\pi / 3$	1.81 A
$\pi / 2$	2.51 A
$2\pi / 3$	2.03 A

TABLE V
CURRENT RIPPLE RESULTS ON THE DC-SIDE FOR SVPWM

Interleaving Angle	DC-link Current Ripple
0	3.57 A
$\pi / 3$	1.78 A
$\pi / 2$	2.60 A
$2\pi / 3$	2.03 A

TABLE VI
CURRENT RIPPLE RESULTS ON THE DC-SIDE FOR DPWM

Interleaving Angle	DC-link Current Ripple
0	3.56 A
$\pi / 3$	2.14 A
$\pi / 2$	2.06 A
$2\pi / 3$	1.89 A

V. EXPERIMENTAL RESULTS

Fig. 8 shows the experimental setup of the generators. The overall experimental setup comprises control boards, power boards, and PMSGs. The generator side inverters are controlled under the current control mode by employing a digital signal processor (DSP) TMS320F28335. 7.5kW induction motors with a rated speed of 1,750 rpm are used as load motors for this experiment. The PMSG speed information was attained using a rotary incremental encoder. The experimental parameters and operating conditions are the same as those of the PSIM simulations.

Fig. 9 shows experimental waveforms that verify the effectiveness of the proposed interleaving scheme for a parallel-connected generator system with SPWM. Since the interleaving scheme only controls the total DC-link current by delaying the carrier waves of each generator side converter, the amplitude and RMS value of the DC-link current from each of the converters (i_{dc1} , i_{dc2} , i_{dc3}) are the same, even when the interleaving scheme is applied. However, applying the interleaving scheme can decrease the total DC-link current ripple (i_{dc}). Fig. 9(a) shows that the RMS value before applying the interleaving scheme is 3.76 A. Fig. 9(b) confirms that applying the proposed interleaving scheme with an optimal angle of $\pi/3$ reduces the RMS value of the current ripple to 1.92 A. In addition, Fig. 10 shows the

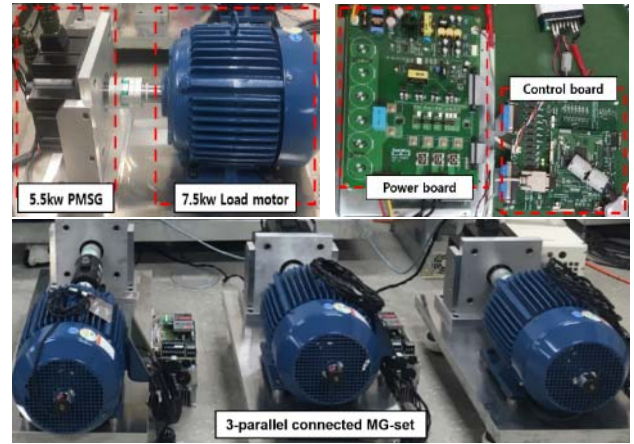
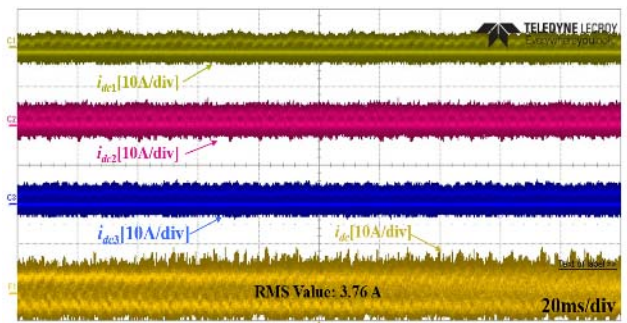
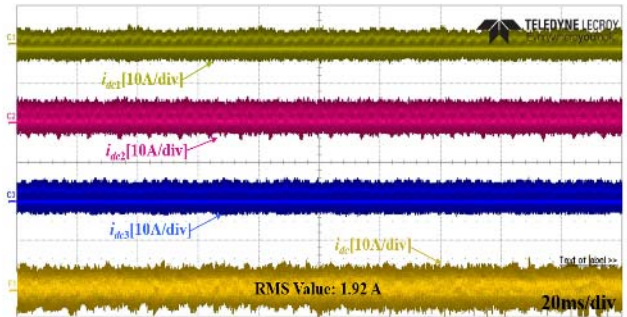


Fig. 8. Hardware setup for the experiment.



(a)



(b)

Fig. 9. DC-link current ripple waveforms with SPWM: (a) without an interleaving scheme and (b) with $\pi / 3$ interleaving.

effectiveness of the harmonics components with FFT waveforms by applying the interleaving method with SPWM. Fig. 10(a) shows that the harmonics in the second-order switching frequency is dominant. Fig. 10(b) shows that the dominant harmonics component is decreased by applying the proposed method.

Fig. 11 shows DC-link current ripple waveforms and FFT of the current ripple when the SVPWM scheme is used. Fig. 11(a) shows that the dominant harmonic components of the DC-link current is located in the second-order switching frequency and that the RMS value of the DC-link current ripple is 3.98 A without the interleaving scheme. Fig. 11(b) shows that the dominant harmonic is cancelled and that the

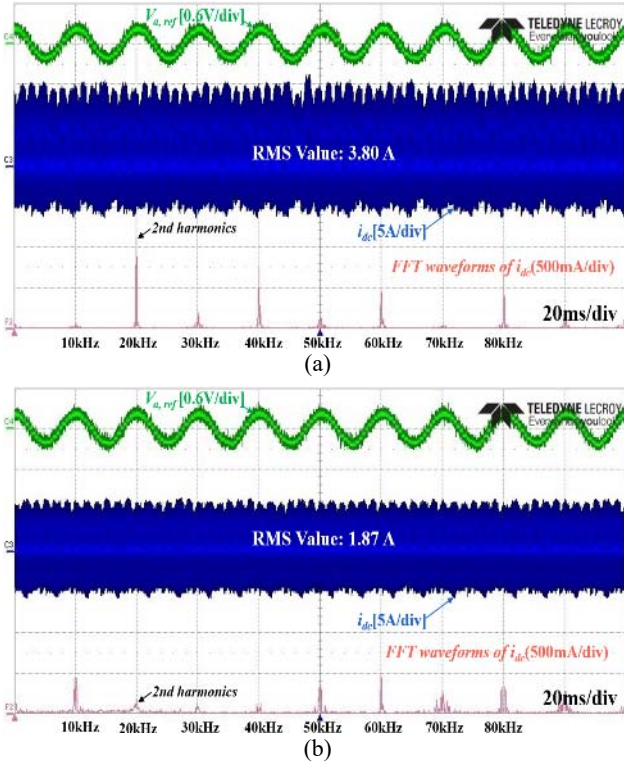


Fig. 10. DC-link current harmonics waveforms with SPWM: (a) without interleaving scheme and (b) with $\pi/3$ interleaving.

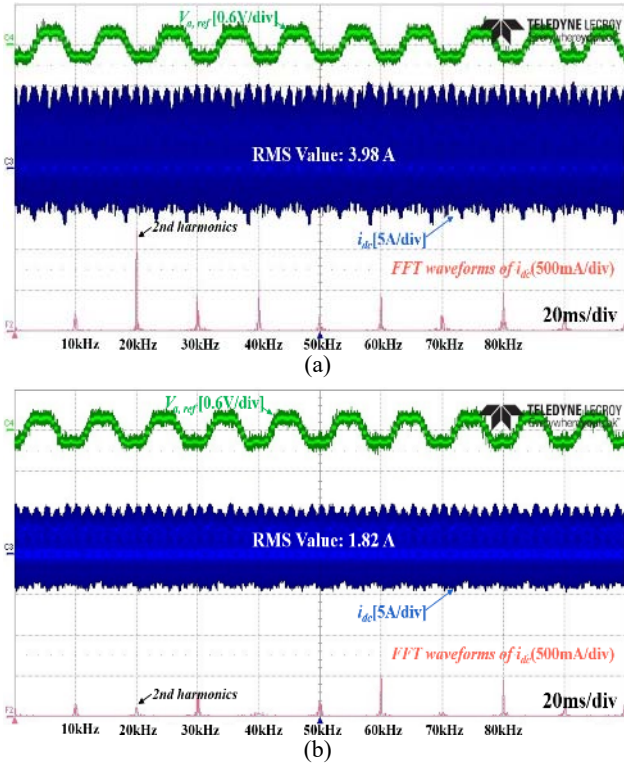


Fig. 11. DC-link current harmonics waveforms with SVPWM: (a) without interleaving scheme and (b) with $\pi/3$ interleaving.

RMS value is reduced to 1.82 A by using the simple interleaving scheme with an optimal angle.

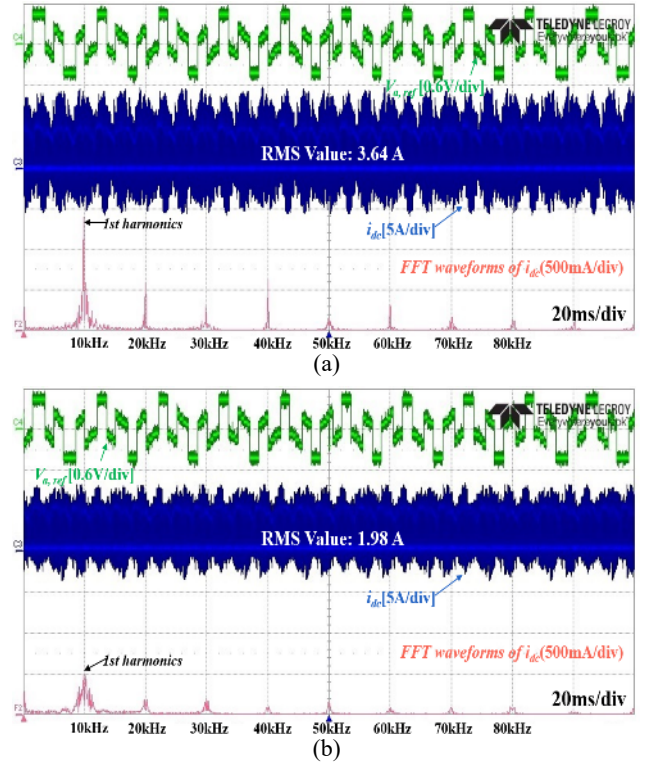


Fig. 12. DC-link current harmonics waveforms with DPWM: (a) without interleaving scheme and (b) with $2\pi/3$ interleaving.

Fig. 12 shows the effectiveness of the proposed interleaving scheme for DPWM. As shown in Fig. 12(a), the dominant current harmonic component is located in the first-order switching frequency. Based on the analysis of DPWM, the optimal interleaving angle for DC-link current ripple reduction is determined to be $2\pi/3$. Finally, the DC-link current ripple is decreased from 3.64 A to 1.98 A by cancelling the first-order switching frequency, as shown in Fig. 12(b).

A comparison of the simulation results in section IV with the experimental results in this section shows similarities in terms of effectiveness. Applying the selected optimal interleaving angle to cancel the dominant harmonics components reduces the DC-link current ripple.

VI. CONCLUSIONS

This paper presents an interleaving scheme for DC-link current ripple reduction in N-parallel connected generator systems. The proposed method analyzes the current harmonics components generated through the generator side converters using the double-integral Fourier method for various PWM switching schemes. Then it selects an optimized interleaving angle based on this analysis, in order to reduce the current ripple in the DC-link. Both simulation and experimental results demonstrate the validity of the interleaving scheme with 3-parallel 5.5 kW PMSGs. A comparison with the traditional method confirms the validity of the proposed method.

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