

# Design and Control of DC/AC Converters in Parallel with Diode Rectifiers for Regenerative Applications

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## Abstract

This paper introduces a DC/AC converter, which can be connected in parallel with a diode rectifier for regenerative applications. The DC/AC converter is supposed to transmit regenerative energy to the power grid when a motor is braking. Isolation transformers are not needed in the topology, which can reduce the size and cost. An analysis of the zero-order current existing in the system is carried out. In addition, algorithms to minimize the zero-order current, control the power factor and keep the DC bus voltage stable are discussed. A 55kW industrial prototype is built to verify the proposed analysis and control strategies.

**Key words:** Bi-directional, DC/AC converters, PWM, Regenerative energy, Zero-order current

NOMENCLATURES			
$K_1 \sim K_6$	Six IGBTs in the proposed converter	$T_{a-up}$	Time span when $K_1$ is on in case I <sup>(1P)</sup>
$D_1 \sim D_6$	Six diodes in the diode rectifier	$T_{a2}$	Time span when $K_1$ is on in case I <sup>(1N)</sup>
$v_a, v_b, v_c$	Three-phase voltages of the power grid	$T_{b2}$	Time span when $K_3$ is on in case I <sup>(1N)</sup>
$i_a, i_b, i_c$	Three-phase currents to the power grid	$T_{c2}$	Time span when $K_6$ is on in case I <sup>(1N)</sup>
$i_z$	Zero-order current of the converter	$K_p$	Gain of the current regulator
$L$	Inductance of the three-phase inductors	$I_{cmd}$	Output of the DC bus voltage regulator
$f_s$	Switching frequency of the IGBT	$t_1 \sim t_6$	Used to divide each $T_s$ into several stages
$T_s$	Sample period of the control system		
$V_{dc}$	DC bus voltage		
$V_p$	Amplitude of the phase voltage		
$\omega$	Angular frequency of the grid voltage		
$v_{D1} \sim v_{D6}$	Diode voltages in the diode rectifier		
$v_{a-r}, v_{b-r}, v_{c-r}$	Three-phase reference voltages		
$G_1 \sim G_8$	Derivatives of the zero-order current		
$T_{stage-1} \sim T_{stage-7}$	Time spans for all of the stages		
$g_{a-up}, g_{a-down}$	Gate signals of $K_1$ and $K_2$		
$g_{b-up}, g_{b-down}$	Gate signals of $K_3$ and $K_4$		
$g_{c-up}, g_{c-down}$	Gate signals of $K_5$ and $K_6$		
$v_{a-inv}, v_{b-inv}, v_{c-inv}$	Equivalent three-phase output voltages		
$T_{b-down}$	Time span when $K_4$ is on in case I <sup>(1P)</sup>		
$T_{c-down}$	Time span when $K_6$ is on in case I <sup>(1P)</sup>		

## I. INTRODUCTION

Regenerative braking is widely utilized in industrial applications such as electric and hybrid vehicles [1]-[3]. Many applications such as subways, tractions, and elevators can benefit from regenerative braking and a lot of power energy can be saved. Typically, the regenerative energy raises the DC bus voltage if diode-rectifiers are used, as shown in Fig. 1. As a result, the braking energy is usually dissipated by the shunt resistors or stored in super-capacitors and batteries. In order to reduce the cost of the device, shunt resistors are usually used to consume the regenerative energy. The authors of [4]-[6] introduced applications where super capacitors are used to store the energy for motor drives. However, the disadvantages are: (1) the capacity of the storage system is limited; (2) the price of super-capacitors is high; (3) a super-capacitor management system is required since the rating voltage of a super-capacitor cell is relatively low; (4) the volume of super-capacitors is large.

Regenerative energy can also be transmitted to the power

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grid by DC/AC converters to improve the system efficiency. An active rectifier, usually referred to as a PWM rectifier [7]-[10], is a solution for regenerative applications since the power can flow bi-directionally between the AC side and the DC side [11]-[13]. However, there are some disadvantages in the following occasions.

- 1) When the regenerative power is much smaller than the rating power of the motor (for example, if the regenerative power is 10kW and the motor's power is 30kW, a 30kW PWM rectifier is needed), it is necessary to install a full-power PWM rectifier, which is wasteful.
- 2) There are a lot of inverters with diode rectifiers, and replacing diode rectifiers with PWM rectifiers is not practical due to limitations on the volume, the product warrant law, etc.

This paper focuses on the topology shown in Fig. 2, where a DC/AC converter is connected in parallel with an inverter. When regenerative energy is produced, the DC/AC converter can transmit energy to the power grid. No shunt resistors or batteries are necessary.

The proposed DC/AC converter can also be used in industrial applications where several inverters are connected in parallel to absorb regenerative power, as shown in Fig. 3. In that case one DC/AC converter, instead of a lot of PWM rectifiers, is needed to transmit regenerative energy to the power grid when necessary.

There have been many discussions on how to control the three-phase currents flowing to the power grid for a DC/AC converter [14]-[17]. The strategies include d-q transformation methods [18]-[21], hysteresis control methods [22]-[25], model predictive control [26] - [29] and others.

Unlike conventional PWM rectifiers, there are several potential current paths in Fig. 2 and Fig. 3, where the DC buses are directly connected in parallel, leading to the balance of the DC bus voltages. As depicted in Fig. 2, the diode, the IGBT and the inductor form a current path between two power grid lines. The current  $i_b$  (when  $v_a > v_b$ ) can be calculated as Equ. (1). Thus, traditional control strategies are not suitable for the topology proposed in this paper because of the diode rectifiers.

Fig. 4 shows simulation results with the conventional d-q transformation control method. The simulation results shown in Fig. 4 are obtained with the parameters shown in Table I. Result #1 concerns the conventional PWM rectifier (Note that there is no diode-rectifier in this case) and it verifies the control strategy since the three-phase currents are sinusoidal and the zero-order current is 0. The control method does not work well for the proposed converter in this paper, as shown in result #2. The amplitude of the zero-order current is over 50A, as shown in result #3. The zero-order current is defined as the sum of the three-phase currents, and it brings the following disadvantages [30]-[32]:

- High currents flow through the diode rectifier, which can

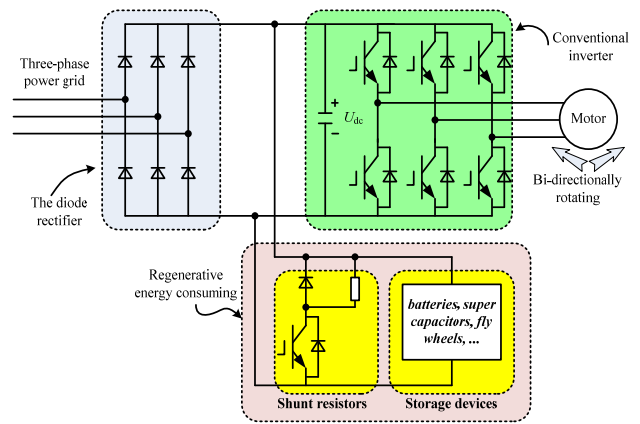


Fig. 1. Topology of traditional inverters with regenerative energy consumption capability.

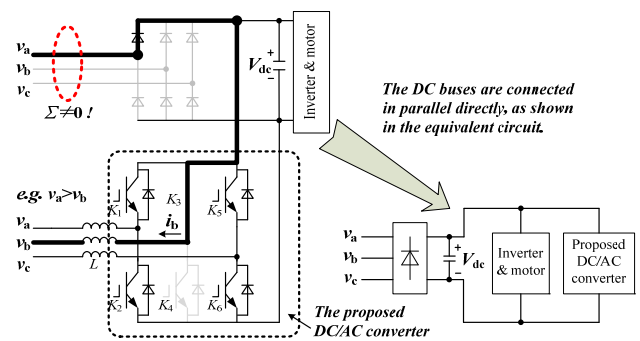


Fig. 2. Proposed converter and its equivalent circuit.

TABLE I  
PARAMETER SETTINGS IN THE SIMULATION

Items	Values
$L$	0.8mH
$v_a \sim v_c$	380V(line-line, RMS), 50Hz
$f_s$	8kHz
$T_s$	0.000125s
$V_{dc}$	700V

increase the power loss (The diode rectifier is not supposed to work when the DC bus voltage is raised by regenerative energy).

- The protection system of the power grid may cut off the power supply because of the zero-order current.
- The equipment on the power grid can be affected by the zero-order current and cannot work as normal.

$$L \frac{di_b}{dt} = v_a - v_b \quad (1)$$

Experimental waveforms, shown in Fig. 5, are obtained when the proposed DC/AC converter works with the diode rectifier and the traditional control algorithm is adopted. The rating power of the converter and the diode rectifier are both 55kW. In addition, the grid voltage is 380V/50Hz. Waveforms of the currents are similar to those of the simulation results.

This paper presents the design and control of a DC/AC

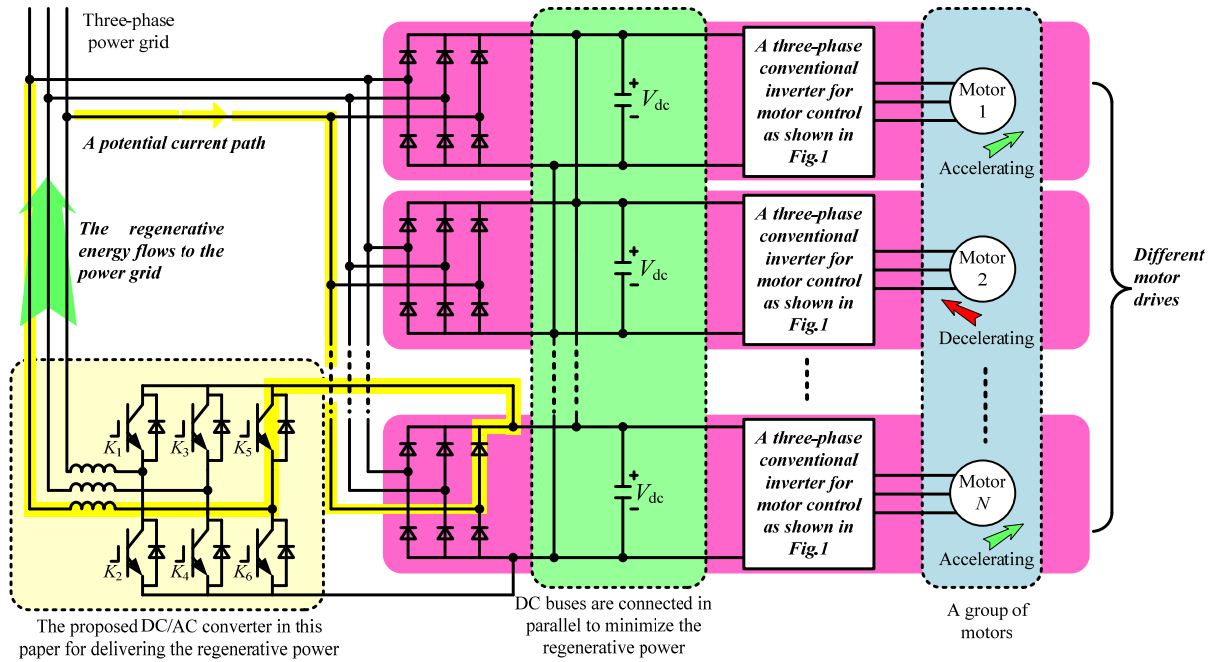


Fig. 3. Topology of multiple inverters with the proposed DC/AC converter for regenerative energy delivery.

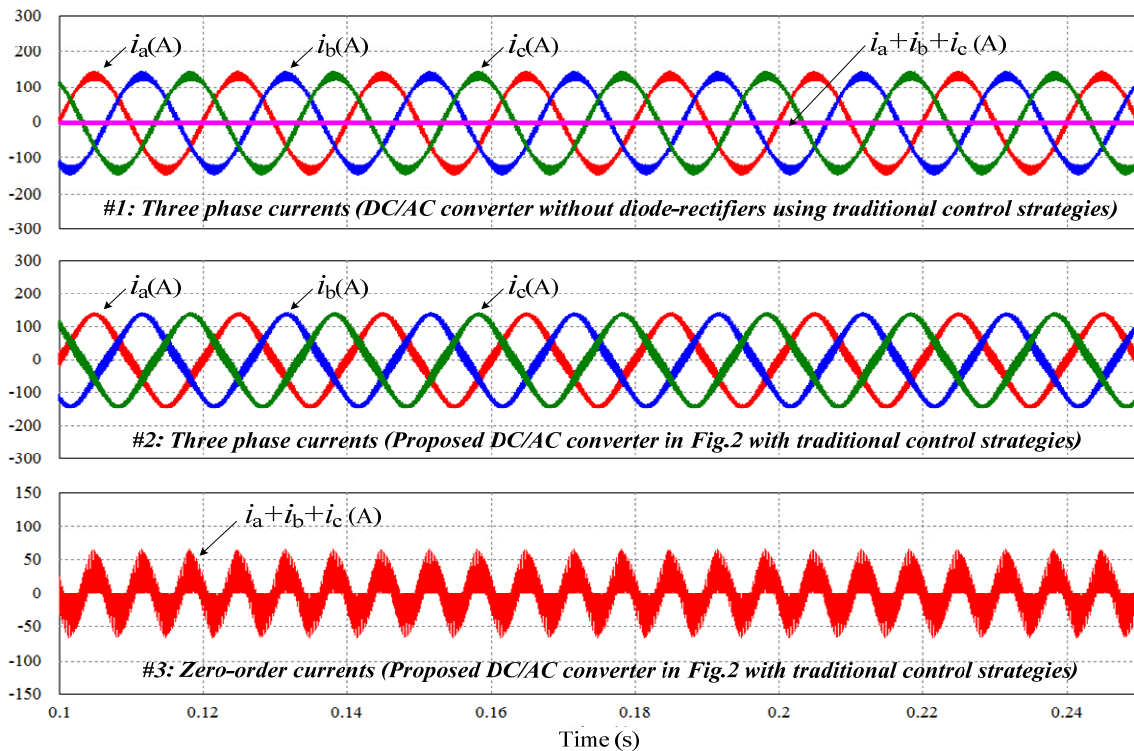


Fig. 4. Simulation results of the DC/AC converter with conventional control algorithms.

converter which is connected in parallel with diode rectifiers for regenerative occasions.

The proposed converter and control algorithm can meet the requirements in regenerative occasions and make it possible to re-use the braking energy. They can also work together with traditional inverters which lack bi-directional power flowing capability. This paper describes the models of the

converter, and an analysis of the zero-order current is done. An industrial prototype is built and experimental results are used to validate the proposed design and algorithm.

## II. MODELLING OF THE PROPOSED CONVERTER

### A. The model of the Zero-Order Current

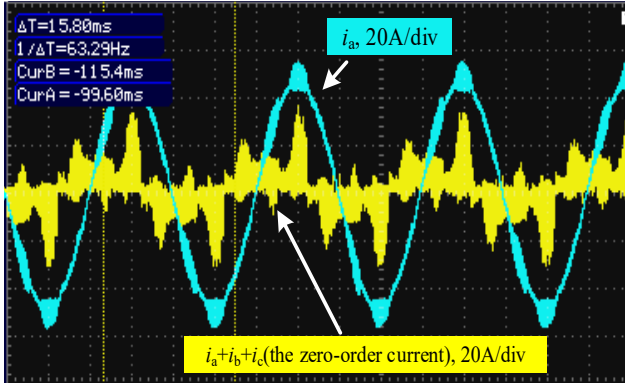


Fig. 5. Phase current and zero-order current obtained in industrial applications with conventional control algorithms.

TABLE II  
THE SIX CASES IN ONE CYCLE ( $\pi/2, 5\pi/2$ ]

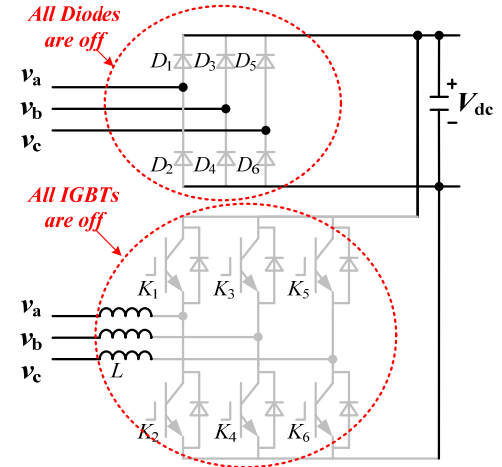
Cases	$\omega t$	Features
I	$(\frac{\pi}{2}, \frac{5\pi}{6}]$	$v_a > v_b \geq v_c$
II	$(\frac{5\pi}{6}, \frac{7\pi}{6}]$	$v_b > v_a \geq v_c$
III	$(\frac{7\pi}{6}, \frac{3\pi}{2}]$	$v_b > v_c \geq v_a$
IV	$(\frac{3\pi}{2}, \frac{11\pi}{6}]$	$v_c > v_b \geq v_a$
V	$(\frac{11\pi}{6}, \frac{13\pi}{6}]$	$v_c > v_a \geq v_b$
VI	$(\frac{13\pi}{6}, \frac{5\pi}{2}]$	$v_a > v_c \geq v_b$

Three-phase power grid voltages are sinusoidal and the phase voltages can be defined as Equ. (2), where  $t$  denotes the time. Since the voltages are periodic, each cycle can be divided into 6 cases, as shown in Table II.

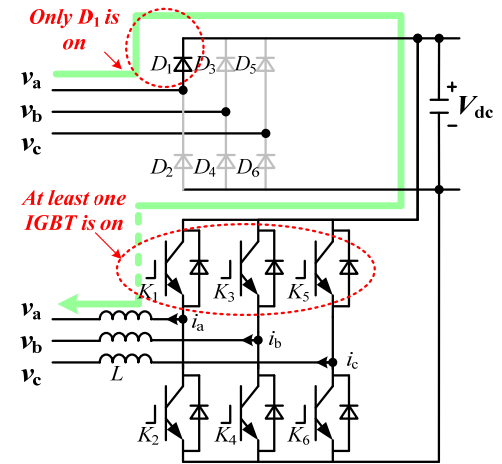
$$\begin{cases} v_a = V_p \sin(\omega t) \\ v_b = V_p \sin(\omega t - \frac{2\pi}{3}) \\ v_c = V_p \sin(\omega t + \frac{2\pi}{3}) \end{cases} \quad (2)$$

There are three modes for the proposed converter in case I. (1) In Fig. 6(a), all of the IGBTs are off and there are no currents on the inductors. In addition, the diodes are all off. As a result, this mode is referred to as “All Turned Off (ATO) mode.” (2) In Fig. 6(b),  $D_1$  is on and one or more of the upper IGBTs is on. This mode is referred to as “Positive Zero-order Current (PZC) mode.” (3) In Fig. 6(c),  $D_6$  is on and at least one of the lower IGBTs is on. This mode is referred to as “Negative Zero-order Current (NZC) mode.”

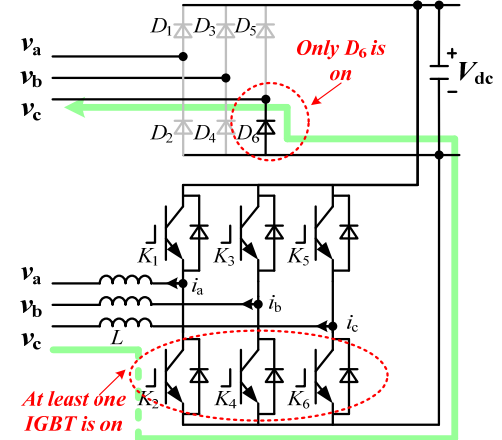
In Fig. 6(b), the diode  $D_1$  is on. Based on KVL, the diode voltages can be calculated as:



(a) all turned off mode (ATO), when  $v_a > v_b > v_c$ .



(b) Positive Zero-order Current (PZC) mode, when  $v_a > v_b > v_c$ .



(c) Negative Zero-order Current (NZC) mode, when  $v_a > v_b > v_c$ .  
Fig. 6. Topological modes for case I when  $V_{dc}$  is high enough for regeneration.

$$\begin{cases} v_{D1} + v_{D2} = -V_{dc} \\ v_{D1} - v_{D3} = v_a - v_b > 0 \\ v_{D1} - v_{D5} = v_a - v_c > 0 \\ v_{D1} + v_{D4} + V_{dc} = v_a - v_b > 0 \\ v_{D1} + v_{D6} + V_{dc} = v_a - v_c > 0 \end{cases} \quad (3)$$

$D_1$  is on. Therefore,  $v_{D1}=0$ . In addition,  $V_{dc}$  is high enough for regeneration. Hence  $V_{dc} > (v_a-v_b)$  and  $V_{dc} > (v_a-v_c)$ . The equations can be solved and the result is shown in Equ. (4).

As a result, the other diodes  $D_2 \sim D_6$  are all off in Fig. 6(b). In the same manner, it can be verified that  $D_1 \sim D_5$  are all off when  $D_6$  is on in NZC mode, as shown in Fig. 6(c).

According to the PWM strategy, the duty ratio of each IGBT is updated in every sample period. In addition, the typical gate signals can be drawn as Fig.7.  $g_x$  is introduced to represent the gate signals.  $g_x \in \{g_{a-up}, g_{a-down}, g_{b-up}, g_{b-down}, g_{c-up}, g_{c-down}\}$ .  $g_x=1$  means that the switch is on, while  $g_x=0$  means that the switch is off.

$$\begin{cases} v_{D2} = -V_{dc} < 0 \\ v_{D3} = v_b - v_a < 0 \\ v_{D5} + v_c - v_a < 0 \\ v_{D4} = (v_a - v_b) - V_{dc} < 0 \\ v_{D6} = (v_a - v_c) - V_{dc} < 0 \end{cases} \quad (4)$$

### B. Analysis of the Working Stages in Case I

The principle law of traditional PWM rectifiers shows that the phase of the reference voltage is ahead of the power grid voltage by a small angle [9]. Hence in Fig.7,  $v_{a-r} \approx v_a$ ,  $v_{b-r} \approx v_b$  and  $v_{c-r} \approx v_c$ , which can be used to simplify the analysis. Fig.8 shows the gate signals in the first sample period for PZC mode, and the working scheme of the converter can be described as:

**Stage 1**  $[0, t_1]$  [See Fig. 9(a) and Fig. 10(a)]:  $K_1$ ,  $K_3$  and  $K_5$  are off.  $i_z$  can be written as:

$$i_z = i_a + i_b + i_c \quad (5)$$

For the three-phase power grid:

$$v_a + v_b + v_c = 0 \quad (6)$$

Equ.(7) shows the calculation of the derived numbers in different stages.

$$G_1 \sim G_8 = \frac{di_z}{dt} = \frac{di_a}{dt} + \frac{di_b}{dt} + \frac{di_c}{dt} \Rightarrow \begin{cases} G_1 = \frac{3v_a - 3V_{dc}}{L} \\ G_2 = \frac{3v_c}{L} \\ G_3 = \frac{3v_a - 2V_{dc}}{L} \\ G_4 = \frac{3v_c + V_{dc}}{L} \\ G_5 = \frac{3v_a - V_{dc}}{L} \\ G_6 = \frac{3v_c + 2V_{dc}}{L} \\ G_7 = \frac{3v_a}{L} \\ G_8 = \frac{3v_c + 3V_{dc}}{L} \end{cases} \quad (7)$$

a) PZC mode in stage 1: If  $i_z > 0$ , the converter works in PZC

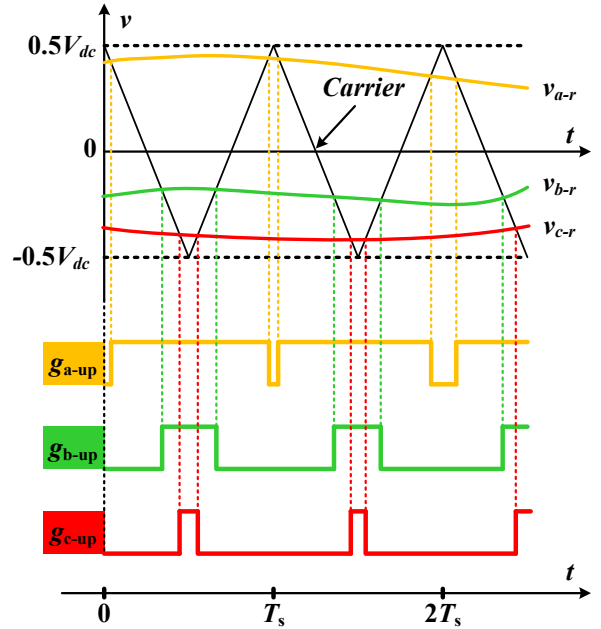


Fig. 7. PWM strategy in all of the sample periods.

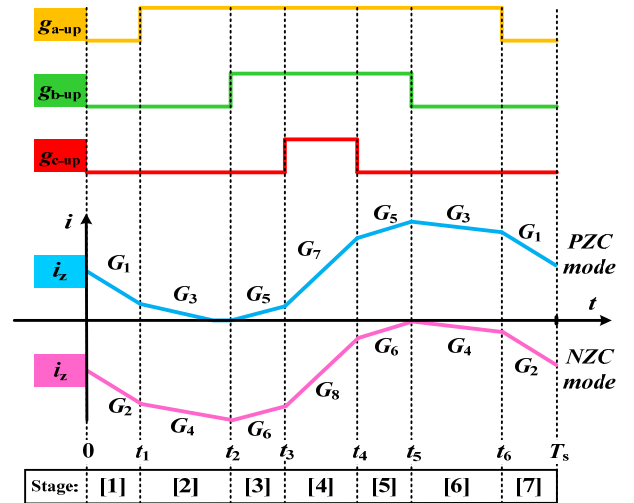


Fig. 8. Zero-order current in one sample period.

mode. The equivalent circuit is shown in Fig. 9(a). The curve of  $G_1$  is shown in Fig. 8.  $i_z$  decreases since  $G_1 < 0$ .

b) NZC mode in stage 1: If  $i_z < 0$ , the converter works in NZC mode. The equivalent circuit is shown in Fig. 10(a). The curve of  $i_z$  is shown in Fig. 8.  $i_z$  decreases since  $v_c < 0$ .

c) Hybrid mode in stage 1:  $i_z$  can fall and may be negative in stage 1. In addition, the slope of the curve above zero is  $G_1$ , while it is  $G_2$  below zero.

Then there are three types of curves, as shown in Fig.11. The curves of  $G_1$  and  $G_2$  with different values of  $V_{dc}$  are shown in Fig. 12(a) and Fig. 12(b).

**Stage 2**  $[t_1, t_2]$  [See Fig. 9(b) and Fig. 10(b)]:  $K_1$  is on.  $K_3$  and  $K_5$  are off.

a) PZC mode in stage 2

If  $i_z > 0$ , the equivalent circuit is shown in Fig. 9(b). In

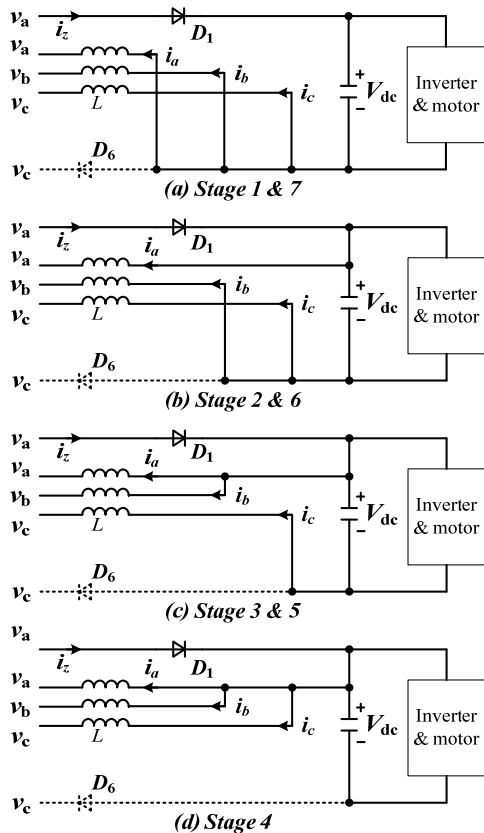


Fig. 9. Equivalent circuits in PZC mode.

addition, it can be determined that  $G_3$  is negative. As a result,  $i_z$  decreases in this stage. The curve of  $G_3$  is shown in Fig. 12(c).

b) NZC mode in stage 2

If  $i_z < 0$ , the equivalent circuit is shown in Fig. 10(b). The curve of  $G_4$  is shown in Fig. 12(d).  $G_4$  is bipolar.

c) Hybrid mode in stage 2

There are four possibilities. (1) If  $i_z > 0$ ,  $i_z$  decreases and when it reaches zero,  $D_1$  is off. Then if  $G_4 < 0$ ,  $D_6$  conducts and  $i_z$  decreases. (2) If  $i_z > 0$ ,  $i_z$  decreases and when it reaches zero,  $D_1$  is off. Then if  $G_4 \geq 0$ ,  $D_6$  is off and  $i_z = 0$ . (3) If  $i_z < 0$ ,  $i_z$  decreases if  $G_4 < 0$ . (4) If  $i_z < 0$ ,  $i_z$  increases if  $G_4 \geq 0$ . When it reaches zero,  $D_6$  is off.  $D_1$  is also off since  $G_3 < 0$ .

Fig. 11(b) shows the four types of curves in stage 2.

**Stage 3 [ $t_2, t_3$ ] [See Fig. 9(c) and Fig. 10(c)]:**  $K_1$  and  $K_3$  are on.  $K_5$  is off.

a) PZC mode in stage 3

When  $i_z > 0$ , the converter works in PZC mode, and the equivalent circuit is shown in Fig. 9(c).  $G_5$  is bipolar, as shown in Fig. 12(e).

b) NZC mode in stage 3

If  $i_z < 0$ , the equivalent circuit is shown in Fig. 10(c).  $G_6$  is positive, as shown in Fig. 12(f).

c) Hybrid mode in stage 3

As shown in Fig. 11(c), there are four possibilities in the hybrid mode of this stage. (1) If  $i_z > 0$ ,  $i_z$  increases when

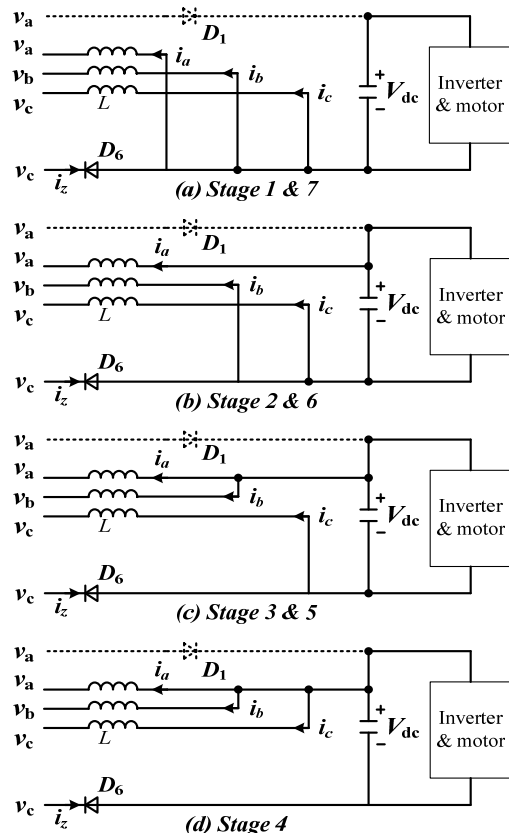


Fig. 10. Equivalent circuits in NZC mode.

$G_3 \geq 0$ . (2) If  $i_z > 0$ ,  $i_z$  decreases when  $G_5 < 0$ . After it reaches zero,  $D_1$  and  $D_6$  are both off. (3) If  $i_z < 0$ ,  $i_z$  increases since  $G_6 > 0$ . After it reaches zero,  $D_6$  is off. Then  $D_1$  is off if  $G_5 < 0$ . (4) If  $i_z < 0$ ,  $i_z$  increases since  $G_6 > 0$ . After it reaches zero,  $D_6$  is off. Then  $D_1$  is on if  $G_5 \geq 0$ .

**Stage 4 [ $t_3, t_4$ ] [See Fig. 9(d) and Fig. 10(d)]:**  $K_1, K_3$  and  $K_5$  are on.

a) PZC mode in stage 4

$G_7$  is positive since  $v_a > 0$ .  $i_z$  increases. The curve of  $G_7$  is shown in Fig. 12(g).

b) NZC mode in stage 4

$G_8$  is positive, as shown in Fig.12(h).

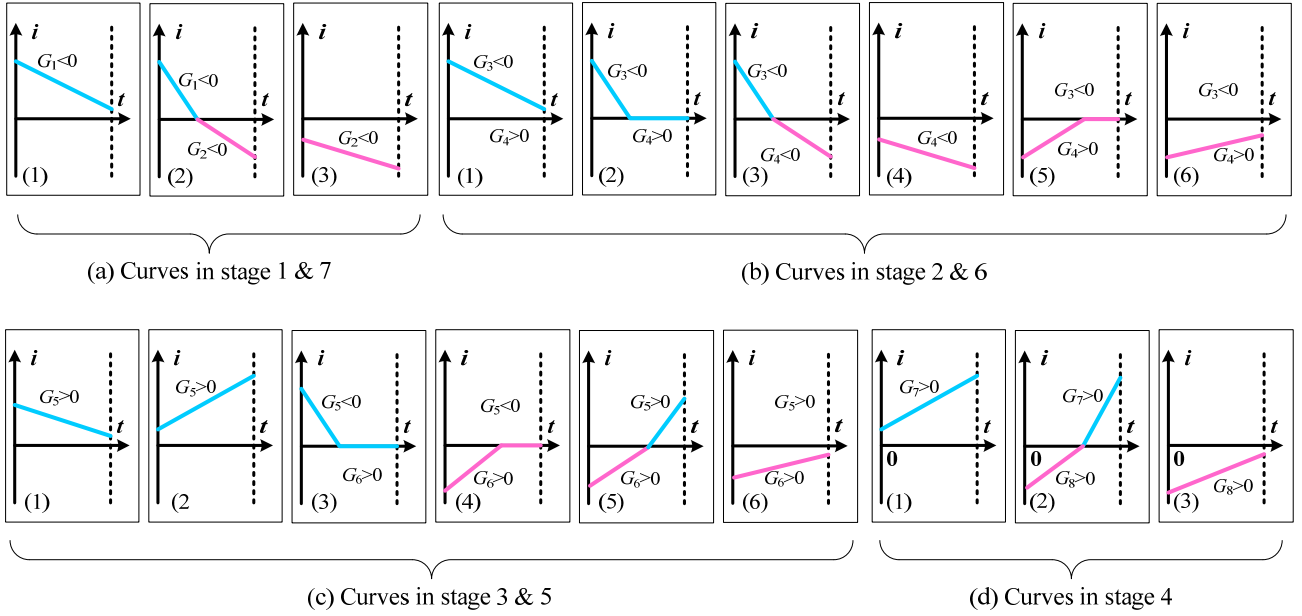
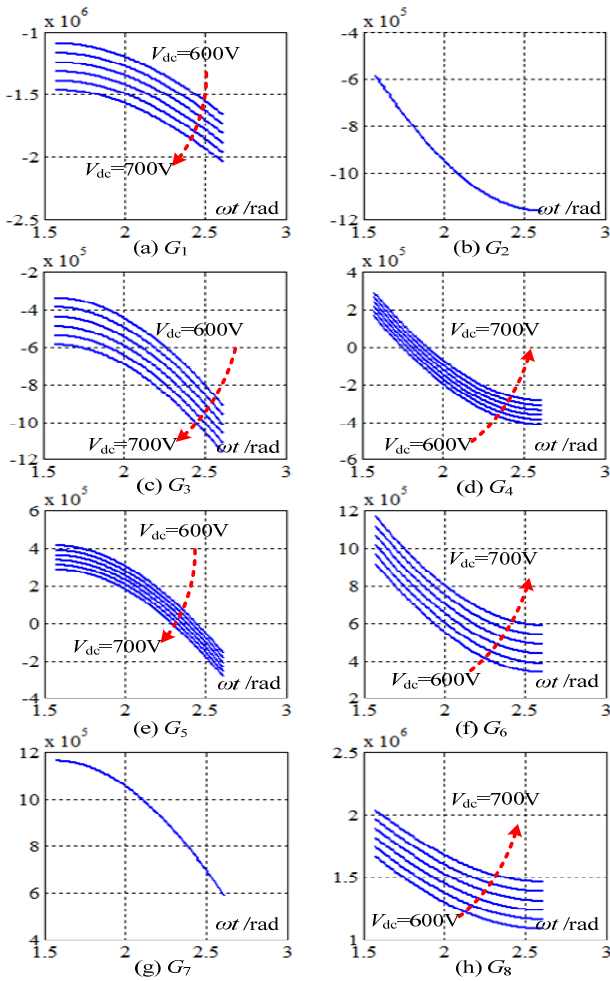
c) Hybrid mode in stage 4

$i_z$  can increase and become positive. The slope of the curve above zero is  $G_7$ , while it is  $G_8$  below zero. The curves of  $i_z$  in this stage are shown in Fig.11(d).

The equivalent circuits of stage 5 [ $t_4, t_5$ ], stage 6 [ $t_5, t_6$ ] and stage 7 [ $t_6, T_s$ ] are shown in Fig.9 and Fig.10. They are similar to stage 3, stage 2 and stage 1, respectively.

C. Characteristics of  $i_z$  in case I

In each sample period,  $v_a \sim v_c, v_{a-r} \sim v_{c-r}$  and  $V_{dc}$  can be considered constant. In Fig.8,  $K_1$  is on between  $t_1$  and  $t_6$ ,  $K_3$  is on between  $t_2$  and  $t_5$ ,  $K_5$  is on between  $t_3$  and  $t_4$ . In addition, the gate signals are center-aligned in every sample period. Hence:


 Fig. 11. Curves of  $i_z$  in each stage.

 Fig. 12. Curves of  $G_1 \sim G_8$  in case I.

$$\begin{cases} t_6 - t_1 = \frac{T_s}{2} + \frac{v_a - r}{V_{dc}} T_s \approx \frac{T_s}{2} + \frac{v_a}{V_{dc}} T_s \\ t_5 - t_2 = \frac{T_s}{2} + \frac{v_b - r}{V_{dc}} T_s \approx \frac{T_s}{2} + \frac{v_b}{V_{dc}} T_s \\ t_4 - t_3 = \frac{T_s}{2} + \frac{v_c - r}{V_{dc}} T_s \approx \frac{T_s}{2} + \frac{v_c}{V_{dc}} T_s \end{cases} \quad (8)$$

The time spans for all of the stages can be calculated as:

$$\begin{cases} T_{stage-1} = T_{stage-7} = \frac{V_{dc} - 2v_a}{4V_{dc}} T_s \\ T_{stage-2} = T_{stage-6} = \frac{v_a - v_b}{2V_{dc}} T_s \\ T_{stage-3} = T_{stage-5} = \frac{v_b - v_c}{2V_{dc}} T_s \\ T_{stage-4} = \frac{V_{dc} + 2v_c}{2V_{dc}} T_s \end{cases} \quad (9)$$

$$\begin{aligned} \Delta i_z &= G_1 T_{stage-1} + G_5 T_{stage-3} + G_7 T_{stage-4} + G_5 T_{stage-5} + G_3 T_{stage-6} + G_1 T_{stage-7} \\ &= \frac{T_s}{4L} \frac{(6V_{dc}^2 - 18V_{dc}V_p \sin(\alpha) - 2\sqrt{3}V_{dc}V_p \cos(\alpha))}{V_{dc}} \\ &\quad - \frac{T_s}{4L} \frac{(9V_p^2 \sin^2(\alpha) + 3\sqrt{3}V_p^2 \sin(\alpha)\cos(\alpha))}{V_{dc}} > 0 \end{aligned} \quad (10)$$

$$\begin{aligned} \Delta i_z^+ &= G_1 T_{stage-1} + G_3 T_{stage-2} + G_5 T_{stage-3} + G_7 T_{stage-4} \\ &\quad + G_5 T_{stage-5} + G_3 T_{stage-6} + G_1 T_{stage-7} \\ &= \frac{30T_s (31 \sin(\alpha) - 32)}{L} < 0 \end{aligned} \quad (11)$$

Typically, when  $\omega t = \pi/2$  and stage 2 is not taken into consideration,  $i_z$  increases by  $\Delta i_z$ , which can be calculated by Equ. (10). In addition, when stage 2 is taken into consideration,  $i_z$  increases by  $\Delta i_z^+$ , which is calculated by



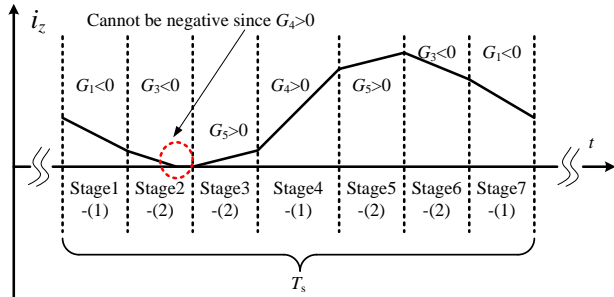


Fig. 13. Waveform of  $i_z$  when  $\omega t = \pi/2$  in case I (in theory).

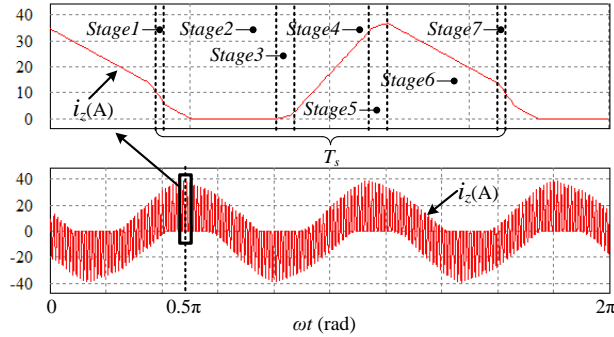


Fig. 14. Waveform of  $i_z$  when  $\omega t = \pi/2$  in case I (simulation).

Equ. (11). Since  $\Delta i_z > 0$ ,  $\Delta i_z^+ < 0$ ,  $G_4 < 0$  and  $G_5 > 0$ ,  $i_z$  falls to zero in stage 2, as shown in Fig. 13.

Fig. 14 shows the simulation result of  $i_z$ , which coincides with Fig. 13. In other cases, a similar model can be established. The conclusions are:

- (1) In every sample period,  $i_z$  is determined by the derivatives  $G_1 \sim G_8$ .
- (2) If  $D_1$  is on,  $i_z$  is positive. If  $D_6$  is on,  $i_z$  is negative.
- (3)  $i_z$  is a combination of several curves, as shown in Fig. 14.
- (4) Conventional control algorithms are not suitable for the proposed converter.

### III. PROPOSED CONTROL STRATEGY

#### A. Division of a Case

Take case I as an example, it can be divided into two parts, which are referred to as case I<sup>(IP)</sup> and case I<sup>(IN)</sup>. In case I<sup>(IP)</sup>, there is only one positive voltage ( $v_a$ ). Meanwhile, in case I<sup>(IN)</sup>, there is only one negative voltage ( $v_c$ ). Fig. 15 shows the two sub cases.

#### B. Strategy in Case I<sup>(IP)</sup>

In case I<sup>(IP)</sup>, the converter works in PZC mode. It can be determined that  $i_z$  increases if  $K_3$  or  $K_5$  is on. As a result,  $K_3$  and  $K_5$  should be off during this period. In addition,  $K_2$  should be off, otherwise  $D_6$  conducts. The equivalent circuit can be redrawn as Fig. 16(a). The gate signal of  $K_1$  is set as:

$$g_{a-up} = g_{b-down} \cup g_{c-down} \quad (12)$$

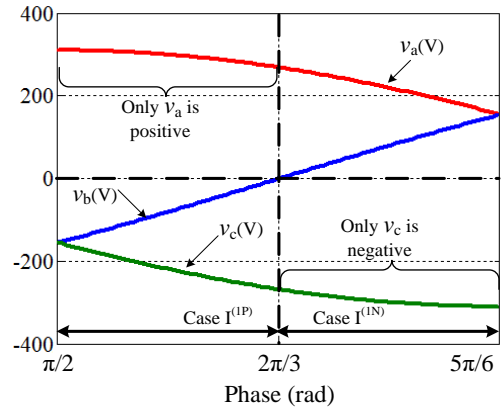
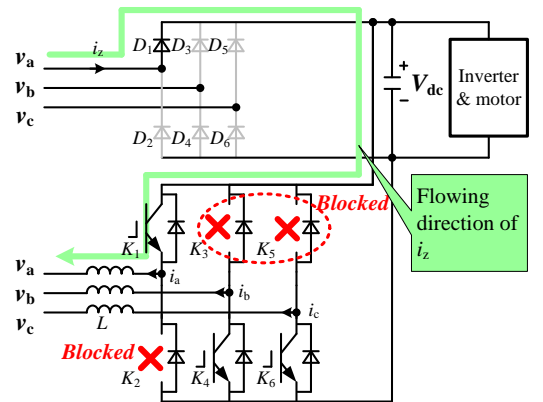
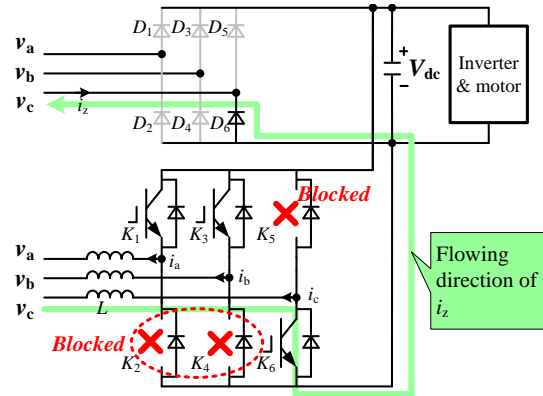


Fig. 15. Two sub cases in case I.



(a)  $K_3$ ,  $K_5$  and  $K_2$  are off in PZC mode, when in case I<sup>(IP)</sup>.



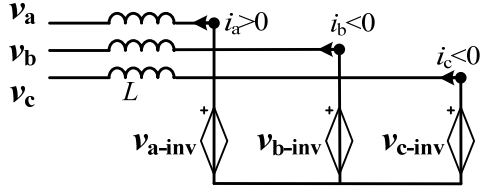
(b)  $K_5$ ,  $K_2$  and  $K_4$  are off in NZC mode, when in case I<sup>(IN)</sup>.

Fig. 16. Equivalent circuits with the proposed strategy.

From Equ. (12), it can be seen that when  $g_{a-up} = 0$ , all of the switches are off. The converter turns to be a traditional diode rectifier. The absolute values of  $i_a$ ,  $i_b$  and  $i_c$  are getting smaller until zero.

Otherwise, when  $g_{a-up} = 1$  it can be seen that  $i_b$  and  $i_c$  are controllable only if they are negative, as proved in the appendix. Luckily, it should be noticed that  $v_b$  and  $v_c$  are both negative in case I<sup>(IP)</sup>. In addition, the power factor is set as 1 in regenerative applications. Thus, the reference values of  $i_b$  and  $i_c$  are both negative in case I<sup>(IP)</sup>.




 Fig. 17. Model of the circuit in case I<sup>(1P)</sup>.

In one sample period, a model of the equivalent circuit is shown in Fig. 17. The output voltages can be:

$$\begin{cases} v_{a-inv} = \frac{T_{a-up} V_{dc}}{T_s} \\ v_{b-inv} = \frac{V_{dc}(T_s - T_{b-down}) + 0T_{b-down}}{T_s} = V_{dc} - \frac{T_{b-down} V_{dc}}{T_s} \\ v_{c-inv} = \frac{V_{dc}(T_s - T_{c-down}) + 0T_{c-down}}{T_s} = V_{dc} - \frac{T_{c-down} V_{dc}}{T_s} \end{cases} \quad (13)$$

Therefore,  $v_{a-inv}$  can be calculated as:

$$\begin{cases} v_{a-inv} = \frac{T_{b-down} V_{dc}}{T_s}, & \text{if } T_{b-down} \geq T_{c-down} \\ v_{a-inv} = \frac{T_{c-down} V_{dc}}{T_s}, & \text{if } T_{b-down} < T_{c-down} \end{cases} \quad (14)$$

In addition, the equations for the model in Fig.17 are:

$$\begin{cases} -v_{b-inv} + L \frac{di_b}{dt} + v_b = -v_{a-inv} + L \frac{di_a}{dt} + v_a \\ -v_{c-inv} + L \frac{di_c}{dt} + v_c = -v_{a-inv} + L \frac{di_a}{dt} + v_a \end{cases} \quad (15)$$

In the proposed strategy,  $i_z \approx 0$ . Therefore, Equ.(14) can be solved as:

$$\begin{cases} \frac{di_b}{dt} = \frac{v_{b-inv} - v_{a-inv} + v_a - v_b}{2L} - \frac{1}{2} \frac{di_c}{dt} \\ \frac{di_c}{dt} = \frac{v_{c-inv} - v_{a-inv} + v_a - v_c}{2L} - \frac{1}{2} \frac{di_b}{dt} \end{cases} \quad (16)$$

Equ. (15) can also be written as Equ. (16), which is useful for the design of the control algorithm.

$$\begin{cases} v_{b-inv} = 2L \frac{di_b}{dt} + v_b - v_a + v_{a-inv} + L \frac{di_c}{dt} \\ v_{c-inv} = 2L \frac{di_c}{dt} + v_c - v_a + v_{a-inv} + L \frac{di_b}{dt} \end{cases} \quad (17)$$

Thus, the control diagram can be designed as Fig. 18, where a compensation is added to improve the performance of the system. In this case, the output of the controller is assumed to be identical to  $2L di_b / dt$ . As a result, the simplified close-loop control diagram for  $i_b$  can be drawn as Fig. 19.  $I_b(s)$  is the current on phase b in the s-domain, and  $I_b(s)^*$  is the reference value for  $i_b$ .

A proportional regulator is adopted in this paper for the following reasons.

(1) With proportional regulators, the control diagram can be simplified to a typical I-type system, which is common and stable.

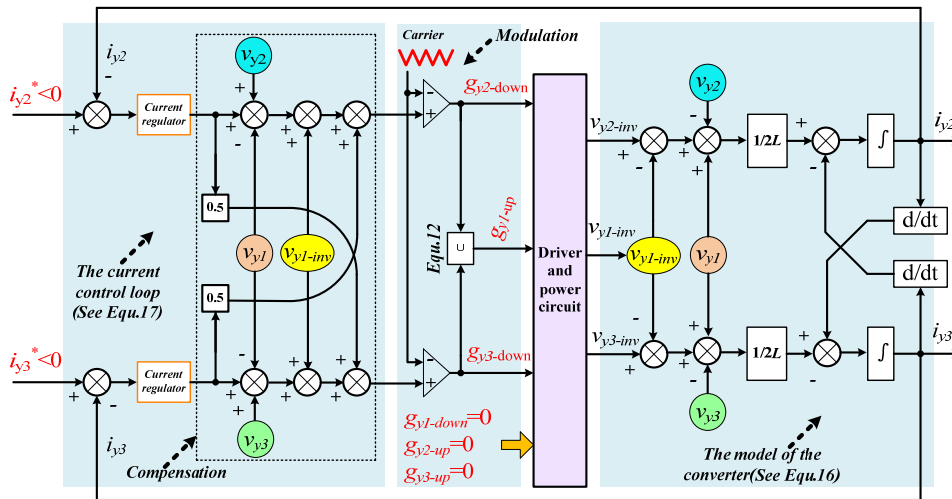
(2) In industrial applications, the proposed converter is used to keep the DC bus voltage constant while zero error tracking for the current loop is not mandatory.

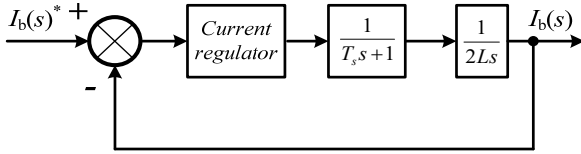
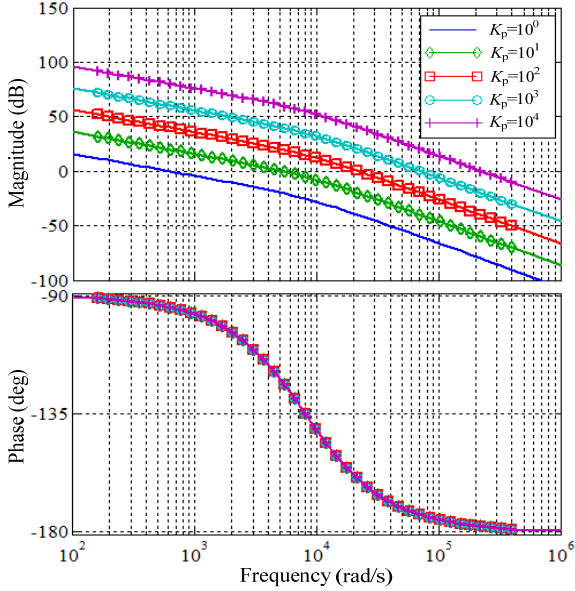
(3) There is no standard for the THD (total harmonic distortion) of currents. As a result, even a proportional regulator may induce certain ripples. However, this result is acceptable. Actually, a low THD can make the product more competitive. As a result, the output of the regulator should be constrained.

(4) Fast response speed is required to prevent the DC bus voltage from rising. In addition, proportional regulators are easy to tune for specific occasions.

Therefore, the open-loop transfer function is as Equ.(18). The values of  $T_s$  and  $L$  are shown in Table I.

$$G(s) = \frac{K_p}{2L} = \frac{625 K_p}{s(T_s s + 1)} = \frac{625 K_p}{s(0.000125 s + 1)} \quad (18)$$


 Fig. 18. Current-loop control diagram for case I<sup>(1P)</sup> ( $y1='a'$ ,  $y2='b'$  and  $y3='c'$ ).

Fig. 19. Control diagram of  $i_b$  in the s-domain.Fig. 20. Bode diagrams of the open-loop transfer function in case  $I^{(1P)}$ .

When  $K_p=10^0, 10^1, 10^2, 10^3,$  and  $10^4$ , the bode diagrams are shown in Fig. 20.  $y_1, y_2$  and  $y_3$  are introduced to represent the three phases (phase 'a', 'b' and 'c'). Thus,  $i_{y1}, i_{y2}$  and  $i_{y3}$  can be used to demonstrate the three-phase currents, which makes it simple to carry out the control diagram.

Fig. 20 shows that the system is stable even if  $K_p=10^4$ . In the experimental prototype,  $K_p$  is set as 15. Thus, the cut-off frequency  $\omega_c$  and the phase margin  $\gamma$  can be calculated as:

$$G(\omega j) = \frac{625K_p}{\omega j(0.000125\omega j + 1)} = \frac{625K_p}{-0.000125\omega^2 + \omega j} \quad (19)$$

$$\Rightarrow \begin{cases} \omega_c = 7028(\text{rad/s}) \\ \gamma = 180^\circ - 131.3^\circ = 48.7^\circ \end{cases}$$

Since the ripple of the current is usually a consideration, a limiter is often necessary.

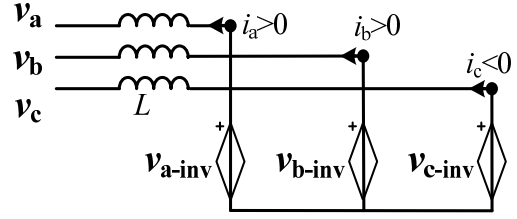
### C. Strategy in Case $I^{(1N)}$

In case  $I^{(1N)}$ , the converter works in NZC mode.  $K_2, K_4$  and  $K_5$  should be off to eliminate the zero-order current. The equivalent circuit is shown in Fig. 16(b). The gate signal of  $K_6$  is set as:

$$g_{c-down} = g_{a-up} \cup g_{b-up} \quad (20)$$

Hence, when  $g_{c-down}=0$ , all of the switches are off. The converter becomes a traditional diode rectifier, and the absolute values of  $i_a, i_b$  and  $i_c$  decrease.

In addition, when  $g_{c-down}=1$ ,  $i_b$  and  $i_c$  are controllable only

Fig. 21. Model of the circuit in case  $I^{(1N)}$ .

if they are positive, as proved in the appendix.  $v_b$  and  $v_c$  are both positive in case  $I^{(1N)}$ . In addition, the power factor is set as 1 in regenerative applications. Thus, the reference values of  $i_b$  and  $i_c$  are both positive in case  $I^{(1N)}$ .

In one sample period, the model of the equivalent circuit is shown in Fig. 21. The output voltages are:

$$\begin{cases} v_{a-inv} = \frac{T_{a2}V_{dc}}{T_s} \\ v_{b-inv} = \frac{T_{b2}V_{dc}}{T_s} \\ v_{c-inv} = \frac{V_{dc}(T_s - T_{c2}) + 0T_{c2}}{T_s} = V_{dc} - \frac{T_{c2}V_{dc}}{T_s} \end{cases} \quad (21)$$

Therefore,  $v_{c-inv}$  can be calculated as:

$$\begin{cases} v_{c-inv} = V_{dc} - \frac{T_{b2}V_{dc}}{T_s}, & \text{if } T_{b2} \geq T_{c2} \\ v_{c-inv} = V_{dc} - \frac{T_{c2}V_{dc}}{T_s}, & \text{if } T_{b2} < T_{c2} \end{cases} \quad (22)$$

The solutions are:

$$\begin{cases} \frac{di_b}{dt} = \frac{v_{b-inv} - v_{c-inv} + v_c - v_b}{2L} - \frac{1}{2} \frac{di_a}{dt} \\ \frac{di_a}{dt} = \frac{v_{a-inv} - v_{c-inv} + v_c - v_a}{2L} - \frac{1}{2} \frac{di_b}{dt} \end{cases} \quad (23)$$

In addition:

$$\begin{cases} v_{b-inv} = 2L \frac{di_b}{dt} + v_b - v_c + v_{c-inv} + L \frac{di_a}{dt} \\ v_{a-inv} = 2L \frac{di_a}{dt} + v_a - v_c + v_{c-inv} + L \frac{di_b}{dt} \end{cases} \quad (24)$$

The control diagram can be designed as Fig. 22. As a result, the control diagram can also be represented by Fig. 21.

### D. Control Strategy in all of the Sub Cases

Fig. 23 shows six cases in every cycle. It can be seen that each case can be divided into two sub cases. The control algorithm in case I can be modified to meet the requirements in the other cases.

Fig. 24 also shows a control strategy with DC bus voltage control. The converter only works when regeneration is necessary. When  $I_{cmd} > 0$ , the power flows from the DC bus to the power grid.  $i_a^*, i_b^*$  and  $i_c^*$  are the three-phase reference currents for the converter.

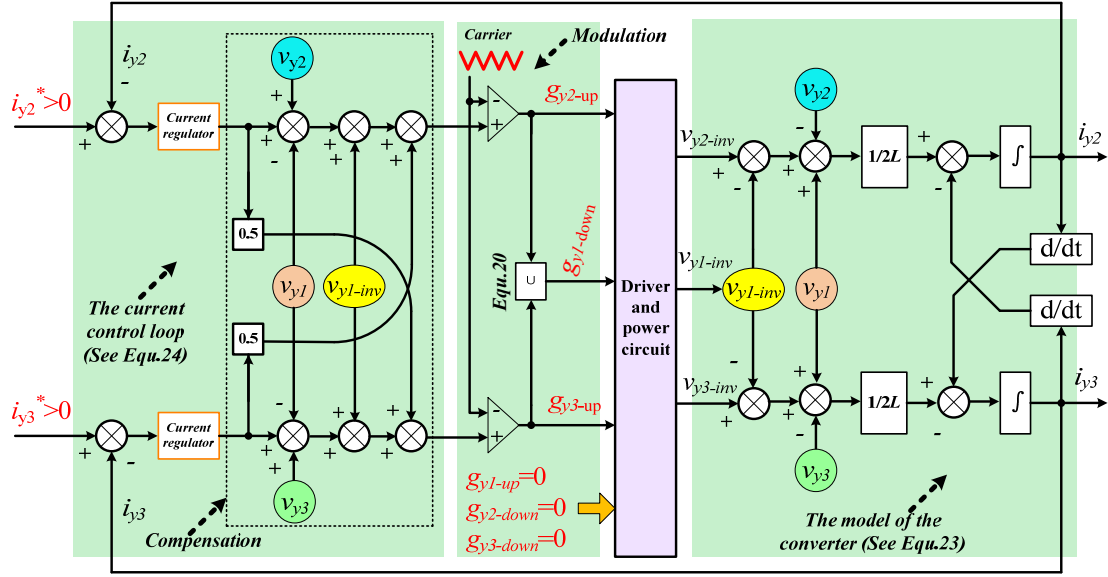
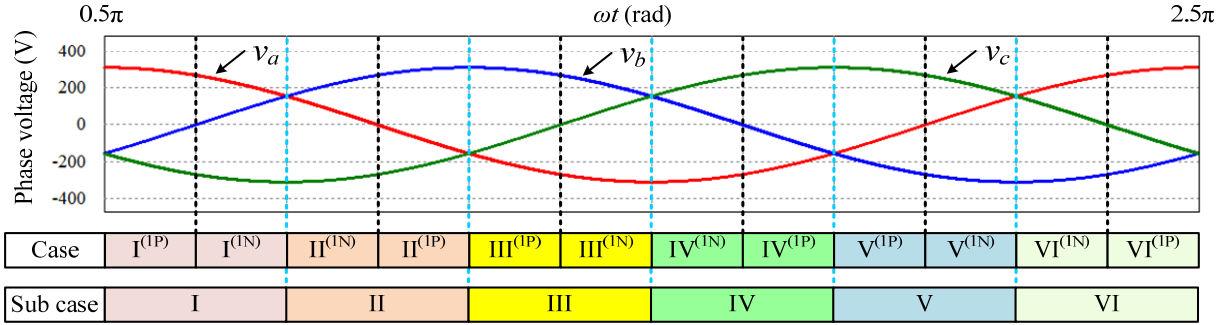

 Fig. 22. Current-loop control diagram for case  $I^{(1N)}$  ( $y1='c'$ ,  $y2='a'$  and  $y3='b'$ ).


Fig. 23. Phase voltages and sub cases.

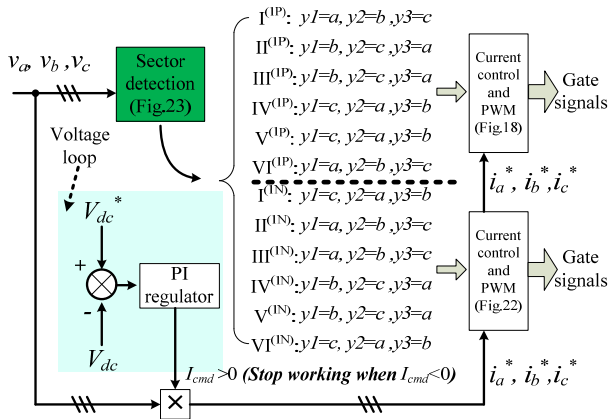


Fig. 24. Control strategy with a DC bus voltage loop.

 TABLE III  
EXPERIMENTAL PARAMETERS

Parameters	Values
Three-phase inductor $L$	0.8mH
Power grid voltage $v_a \sim v_c$	380V(RMS)
Power grid frequency	50Hz
Switching frequency, $f_s$	8kHz
Sample period, $T_s$	0.000125s
Rating power, $P$	55kW
Threshold voltage for regeneration <sup>Ⓛ</sup>	660V
Reference value of DC bus voltage <sup>Ⓜ</sup>	630V
Capacitance of DC bus capacitors <sup>Ⓨ</sup>	13600μF

<sup>Ⓛ</sup> This parameter can be configured by the users.

<sup>Ⓨ</sup> The calculation of the capacitance is done according to the AC voltages, the rating power and other factors [33] - [34].

#### IV. EXPERIMENTAL PROTOTYPE AND VALIDATION

##### A. Descriptions of the Prototype

The experimental prototype is based on a digital microprocessor DSP (Texas Instruments TMS320F28335)

with a clock frequency of 150MHz (6.67ns cycle time). All of the algorithms are implemented in the DSP chip. The DC bus capacitance and the parameters are shown in Table III.

The experimental prototype is based on a digital

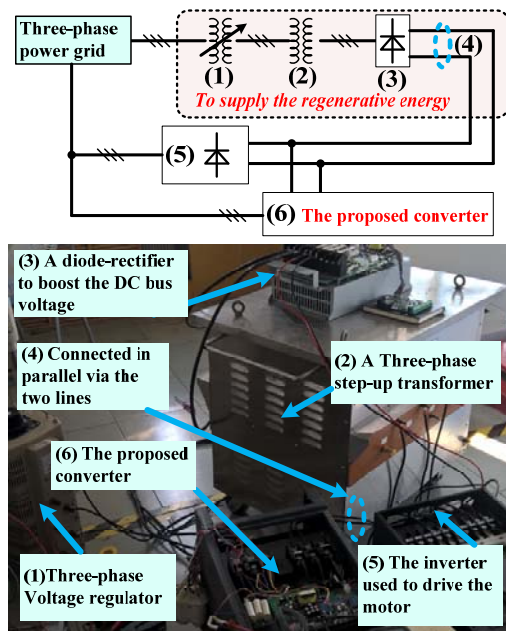


Fig. 25. Experimental prototype in the lab.

microprocessor DSP (Texas Instruments TMS320F28335) with a clock frequency of 150MHz (6.67ns cycle time). All of the algorithms are implemented in the DSP chip. The DC bus capacitance and the parameters are shown in Table III.

### B. Experimental Validations in the Lab

Fig. 25 shows photos of the experimental platform. A step-up transformer (see part (2) in Fig. 25) and a diode-rectifier (see part (3) in Fig. 25) are used to provide the regenerative energy. The voltage regulator (see part (1) in Fig. 25) can tune the DC bus voltage. In the lab, the voltage loop is disabled to verify the current loop. Experimental results are shown in Fig. 26.

Fig. 26(a)-(c) show the AC voltage, the AC current, the zero-order current and the DC bus voltage.  $V_{dc-sensor}$  is the output of the voltage sensor on the control board for  $V_{dc}$ . In addition, the ratio is 300. Thus, when  $V_{dc}=700V$ ,  $V_{dc-sensor}$  can be 2.3V.

The results in Fig. 26 indicate that when the converter is working, the DC bus voltage drops. The AC current is sinusoidal and the power factor is about 1. The zero-order current is kept zero. Fig. 26(d) - (f) show the AC voltage, the AC current and the gate signals. The AC current is highly sinusoidal (the THD is about 8% according to the multi-meter) and the power factor is 1.

In addition, the gate signals in Fig. 26 coincide with the proposed strategy in Fig. 18 and Fig. 22. (In the prototype, the IGBT is off when the gate signal is 5V, and IGBT is on when the gate signal is 0V) Fig. 26(g) shows the three-phase currents, which are all sinusoidal and balanced. The zero-order currents  $i_z$  is around 0, as shown in Fig. 26(h).

The efficiency is also tested in the lab based on the topology in Fig. 25. The currents to the power grid are tuned

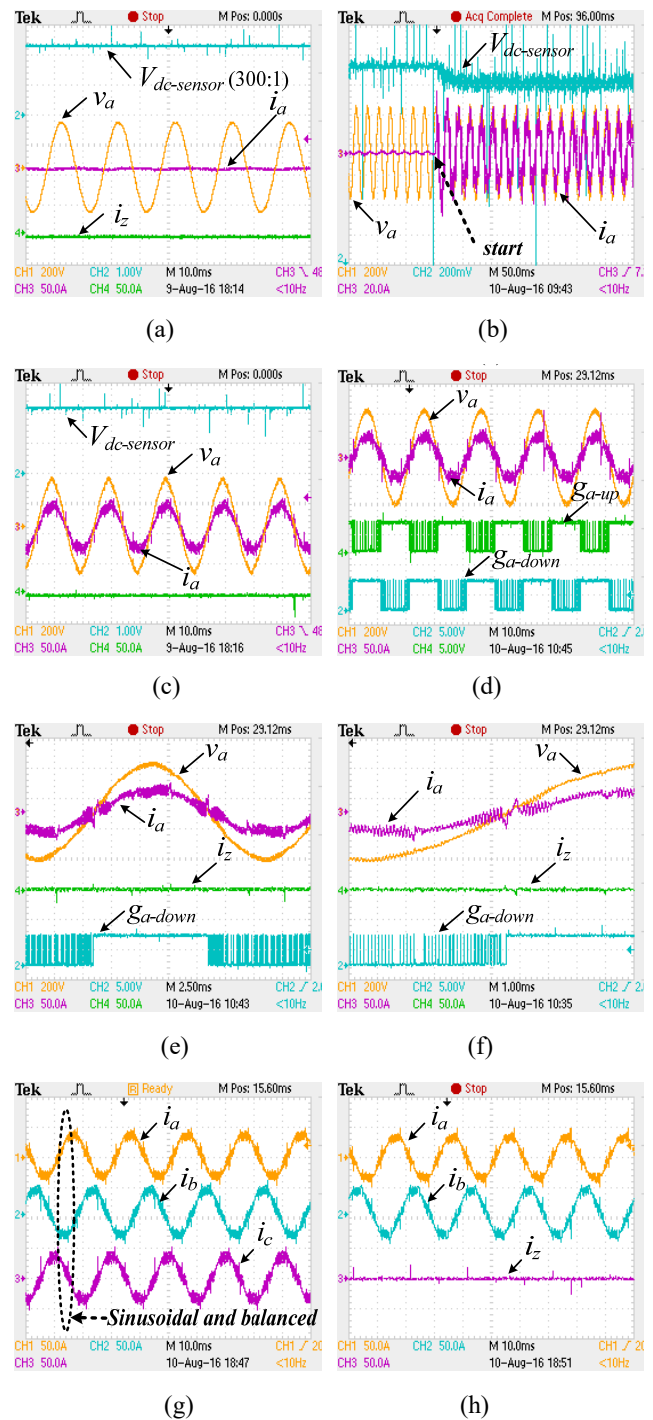


Fig. 26. Experimental results obtained in the lab: (a) DC bus voltage, AC voltage, AC current and zero-order current when the converter is not working. (b) DC bus voltage, AC voltage and AC current when the converter is working. The DC bus voltages drops. The AC current is sinusoidal. (c) DC bus voltage, AC voltage, AC current and zero-order current when the converter is working. The AC current is sinusoidal and the power factor is 1. The zero-order current is 0. (d) AC voltage, AC current and gate signals. The current is sinusoidal. The power factor is 1. (e) AC voltage, AC current, zero-order current and a gate signal (1 cycle of the grid voltage). (f) AC voltage, AC current and gate signals (0.5 cycle of the grid voltage). (g) Three-phase AC currents. (h) Two AC currents and zero-order current.

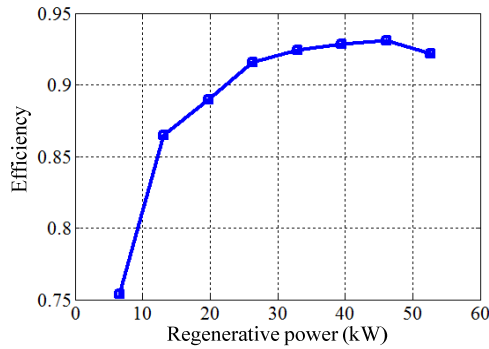


Fig. 27. System efficiency curve.

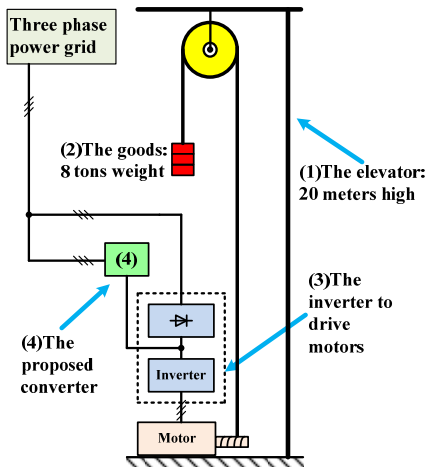


Fig. 28. Experimental prototype in an elevator.

to be 10A ~ 80A (RMS value) and the efficiency is calculated, as shown in Fig. 27. The maximal efficiency is about 93%.

### C. Industrial Applications in Elevators

The proposed converter in this paper is installed in an elevator to validate its performance. The configuration of the elevator is shown in Fig. 28. The weight of the goods is 8 tons. The height of the elevator is 20 meters. The inverter drives the motor to lift the goods. When the goods are falling, the regenerative power is transmitted to the power grid via the proposed converter in this paper (see part (4) in Fig. 28).

The experimental results with an elevator are shown in Fig. 29. The control strategy is shown in Fig. 24, where the DC bus voltage loop is enabled. When the DC bus voltage exceeds the threshold voltage, the converter works automatically to maintain the DC bus voltage.

In Fig. 29(a), the response time of the converter is measured. The result is about 300 $\mu$ s, which is short enough for industrial applications. Fig. 29(b) shows the DC bus voltage and the gate signal. The DC bus voltage is maintained at 630V when the converter is working. Fig. 29(c) shows the DC bus voltage, zero-order current, gate signals and AC currents. In addition, an entire working cycle can be found in the picture. When the DC bus voltage is over the threshold voltage, the converter starts working to maintain the DC bus voltage. When the regenerative power disappears, the

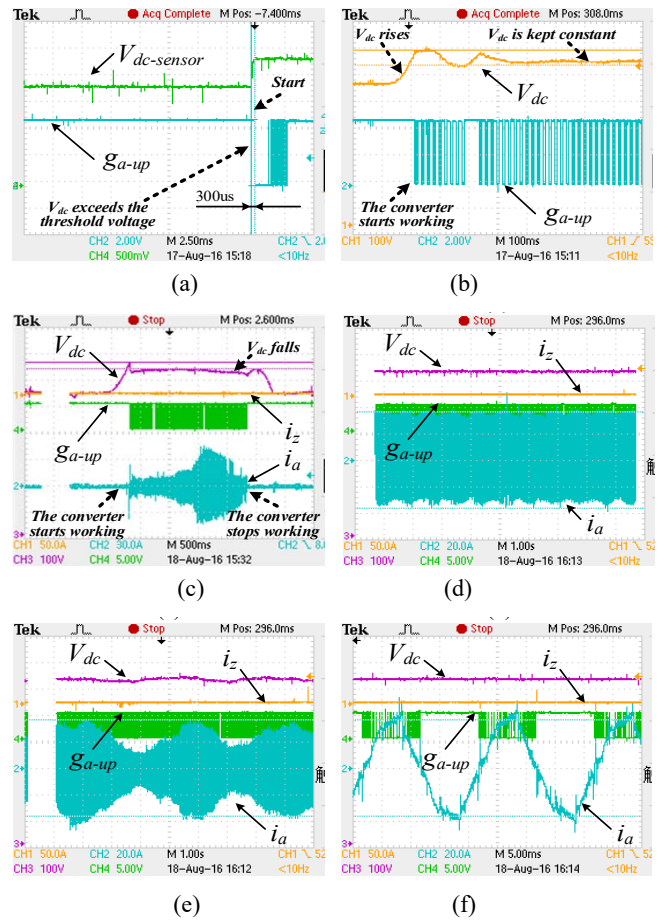


Fig. 29. Experimental results obtained in an elevator: (a) DC bus voltage and gate signals. The response time is measured. (b) The DC bus voltage is kept constant when the converter is working. (c) A set of waveforms in one working cycle. (d) DC bus voltage, zero-order current, gate signals and AC current in the steady state. (e) DC bus voltage, zero-order current, gate signals and AC current in the transient state. (f) DC bus voltage, zero-order current, gate signals and AC current in the transient state (Zoomed in).

converter stops working. Fig. 29(d) shows the DC bus voltages, zero-order current, gate signals and AC current in the steady state. The amplitude of  $i_a$  is kept constant. Fig. 29(e) shows waveforms that are similar to those in Fig. 29(d) in the transient state. The amplitude of  $i_a$  changes with time. However, the DC bus voltage is kept constant. In Fig. 29(f), sinusoidal current can be observed and the proposed control strategy is validated.

### D. Comparison with the Conventional Control Algorithm

As shown in Fig. 2, Fig. 4 and Fig. 5, the conventional control algorithm is not suitable for the proposed DC/AC converter. The conventional control method causes a serious zero-order current, which damages the device and lower the reliability of the system.

In the experiment, the reference currents are set as 10A, 20A, 30A and 40A (Fig. 30(a) - Fig. 30(d)) to test the performance. Fig. 30 shows experimental results, where the



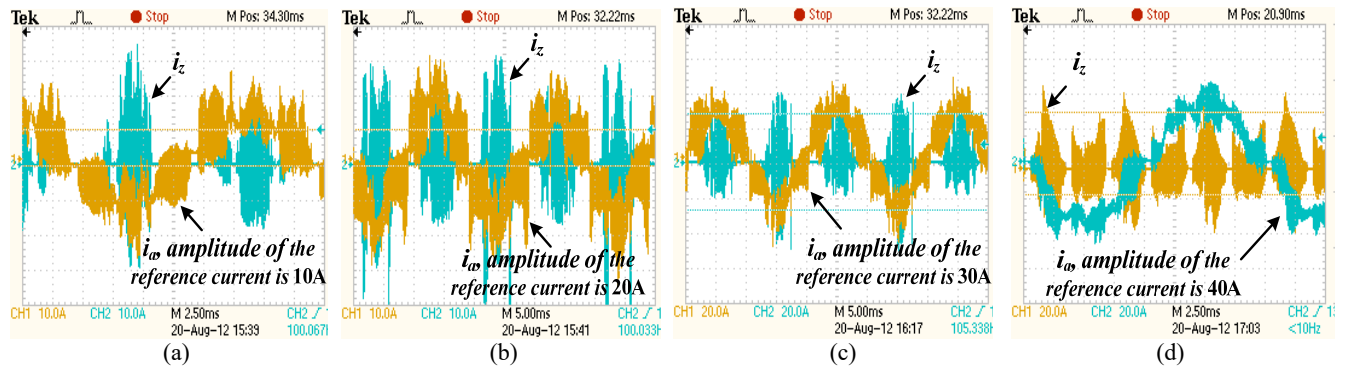






Fig. 30. Serious zero-order current can be observed in the experiments when the conventional control method is adopted.

TABLE IV  
COMPARISON WITH OTHER INDUSTRIAL PRODUCTS

Similar products	Control strategy	Switching frequency	Continuously working ability	The zero-order current	THD of the AC currents	Comments
Product 1, by 	Hysteresis control	Not constant. 38kHz or higher	No. Usually within 1 minute	<b>Almost 0</b>	<b>Low.</b> Usually <10%	See Appendix for reference
Product 2, by 	Line-voltage mode	<b>Constant</b> <10kHz	<b>Yes.</b>	<b>0</b>	Not low. Usually >25%	See Appendix for reference
Product 3, by 	Line-voltage mode	<b>Constant</b> <10kHz	<b>Yes.</b>	<b>0</b>	Not low. Usually >25%	R1000 series, similar to 
Proposed in this paper	Fig. 24	<b>Constant</b> <10kHz	<b>Yes</b>	<b>Almost 0</b>	<b>Low.</b> Usually <10%	See Fig. 26 and Fig. 29

zero-order current can be clearly observed. Hence, the conventional method causes a serious zero-order current and the converter cannot work normally.

Three of the most popular products in the industrial market are chosen for comparison. Table IV shows the comparison results. The three kinds of products are manufactured by IPC®, invtr®, and YASKAWA®.

Compared with the available products on the market, the proposed control method in this paper can eliminate the zero-order current and improve the quality of the AC currents (The THD of the AC current can be lower than 10%). In addition, the switching frequency is low, which enables the converter to work continuously in industrial fields. Hence, the proposed strategy is competitive.

## V. CONCLUSIONS

This paper focuses on developing a control strategy for converters in regenerative applications. Due to the diode rectifier in traditional inverters, zero-order current appears if the control algorithm is not carefully designed. This paper analyzed the flow paths and model of the zero-order current. Simulation results for the zero-order current are similar to the waveforms observed in industrial occasions. The analysis shows that the conventional d-q transformation method is not

suitable for the converter and that the traditional PWM method induces the zero-order current.

This paper established equivalent circuits in different cases and proposed a method to suppress zero-order current. With the proposed PWM method, the gate signals for the upper and lower switches are not complementary. A proportional regulator is introduced to control the AC current. In addition, a DC bus voltage loop is designed to keep the DC bus voltage constant in regenerative applications.

A 55kW experimental prototype was built to validate the proposed strategy. Experimental results obtained in the lab validate the current loop and show that the zero-order current can be eliminated. The prototype was installed in an elevator. When the goods are falling, regenerative energy can be delivered to the power grid by the proposed converter. The obtained results validate the DC bus voltage loop. The prototype works normally and can meet the requirements for regeneration.

The proposed converter can be used in regenerative occasions, such as elevators and electric vehicles. With the proposed strategy, bi-directional power flow is practical. It can also be used to modify traditional diode-rectifier-based inverters and to remove shut resistors, which can reduce electric energy, improve efficiency, make the system more reliable and lower cost.

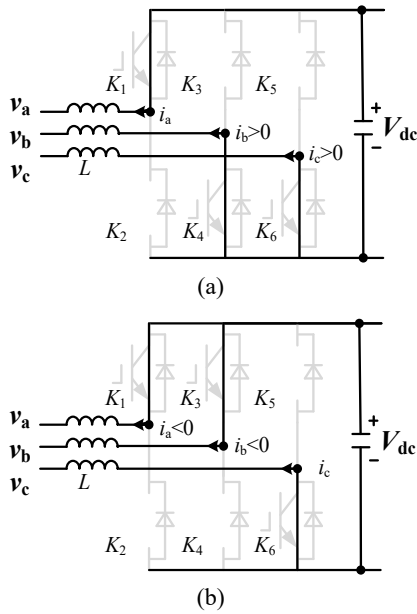


Fig. 31. Equivalent circuits in case  $I^{(IP)}$  and case  $I^{(IN)}$ : (a)  $g_{a-up} = 1$ ,  $i_b > 0$  and  $i_c > 0$  in case  $I^{(IP)}$ , (b)  $g_{c-down} = 1$ ,  $i_b < 0$  and  $i_c < 0$  in case  $I^{(IN)}$ .

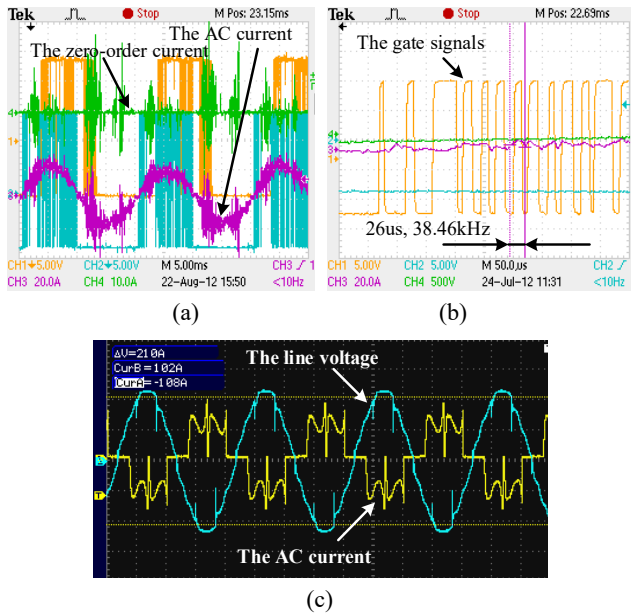


Fig. 32. Experimental results of various products: (a) gate signals, zero-order current and AC current for product 1 in Table IV, (b) gate signals for product 1 in Table IV, (c) line voltage and current for product 2 in Table IV.

## APPENDIX

*A. The Proof of “when  $g_{a-up} = 1$  it can be determined that  $i_b$  and  $i_c$  are controllable only if they are negative” and “when  $g_{c-down} = 1$  it can be determined that  $i_a$  and  $i_b$  are controllable only if they are positive”*

As shown in Fig. 31(a), when  $i_b > 0$ , the parasitic diode of  $K_4$  is on regardless of whether  $g_{b-down}$  is 1 or 0. In addition,

when  $i_c > 0$ , the parasitic diode of  $K_6$  is on regardless of whether  $g_{c-down}$  is 1 or 0.

As shown in Fig. 31(b), when  $i_a < 0$ , the parasitic diode of  $K_1$  is on regardless of whether  $g_{a-up}$  is 1 or 0. In addition, when  $i_b < 0$ , the parasitic diode of  $K_5$  is on regardless of whether  $g_{b-up}$  is 1 or 0.

## B. Experimental Results Obtained with Different Products on the Market

In Fig. 32(a), it can be seen the zero-order current is almost zero and that the AC current is sinusoidal. Fig. 32(b) shows the gate signals. It can be seen that the switching frequency is not constant. In addition, the maximal switching frequency is 38.46kHz. Fig. 32(c) shows the line voltage and current, which are of the same phase. However, the AC current is not sinusoidal.

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