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A New Single Phase Multilevel Inverter Topology with Two-step Voltage Boosting Capability

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Abstract

In this paper, a new single phase multilevel inverter topology with a single DC source is presented. The proposed topology is developed based on the concepts of the L-Z source inverter and the switched capacitor multilevel inverter. The input voltage to the proposed inverter is boosted by two steps: the first step by an impedance network and the second step by switched capacitor units. Compared to other existing topologies, the presented topology can produce a higher boosted multilevel output voltage while using a smaller number of components. In addition, it provides more flexibility to control boosting factor, size, cost and complexity of the inverter. The proposed inverter possesses all the advantages of the L-Z source inverter and the switched capacitor multilevel inverter like controlling the start-up inrush current and capacitor voltage balancing using a simple switching strategy. The operating principle and general expression for the different parameters of the proposed topology are presented in detail. A phase disposition pulse width modulation strategy has been developed to switch the inverter. The effectiveness of the topology is verified by extensive simulation and experimental studies on a 7-level inverter structure.

Key words: Boosting factor, Capacitor voltage balance, Impedance source inverter, Multilevel inverter, Pulse width modulation, Switched capacitor

I. INTRODUCTION

In recent years, one of the most popular power converting systems used for DC to AC conversion is the multilevel inverter (MLI). Compare to classic two-level inverters, MLIs provide better quality output waveforms, lower EMI influence, lower *dv/dt* stress and have more power handling capability with lower power rated switching devices [1], [2]. These advantages enhance the application of MLIs in different fields such as motor drive applications, renewable energy conversion systems, electric vehicles, HVDCs, active filters, distributed power generation, uninterrupted power supplies, induction heating, etc. [1]-[5]. Despite the aforementioned advantages, MLIs suffer due to the requirements of a large number of components and a complex control strategy to generate better quality output waveforms.

These limitations make the whole converting system larger in volume and more expensive. Furthermore, in some applications such as renewable energy conversion systems, boosting the input voltage is required, which increases cost and volume of the whole converting system due to the incorporation of energy storing elements or transformers in the system. Although the conventional MLI topologies namely Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC) and Flying Capacitor (FC) have become viable MLI topologies for industrial applications, they suffer from the aforementioned limitations [3]. Improving the quality of output waveforms and boosting the input voltage to desired levels with a reduced number of components are challenging research issues. To achieve these challenges, a number of attractive MLI structures have been published in the literature [6]-[15]. Some topologies, popularly known as "Reduced Device Count (RDC) MLI topologies," have been developed with the main objective of generating a larger number of voltage levels with a reduced component count [3]. Popular RDC-MLI topologies include the cascaded half bridge MLDCL, T-type, packed U-cell, series connected switched sources (SSCS) and switched series/parallel sources (SSPS) MLI structures. These RDC-MLIs have no capability to boost the input voltage. Furthermore, when increasing the output voltage levels, the device count increases considerably

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despite the fact that it is lower than that of classical MLI topologies. To boost the input voltage and to reduce the number of DC power supplies, new types of MLI topology have been presented in recent years. They are known as switched capacitor multilevel inverter (SCMLI). The SCMLI uses capacitors as alternate DC supplies to the inverter to generate different output voltage levels. In addition, to maintain the capacitor voltages, the SCMLI does not require any complex control algorithm since it simply switches the basic units in series/parallel modes [6]-[12]. However, there is a requirement of a large number of capacitors to boost the input voltage to high levels. This makes the converting system large, expensive and complex. Thus, reducing the number of capacitors in the SCMLI is another challenging issue of research.

Along with the development of MLI topologies, another innovative inverter topology to boost input voltage has been introduced, which is popularly known as impedance source or Z-source inverter (ZSI). The conventional ZSI (C-ZSI) was developed based on the classic two-level inverter [17]. The C-ZSI is considered as one of the viable converting systems in different applications due to its unique buck-boost capability. However, the C-ZSI possesses drawbacks due to its requirement of a large capacitor in the impedance network, no capability to control start-up inrush current, high switching stress, and lack of flexibility in controlling the boosting factor. Some innovative modified impedance structures have been proposed to mitigate the aforementioned limitations of the C-ZSI [18]-[25]. One of the attractive structures is the L-ZSI, which provides more boosting capability, no capacitor voltage stress and lower switching stress when compared to the C-ZSI [22]. In addition, the L-ZSI has the ability to control the input inrush current during transient conditions. However, for a high boosted output, the number of inductors needs to be increased in the impedance network, which increases the size and cost of the inverter.

It has been observed that, both the SCMLI and the L-ZSI are constrained by the requirement of a large number of energy storing elements for generating high boosted output which enhances the size, cost and complexity of the whole converting system. Furthermore, the L-ZSI does not have the ability to generate multilevel outputs. Thus, a new MLI topology based on the concepts of the L-ZSI and the SCMLI is proposed in this paper. The contributions of this paper are as follows:

- A new MLI topology is proposed with one DC source. This topology is developed based on the concept of the L-ZSI and the SCMLI.
- The proposed topology has the ability to boost the input voltage in two steps. The first step is by the impedance network and the second step by the SCMLI. The presented topology provides a greater boosting factor when compared to that for many of the existing topologies.
- Since the number of variables is greater, more flexibility to control the boosting factor as well as the size and volume of the inverter as per the requirements and applications in the case of the proposed topology when compared to other topologies like the SCMLI and the L-ZSI. Under the same boosting factor, the proposed topology has been compared with the conventional SCMLI and the conventional L-ZSI.
- The proposed topology requires a smaller number of switching devices when compared to conventional MLI topologies and a number of the more popular RDC-MLI topologies.
- The proposed topology shows all the advantages of the L-ZSI and the SCMLI like controlling of the input inrush current during the transient state and capacitor voltage balancing using a simple switching strategy.
- The presented topology is easily extendable for a higher number of voltage levels and higher boosting factors.

The phase disposition PWM (PDPWM) technique is developed for switching the proposed topology. Extensive simulation and experimental studies of a 7-level MLI of proposed topology has been carried out to validate its effectiveness and merits.

The organisation of this paper is as follows. In section II, a description of the proposed topology is presented. Further, the operating principle and general expressions for different parameters are presented in the sub-sections of section II. The modulation strategy for the proposed topology is presented in section III. A comparison study of the proposed topology with the other topologies is discussed in section IV. Section V presents simulation and experimental studies. The conclusion is presented section VI.

II. PROPOSED TOPOLOGY

Fig. 1(a) shows the general structure of proposed MLI topology consisting of an L-ZSI impedance network, a DC link circuit, a switched capacitor (SC) circuit and a H-Bridge circuit in a cascaded arrangement. The L-ZSI impedance network is fed by an input voltage source (V_{DC}). The DC link circuit consists of a power switch (S_L), a power diode (D_L) and a capacitor (C_L). The SC circuit is developed by cascading a number of SC basic units. Each basic unit consists of a capacitor, a power diode and two switching devices as shown in Fig. 1(a). V_{DC} is boosted by the impedance network by applying the necessary switching states in the DC link circuit. In addition, the output of this circuit acts as the input to the SC circuit. Further, the SC circuit boosts its input and generates a multilevel output of the positive polarity by switching the basic units in series/parallel modes. Alternating voltage levels at the load

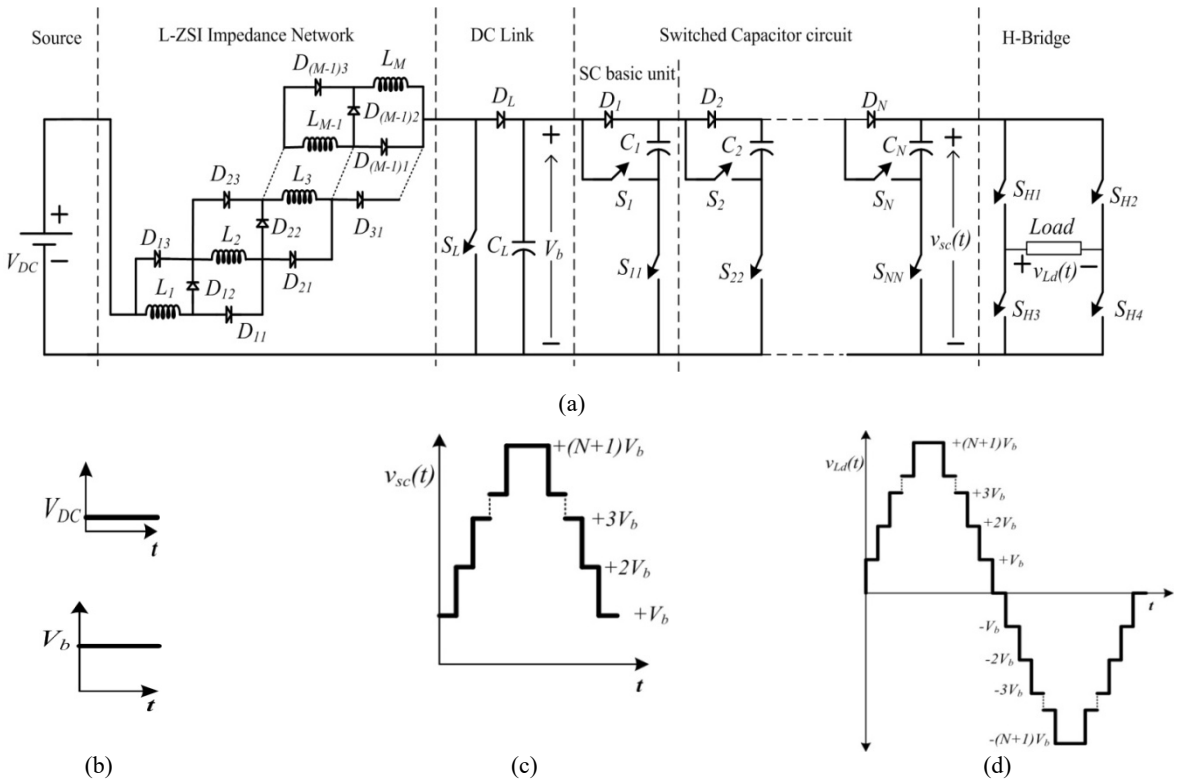

Fig. 1. Proposed MLI topology and wave shapes of different voltages, (a) proposed MLI topology structure, (b) input DC voltage (V_{DC}) and boosted DC link voltage (V_b), (c) output voltage of SC circuit ($v_{sc}(t)$), (d) load voltage ($v_{Ld}(t)$).

terminals are generated by an H-bridge circuit cascaded with a SC circuit. Fig 1(b) shows the wave shape of the input voltage, V_{DC} and the output of the impedance network, V_b. Fig 1(c) shows the wave shape of the output of the SC circuit, $v_{sc}(t)$. The wave shape for boosted multilevel output voltage, $v_{Ld}(t)$ is shown in Fig 1(d). It can be observed that the proposed topology has the ability to boost the input voltage in two steps. The first step is carried out by impedance network and second step is carried out by the SC circuit. The operating principle and general expression for different parameters of the proposed topology are presented in the next sub-sections.

A. Operating Principle

The operating principle of the proposed topology is discussed considering M number of inductors (assume that all of the inductors have same value of inductance, L) in the L-ZSI impedance network, and N number of basic units in the SC circuit. All of the inductors in the impedance network become parallel to each other and store energy from V_{DC} while S_L of the DC link circuit is in the ON state as shown in Fig. 2(a). During this state, (D_{11}, D_{13}, D_{21}, D_{23}....$D_{(M-1)1}$, $D_{(M-1)3}$) and (D_L, D_{12}, D_{22}....$D_{(M-1)2}$) are in the ON and OFF states, respectively. Further, the DC link capacitor, C_L discharges its energy towards the SC circuit during this state. When S_L is in the OFF state, all of the inductors are connected in series as (D_{12}, D_{22}....$D_{(M-1)2}$) enter the ON state and (D_{11}, D_{13}, D_{21}, D_{23}....$D_{(M-1)1}$, $D_{(M-1)3}$) are in the OFF state as shown in Fig. 2(b). During this state, the inductors transfer energy towards the SC circuit and charge C_L through D_L. The following equations (1) and (2) are obtained from Fig. 2(a) and (b), respectively.

$$V_L = V_{DC} \tag{1}$$

$$MV_L = V_{DC} - V_b \tag{2}$$

Where V_L presents the inductor voltage. By the application of the volt-sec balance principle on the inductor voltage, the average value of the DC link voltage, V_b can be expressed by (3).

$$V_b = \frac{1 + \{(M-1)D\}}{1-D} V_{DC} \tag{3}$$

Where D is the duty ratio corresponding to S_L. From (3), it is observed that V_b can be varied by changing D and M. The range for D is [*0-1*].

For the analysis of the SC and H-bridge circuits, it is assumed that the input voltage to the SC circuit i.e. V_b remains constant throughout the operation. While (S_{11}, S_{22}....S_{NN}) and (S_1, S_2....S_N) are in the ON and OFF states respectively in the SC circuit as in Fig 1(a), (C_1, C_2, C_3....C_N) store energy from V_b through (D_1, D_2, D_3....D_N) and are charged to V_b. This mode is known as the parallel mode of the basic units. Similarly, all of the capacitors are connected in series while (S_1, S_2....S_N) and (S_{11}, S_{22}….S_{NN}) are in the ON

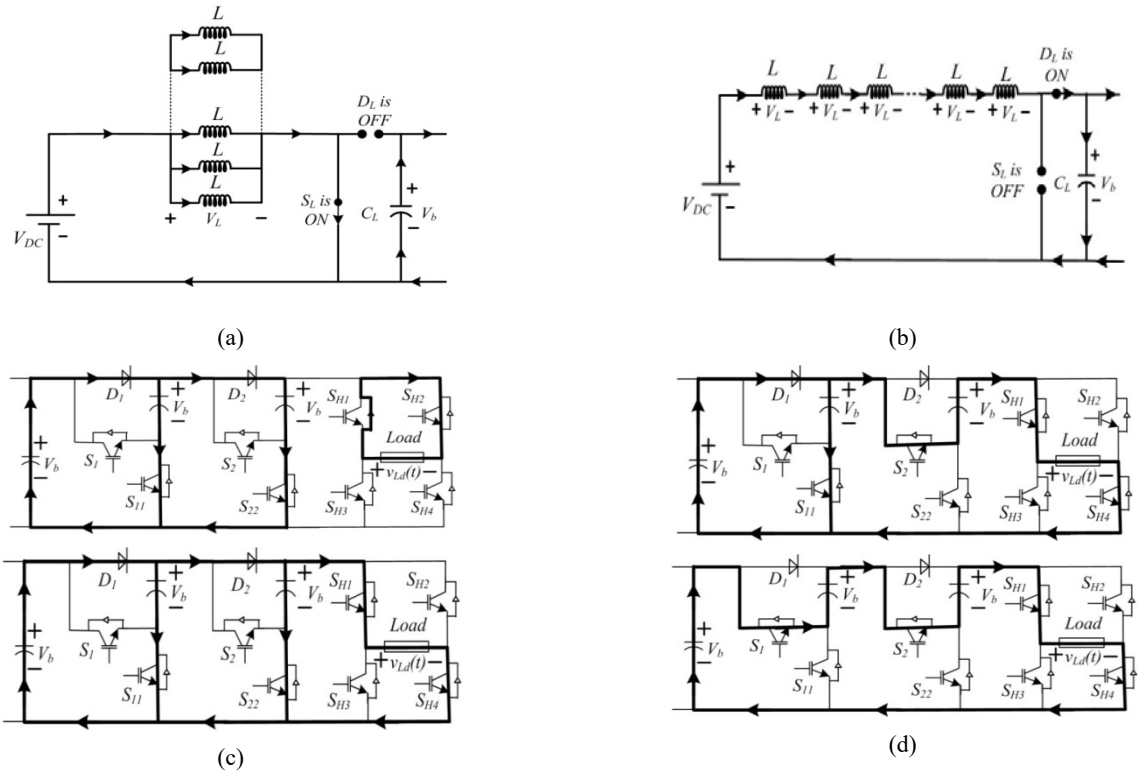

Fig. 2. Equivalent circuits for: (a) a L-ZSI impedance network and a DC link circuit when the inductors are in the charging mode; (b) a L-ZSI impedance network and a DC link circuit when the inductors are in the discharging mode; (c) SC and H-bridge circuits for *N=2* when the load voltages are *0* and $+V_b$; (d) SC and H-bridge circuits for *N=2* when the load voltages are +2 V_b and +3 V_b.

and OFF states, respectively. Furthermore, in this mode, (D_1, D_2, D_3....D_N) are in the OFF state. This mode is known as the series mode of the basic units. In this mode, all of the capacitors transfer energy towards the load. In addition, all of the capacitor voltages are added up with V_b and an output voltage of $(N+1)V_b$ is produced. By switching individual basic unit in the series/parallel modes, different levels of output voltage can be produced. Table 1 shows the states of different switches in the SC and H-bridge circuits corresponding to different load voltage levels for a positive half cycle. In addition, Table 1 shows the state of the SCs (either charging or discharging) corresponding to different voltage levels. Where '1' stands for the ON state and '0' stands for the OFF state of the switching device. Furthermore, '+' stands for the charging state and '-' stands for the discharging state of the SC. Different voltage levels at the load terminals are produced as follows:

- For generating $+V_b$ at the load terminals, (S_1, S_2....S_N) are in the OFF state and (S_{11}, S_{22}....S_{NN}) are in the ON state in the SC circuit. In addition, in the H-bridge circuit (S_{1H} , S_{4H}) are in the ON state and (S_{2H} ,S_{3H}) are in the OFF state. During this combination of switching states, all of the capacitors are in the charging state as shown by the '+' sign in Table 1.
- For generating $+2\ V_b$ at the load terminals, all of the switches remain at the same state as earlier except for S_N and S_{NN}. S_N is in the ON state while S_{NN} is in the OFF state. During this combination of switch states, all of the capacitors are in the charging mode except for C_N which is in the discharging state as shown by the '-' sign in Table 1. Similarly, for generating $+3V_b$, all of the switches are in the same state as the previous state except $S_{(N-1)}$ and $S_{(N-1)(N-1)}$. $S_{(N-1)}$ and $S_{(N-1)(N-1)}$ are in the ON and OFF states, respectively. In this combination of switch states, all of the capacitors are in the charging state while C_{N-1} and C_N are in the discharging state as shown in Table 1.
- In a similar way, for generating the maximum output voltage $+(N+1)V_b$, (S_1, S_2....S_N) are in the ON state while (S_{11}, S_{22}....S_{NN}) are in the OFF state and the H-bridge switches remain in same state as earlier. All of the capacitors are in the discharging state under this condition of the circuit.
- Zero voltage at the load terminal is produced by simultaneously turning ON either upper or lower two switches of the H-bridge circuit. Under this condition, for maintaining charging states for all of the capacitors, ($S1$, S_2....S_N) are in OFF state while (S_{11}, S_{22}....S_{NN}) are in ON state as shown in Table 1.
- Similarly, negative voltage levels at the load terminals can be produced by switching (S_{H2}, S_{H3}) and (S_{H1}, S_{H4}) in ON and OFF states respectively in the H-bridge.

TABLE I
STATES OF THE SWITCHES AND SWITCHED CAPACITORS FOR DIFFERENT OUTPUT VOLTAGE LEVELS IN A POSITIVE HALF CYCLE

Level no	Output voltage levels	State of the switches			Capacitor states
		$(S_1S_2\ldots\ldots S_{N-1}S_N)$	$(S_{11}S_{22}\ldots\ldots S_{(N-1)(N-1)}S_{NN})$	$(S_{H1}\ S_{H2}\ S_{H3}\ S_{H4})$	$C_1C_2\ldots\ldots\ldots C_{N-1}C_N$
1	*0*	(0 0 …….0 0)	(1 1..……..1 1)	(1 1 0 0)	+ +……+ +
	0	(0 0 …….0 0)	(1 1..……..1 1)	(0 0 1 1)	+ +……+ +
2	$+V_b$	(0 0 …….0 0)	(1 1..……..1 1)	(1 0 0 1)	+ +……+ +
3	$+2V_b$	(0 0 …….0 1)	(1 1..……..1 0)	(1 0 0 1)	+ +……+ + -
4	$+3V_b$	(0 0 …….1 1)	(1 1..……..0 0)	(1 0 0 1)	+ +……- -
.....	……	……			……
N+1	$+NV_b$	(0 1 ……..1 1)	(1 0..……..0 0)	(1 0 0 1)	+ - ……- -
N+2	$+(N+1)V_b$	(1 1 ……..1 1)	(0 0..……..0 0)	(1 0 0 1)	- - ……- -

The current flow paths in the SC and H bridge circuits for *N=2* are shown in Fig. 2(c) and 2(d). Fig. 2(c) presents the current flow paths when the load voltages are *0* and $+V_b$, respectively. Similarly, for $+2V_b$ and $+3V_b$ output voltage levels, the current flow paths are presented in Fig. 2(d).

B. General Expression for Different Parameters

The generated total output voltage levels (N_{levels}), required number of switching devices ($N_{s/w}$), diodes (N_{dio}), capacitors (N_{cap}) and maximum load voltage (V_{Lmax}) of the proposed inverter are expressed in terms of *M* and *N* as shown in Table II. Furthermore, Table 2 presents expression for the boosting factor (*B*) of the inverter which is defined as the ratio between the maximum output voltage of the SC circuit, $(v_{sc}(t))_{max}$ and the input voltage, V_{DC}. From the expression of *B*, it is observed that by varying *M*, *N* and *D*, the desired boosting factor of the inverter can be achieved. The variation of *B* with respect to *D* for different values of *N* and a constant *M* is shown in Fig. 3(a). Similarly, Fig. 3(b) presents the variation of *B* against *D* for different values of *M* and a constant *N*. In both cases, *B* of the inverter increases with increasing values of *M*, *N* and *D*. Thus, the output voltage levels of the proposed inverter can be controlled by varying either *M* or *N* or *D* which provides more flexibility for selection of the size, volume and complexity of the inverter, which leads to determination of the economic cost of the inverter as per the requirements and applications. Determination of the total blocking/standing voltage of the inverter is one of the more important parameters for deciding the cost of an inverter since the rating and cost of components increase with increasing values of the blocking voltage. As per the above analysis, it can be said that the maximum blocking voltage for S_L , S_1 , S_2....S_N are same and equal to V_b. However, for S_{11} , S_{22}....S_{NN}, the maximum blocking voltages are V_b, $2V_b$, $3V_b$....NV_b, respectively. The maximum blocking voltage for all of the switches in the H-bridge circuit is

TABLE II
GENERAL EXPRESSIONS FOR DIFFERENT QUANTITIES

Parameters	Expressions
N_{Levels}	$2N+3$
$N_{S/W}$	$2N+5$
N_{dio}	$3(M-1)+N$
N_{cap}	$N+1$
$V_{L\max}$	$(N+1)V_b$
B	$\frac{(N+1)\{1+(M-1)D\}}{1-D}$

$(N+1)V_b$. The total maximum blocking voltage of the inverter is presented by (4). It is observed that the blocking voltage of the inverter increases with increasing values of the boosting factor.

$$V_{BLOCK} = \frac{(N+1)(N+10)}{2} \tag{4}$$

III. MODULATION STRATEGY FOR THE PROPOSED TOPOLOGY

The phase disposition pulse width modulation (PDPWM) is selected as the modulation technique to switch the proposed inverter. In this section, the development of the PDPWM for the proposed inverter with *M*=2 and *N*=2 is discussed. With *M=2* and *N=2*, the generated output voltage levels, N_{levels} is *7*. Thus, the number of required carrier signals is (N_{levels}-1) i.e. *6* for developing the PDPWM. Fig 4(a) shows different carrier signals (C_{1r}, C_{2r} ,C_{3r}, C_{11r}, C_{22r}, C_{33r}), the modulation signal ($m(t)$) and different switching signals while considering a modulation index of unity. The modulation index (*ma*) is defined as the ratio between the peak value of modulation

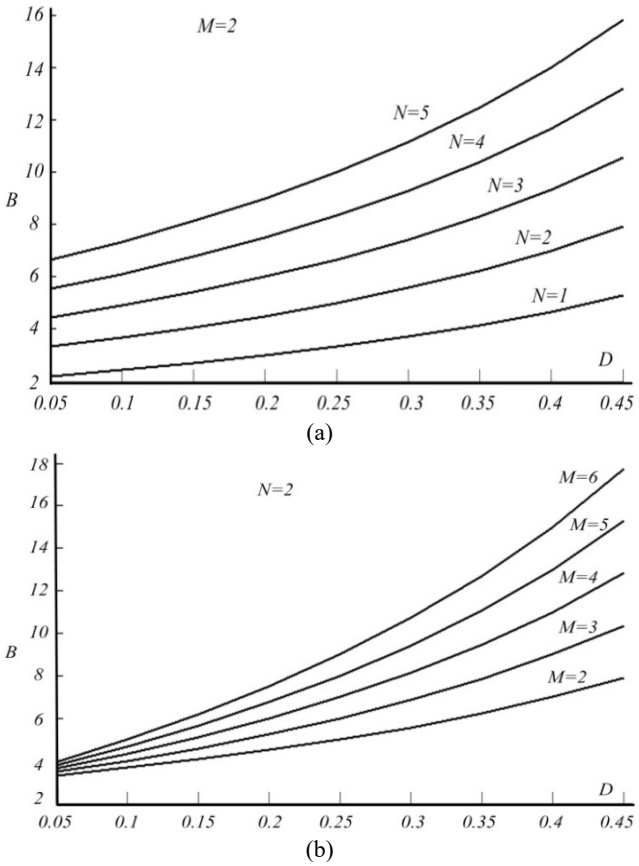

Fig. 3. Variation of the boosting factor, B with respect to different values of the duty ratio (D) for: (a) different values of *N* with *M=2*; (b) different values of *M* with *N=2*.

signal and the peak value of highest carrier signal. Fig 4(b) and (c) show the sub-circuits to generate different logical signals. In sub-circuit 1, *m(t)* is compared with different DC values corresponding to each of the output voltage levels and generating logical signals (I_1, I_2, I_3, I_{11}, I_{22}, I_{33}).

These logical signals are used in sub-circuit 2 to generate the logical signals (P_1, Q_1, P_2, Q_2, P_3, Q_3, P_{11}, Q_{11}, P_{22}, Q_{22}, P_{33}). Different switching pulses are generated by applying logical operations on the output signals of sub-circuit 2 as shown in (5) to (12). Where + indicates the OR operation. Since *SL* is a fixed duty ratio square pulse signal, it is not produced from sine triangle comparison. The same discussion for developing the PDPWM can be extended for higher values of voltage levels by increasing the number of carrier signals.

$$S_1 = P_3 + P_{33} \tag{5}$$

$$S_{11} = \overline{P_3 + P_{33}} \tag{6}$$

$$S_2 = P_3 + Q_3 + P_2 + P_{33} + Q_{33} + P_{22} \tag{7}$$

$$S_{22} = \overline{P_3 + Q_3 + P_2 + P_{33} + Q_{33} + P_{22}} \tag{8}$$

$$S_{H3} = P_{11} + P_{22} + P_{33} + Q_{22} + Q_{33} \tag{9}$$

$$S_{H1} = \overline{P_{11} + P_{22} + P_{33} + Q_{22} + Q_{33}} \tag{10}$$

$$S_{H4} = P_1 + P_2 + P_3 + Q_2 + Q_3 \tag{11}$$

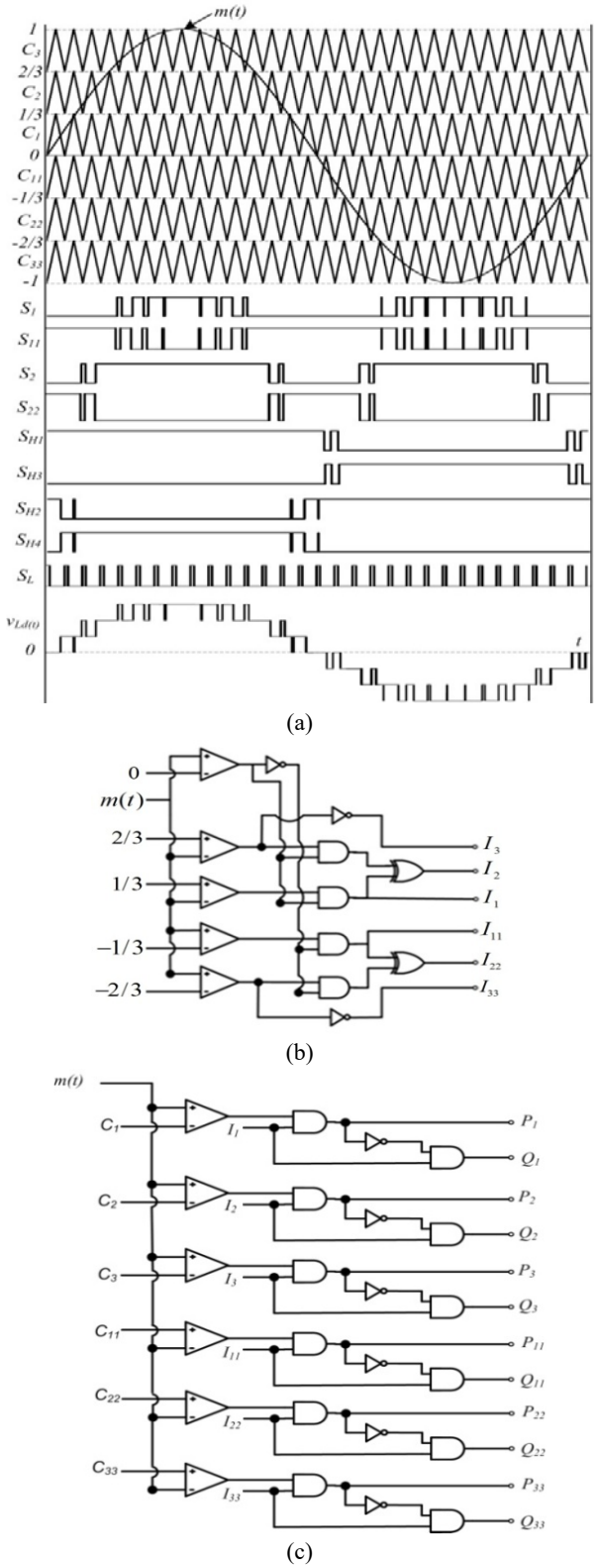

Fig. 4. Multicarrier phase disposition PWM technique for the proposed topology; (a) carrier signals, modulating signals, different switching pulses and output voltage; (b) sub-circuit 1; (c) sub-circuit 2.

$$S_{H2} = \overline{P_1 + P_2 + P_3 + Q_2 + Q_3} \tag{12}$$

TABLE III
GENERAL EXPRESSIONS FOR DIFFERENT QUANTITIES

Topology	Boosting factor (B)	Remarks
C-ZSI	$\frac{1}{1-2D}$	Unique buck/boost capability; lack of flexibility to control boosting factor; high capacitor and switching stress.
SL-ZSI	$\frac{1+D}{1-3D}$	Higher boosting factor can be achieved as compared to that for CZI; requirement of capacitor in impedance network; no capability to suppress inrush current during transient condition.
L-ZSI	$\frac{1+(M-1)D}{1-D}$	More boosting factor compared to CZSI for $M=3$; no need of capacitor in the impedance network; inherent inrush current control during transient state but requires larger impedance network for higher boosting factor.
EB-ZSIZS	$\frac{1}{1+2D^2-4D}$	More boosting compared to SL-ZSI and L-ZSI ($M=2$) but the range of D is small.
SCMLI	$N+1$	Needs large number of switches and capacitors for higher boosting and higher number of levels; Less flexibility to control boosting factor.
Proposed	$\frac{(N+1)\{1+(M-1)D\}}{1-D}$	More boosting factor compared to other topologies; More flexible for controlling boosting factor; ability to generate multilevel output waveform; has inherent inrush current controlling capability; requires simple capacitor voltage balancing scheme.

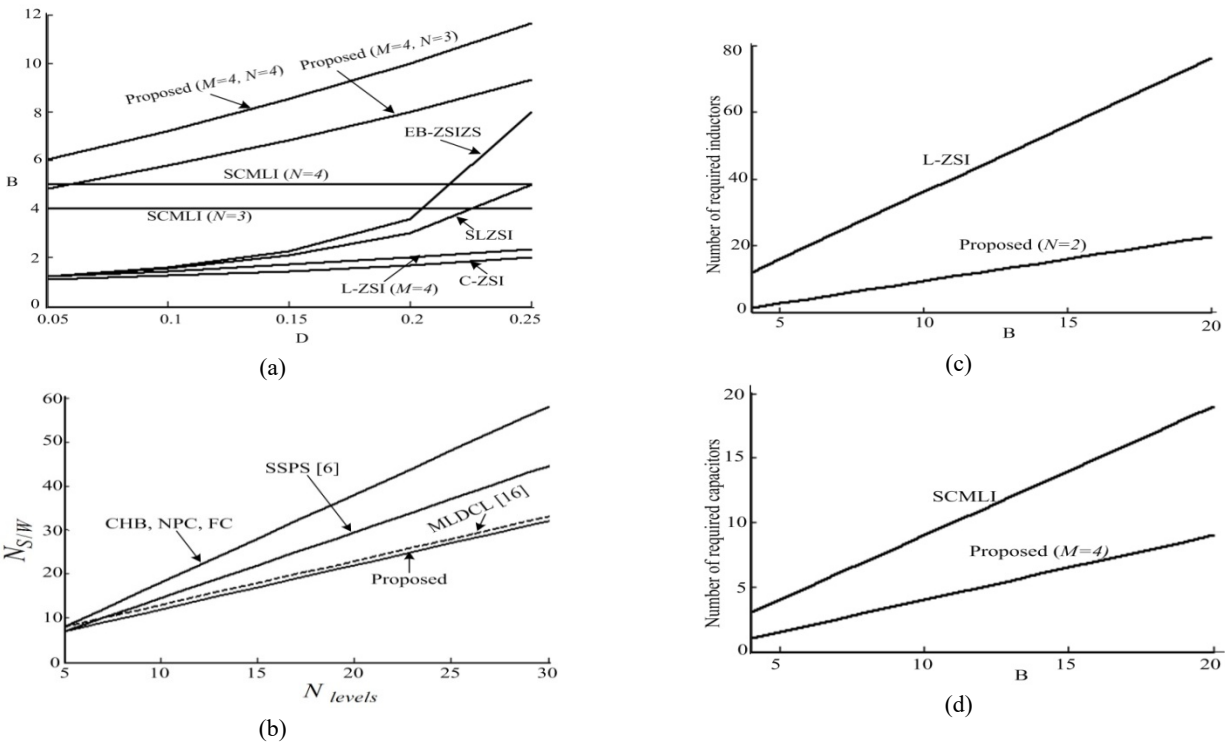

Fig. 5. Comparison study of the proposed topology with other topologies for: (a) B against D; (b) the number of switching devices against the number of output voltage levels; (c) the number of inductors required against the boosting factor; (d) the number of SCs required against the boosting factor.

IV. COMPARISON STUDY

Fig. 5(a) shows a comparison of the boosting factor of the proposed topology with that of the conventional ZSI (C-ZSI) [17], SL-ZSI [19], L-ZSI [22], SCMLI [8] and EB-ZSISZ [23] for $M=4$ and $N=3,4$. It is observed that the boosting factor of the proposed topology is much higher than that of the other topologies. Furthermore, the proposed topology can generate a multilevel output voltage when compared to the C-ZSI, L-ZSI, SL-ZSI and EB-ZSIZS. During the transient state, the inductors in the impedance network are open circuited. This

provides the inrush current controlling of the proposed inverter. This feature is not available in the C-ZSI or SL-ZSI. Fig. 5(b) shows a comparison study of the proposed topology with the classical MLI topologies and two popular RDC-MLI topologies (namely SSPS [6] and MLDCL [16]) in terms of the number of switching devices against the number of output voltage levels. It is observed that for producing same number of output voltage levels, the proposed topology requires a smaller number of switching devices. Thus, the requirement of a gate driver and a protection circuit are also reduced. Fig. 5(c) and 5(d) present a comparison between the proposed topology and the L-ZSI and SCMLI in terms of the requirement of number of inductors and capacitors for producing same amount of *B*. It can be concluded from Fig. 5(c) and 5(d) that for the same boosting factor, the size and cost of the proposed topology are much lower than those of the L-ZSI and SC-MLI. In addition, some remarks are summarised in Table-3 for a better comparative study between the proposed topology and other topologies.

V. Efficiency Comparison

The efficiency of the proposed topology is compared with the C-ZSI, SL-ZSI, L-ZSI, SCMLI. The following assumptions have been considered for the sake of simplicity:

1. The comparison has been done at the same boosting factor.
2. The switching loss for all of the inverters has been neglected.
3. All of the inductor and capacitor values are the same.
4. The equivalent series resistance for the inductors and capacitors are considered same for all of the inverters.
5. For the SCMLI, the conduction loss of the switches has been considered during the discharging state condition of the circuit.
6. All the inverters are analyzed for a resistive load.

The equations for the efficiency of the C-ZSI, SL-ZSI, L-ZSI, have been taken from [22]. In addition, the efficiency of the SCMLI has been derived based on [8]. The efficiency of the proposed topology can be represented as [13].

$$\eta_{TS} = \eta_L \times \eta_{DC} \times \eta_{SC} \quad (13)$$

Where:

η_L : the efficiency of the L-ZSI circuit of the proposed topology.

η_{DC} : the efficiency of the DC link circuit of the proposed topology. For the sake of simplicity, the efficiency of the DC link circuit is considered to be 100%.

η_{SC} : is the efficiency of the SC circuit of the proposed topology.

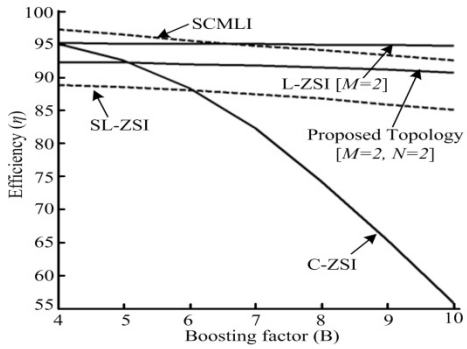

Fig. 6. Efficiency comparison of the proposed topology with other topologies.

Based on [22] and [8], the efficiency of the proposed topology has be derived. Table IV presents an equation for the efficiency of the proposed topology as well as the other topologies. Where:

D is the shoot-through duty ratio, $r_L$and $r_C$are the equivalent series resistances of the inductor and capacitor, respectively, $r_{on}$is the ON state resistance of the switching device, r_l is the load resistance, and V_d is the diode drop during the conduction state. Consider that r_L, r_C, r_{on}, r_l and V_d are 80$m\Omega$, 112$m\Omega$, 0.85Ω (from datasheet of the IRF840), 100Ω and 0.8V, respectively. The efficiencies of different inverters have been determined. Fig. 6 presents an efficiency comparison of the proposed topology with other topologies while considering a *16.5 V* input supply voltage. It can be observed that at the same boosting factor the efficiency of the proposed topology is higher than that for the C-ZSI and SL-ZSI. Further, it can be observed that with the specified assumptions the efficiency of the proposed topology is above 90% throughout the boosting factor range. Nevertheless, the efficiency of the proposed topology is less than that for the L-ZSI and SCMLI. An efficiency comparison of the proposed topology with that of the EB-ZSIZS has not performed due to page limitations. However, from [23], it can be concluded that the proposed topology provide greater efficiency when compared to that of the EB-ZSIZS.

VI. Simulation and Experimental Studies

To verify the effectiveness of the proposed topology, simulation and experimental studies have been performed for a topology with *M=2*, *N=2*, *D=0.2*, V_{DC}*=16.5V*, switching frequency, f_{sw}*=1.5kHz*, and modulation index, *ma*=1. A *R-L* load with *R=100*Ω and *L=25mH* is supplied by an inverter. The value of the capacitance for the SCs are calculated based on the procedure presented in [6]. Considering a voltage ripple of less than *5%* of the maximum SC voltage, the values for the SCs are C_1*=5000μF* and C_2*=12000μF*. Similarly, inductors in the impedance network are selected considering a current ripple of less than 1A (30% of the average inductor current). The inductors values are L_1*=*L_2*=2.67mH*. With the

TABLE IV
EQUATIONS FOR THE EFFICIENCIES OF DIFFERENT TOPOLOGIES

Topology	Efficiency (η)
C-ZSI	$\eta_C = \dfrac{1}{\dfrac{2(1-D)^5}{(1-2D)^2}\left(\dfrac{r_L}{r_l}\right)+\dfrac{2D^2(1-D)^3[(1-2D)^2+1]}{(1-2D)^4}\left(\dfrac{r_c}{r_l}\right)+\dfrac{V_d(1-D)}{V_{DC}}+1}$
SL-ZSI	$\eta_S = \dfrac{1}{\dfrac{4(1-D)^3[(1-D)^2+D^2]}{(1-3D)^2}\left(\dfrac{r_L}{r_l}\right)+\dfrac{16D^2(1-D)^3}{(1-3D)^2}\left(\dfrac{r_c}{r_l}\right)+\dfrac{3V_d(1-D)}{V_{DC}}+1}$
L-ZSI	$\eta_L = \dfrac{1}{\dfrac{M[(1-D)^2+D^2]}{(1-D)}\left(\dfrac{r_L}{r_l}\right)+\dfrac{V_d(M-1+D)}{V_{DC}[1+(M-1)D]}+1}$
SCMLI	$\eta_{SC} = \dfrac{1}{\dfrac{Nr_c}{Nr_c+Nr_{on}+r_l}+\dfrac{Nr_{on}}{Nr_c+Nr_{on}+r_l}+1}$
Proposed	$\eta_{TS} = \dfrac{1}{\left[\dfrac{M(N+1)^2[(1-D)^2+D^2]}{(1-D)^2}\left(\dfrac{r_L}{r_l}\right)+\dfrac{V_d(M-1+D)}{V_{DC}[1+(M-1)D]}+1\right]\left[\dfrac{Nr_c}{Nr_c+Nr_{on}+r_l}+\dfrac{Nr_{on}}{Nr_c+Nr_{on}+r_l}+1\right]}$

above specifications, the theoretical value of the DC link voltage, V_b is *24.75V*. Similarly, the maximum output voltage of the SC circuit is *74.25V*. The total blocking voltage of the inverter is *445.5V*.

A. Simulation Study

Simulation studies for the proposed topology are performed using MATLAB/Simulink. With the above mentioned specifications, the simulated DC link voltage, V_b is *23V* as shown in Fig. 7(a). The switched capacitor voltage (V_{C1}) is presented in Fig. 7(b). It can be observed that V_{C1} is equal to *22.5V*. Similarly, the simulated V_{C2} is equal to *21.5 V*. The output voltage of the inverter is shown in Fig. 7(c). It can be observed that the output voltage has 7 levels. The different voltage levels are (*66.5V*, *44V*, *21.5V, 0, -21.5V, -44V, -66.5V*). The simulation result values are a little less than the theoretical values due to voltage drops of the diodes and switching devices. The simulation has been performed considering that the forward voltage drop for the diode is *0.7V* and that the internal on state resistance of the MOSFET is *0.1Ω*. The load current is presented in Fig. 7(d). It can be observed that the load current is sinusoidal due to the inductive nature of the load. The stress voltage for S_{H1} is shown in Fig. 8(a). Similarly, the stress voltages for the other switching devices are observed and the total simulated blocking voltage of the inverter is evaluated, which is equal to *411V*. A FFT analysis of the load voltage is shown in Fig. 8(b). The peak amplitude of the fundamental component (*50Hz*) and the THD for the load voltage are *66.32V* and *18.19%*, respectively. Similarly, the peak amplitude of the fundamental component and THD for the load current are evaluated and equal to *0.66A* and *6.28%*, respectively. The variation of the THD of the load voltage with respect to different values of m_a and D is shown in Fig. 8(c). With same fundamental output voltage, the THD of the load voltage is evaluated for each values of m_a. For maintaining the same fundamental voltage, when m_a decreases, D as well as the boosting factor of the L-ZSI circuit of the inverter increases. From this study, it has been observed that as m_a decreases the THD value of the load voltage increases. Further, this study has been done considering three different values for the voltage levels. The levels are 7 levels, 9 levels and 11 levels. It can be concluded that as the levels of the inverter increase under the same fundamental voltage, the THD of the output voltage decreases. Thus, by increasing the levels of the inverter, the THD of the inverter can be controlled within limits. For maintaining the same fundamental voltage at the output, different input voltage values are considered for different levels of the inverter. The values of V_{DC} are *16.5V*, *13.2V* and *11.4 V* for 7 levels, 9 levels and 11 levels with the proposed inverter, respectively. A similar study has been done for the load current under the same load conditions. Fig. 8(d) shows the variation of the load current THD against different values of m_a and D considering the same fundamental load current.

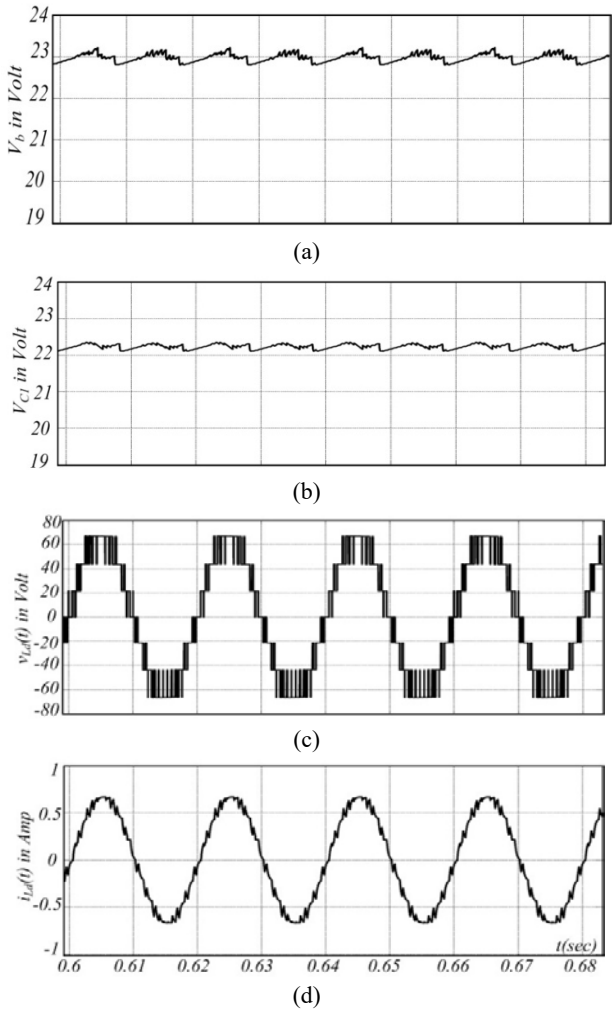

Fig. 7. Simulation results for: (a) the DC link voltage, V_b; (b) the SC (*C1*) voltage, V_{C1}; (c) the output voltage, *vLd(t)*; (d) the load current, $i_{Ld}(t)$.

B. Experimental Study

For experimental investigation of the proposed topology, a laboratory prototype has been developed. MOSFET (IRF840) is used as a switching device. The inductors are designed at L_1=*2.77mH* (and L_2=*2.81mH*) and fabricated for *3A*. Different switching pulses are generated by an ATmega328 microcontroller. The experiment set-up is shown in Fig. 9(a). Fig. 9(b) presents the input DC voltage, V_{DC}=*16.5V* (average).

The DC link voltage V_b is shown in Fig. 9(c) and it is equal to *24V*. The output voltage has 7 levels and the levels are (*65.5V, 43V, 22V, 0, -22V, -43V, -65.5V*) as shown in Fig. 9(d). Fig. 10(a) presents the load current with respect to the load voltage. It can be observed that the load current is sinusoidal and lagging the load voltage due to the inductive nature of the load. The switched capacitor voltages are shown in Fig. 10(b) and 10(c). The capacitor voltages are V_{C1}=*23V* and V_{C2}=*21V*. The voltage difference between the capacitor voltages is due to the voltage drops in the diode (D2) and

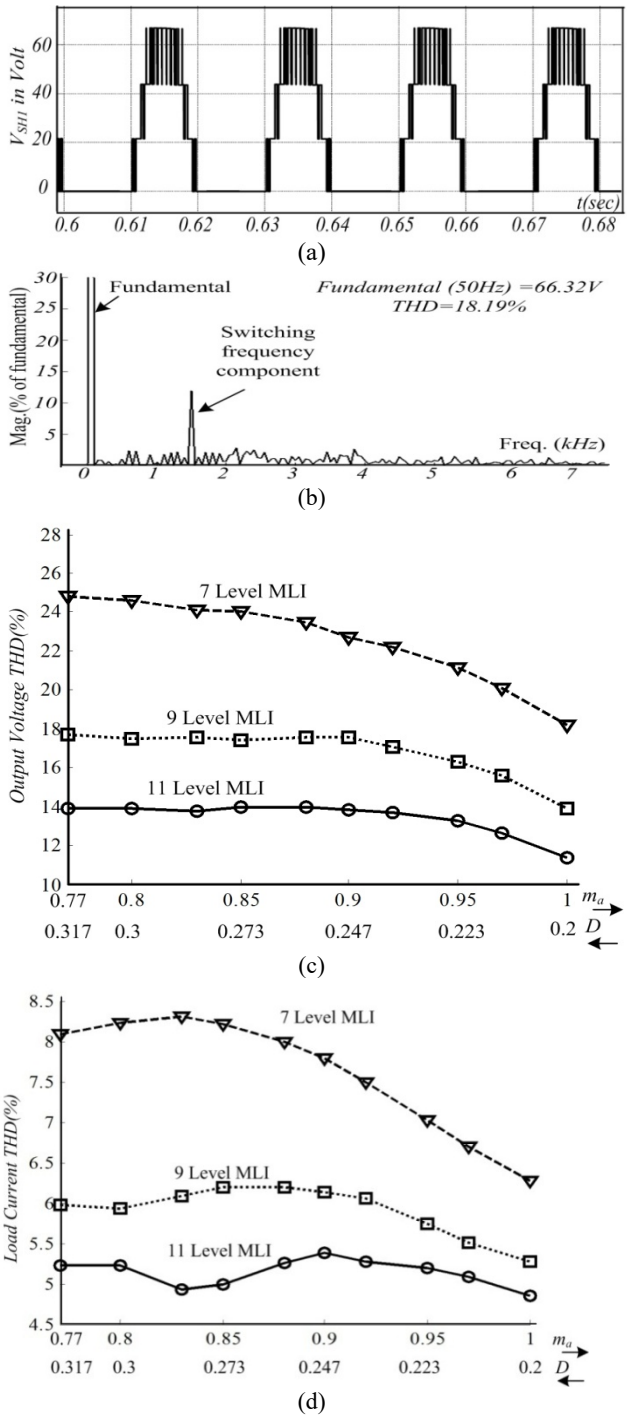

Fig. 8. Results for: (a) the simulated stress voltage across SH1; (b) the FFT analysis of the simulated output voltage; (c) the output voltage THD(%) for different values of ma and D; (d) the output current THD(%) for different values of ma and D.

wire resistance. Further, C_2 is greater than C_1. Thus, the charging current for C_2 is more than that for C_1. In addition, the discharging time for C_2 is more than that for C_1. Hence, the drop is more in the voltage of C_2. By a proper practical set up design, the voltage difference between the capacitor voltages can be reduced. It is observed that with the specified switching, the capacitor voltages are balanced. The stress

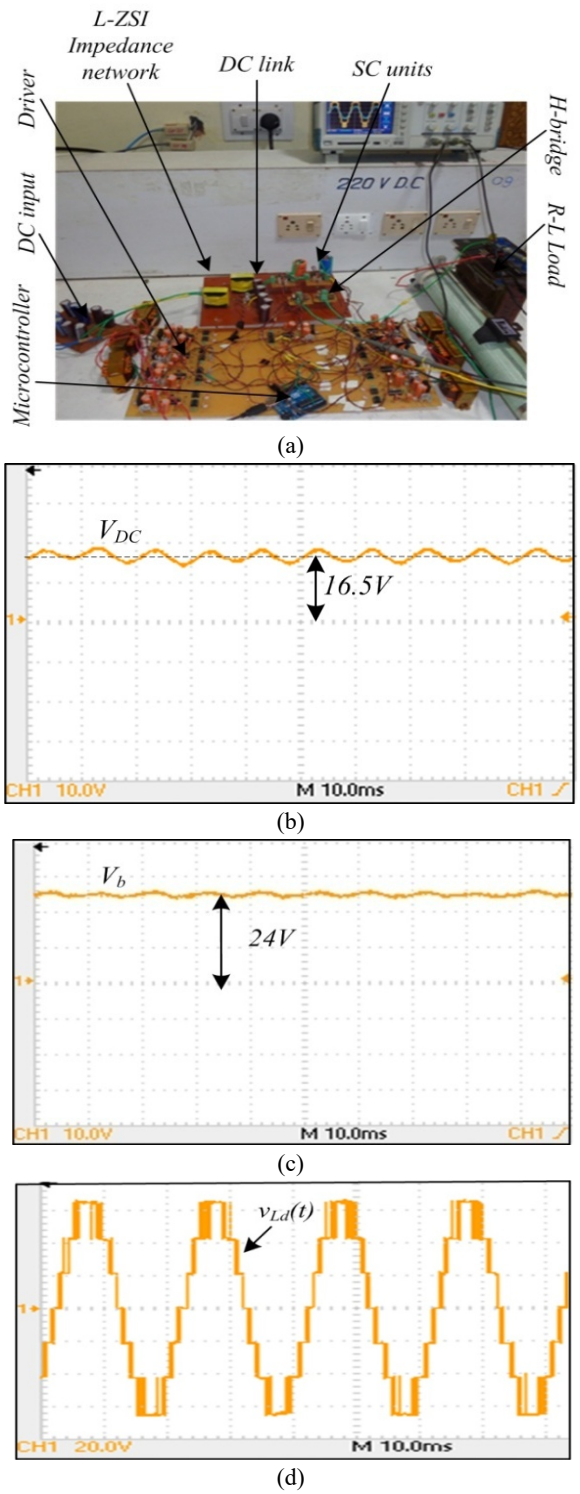

Fig. 9. Results for: (a) the experimental set-up; (b) the input DC voltage, V_{DC}; (c) the boosted DC link voltage, V_b; (d) the output load voltage, $v_{Ld}(t)$.

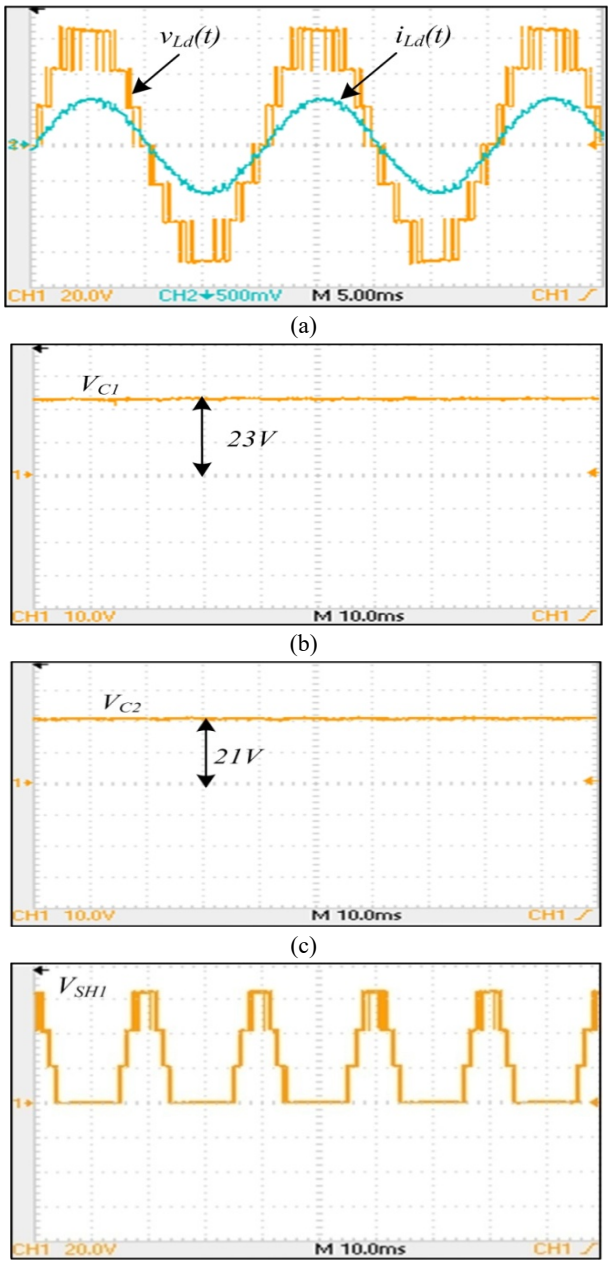

Fig. 10. Experimental results for: (a) the load voltage, $v_{Ld}(t)$ and load current, $i_{Ld}(t)$; (b) the switched capacitor (C_1) voltage, V_{C1}; (c) the switched capacitor(C_2) voltage, V_{C2}; (d) the stress voltage across S_{H1}.

voltage across S_{H1} is presented in Fig 10(d). Similarly, the stress voltages for the other switches have been observed. The total experimental blocking voltage of the inverter is *401V*. The FFT analysis of the experimental data for the load voltage and load current are presented in Fig. 11(a) and 1 1 (b), respectively. The peak amplitude of the fundamental (*50Hz*) component and THD of the load voltage are 64.82V and 20.1%, respectively. Similarly, the peak amplitude of the fundamental component and THD for the load current are 0.6269A and 6.511%, respectively. Fig. 11(c) presents the variation of the THD of the load voltage with different values of m_a and D for the same output fundamental voltage (*64.82V*) for the 7 level proposed MLI. It is observed that the THD of the load voltage increases with lower values of the modulation indices. A similar study has been carried out for

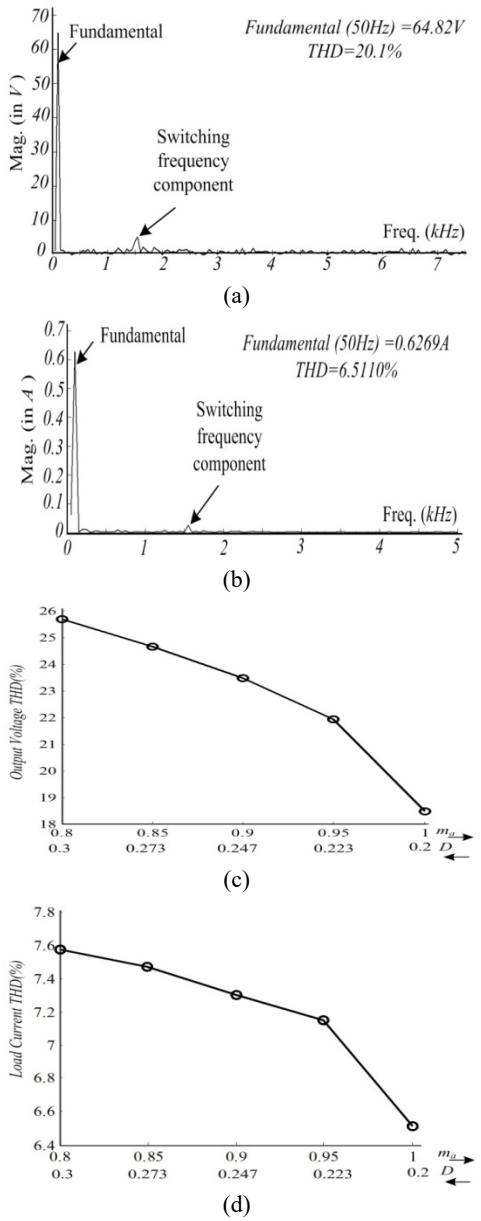

Fig. 11. Results for: (a) a FFT analysis on the experimental data for the load voltage; (b) a FFT analysis on the experimental data for the load current; (c) the experimental output voltage THD(%) for different modulation indexes (for 7 level MLI); (d) experimental output current THD(%) for different modulation indexes (for 7 level MLI).

load current under the same load condition (*100*Ω*, 25mH*) as shown in Fig. 11(d). Thus, it can be concluded that the experimental results are well matched with both the theoretical and simulation results.

VII. CONCLUSION

In this paper, a new single phase multilevel inverter topology has been presented. The proposed topology is developed based on the L-ZSI impedance network and switched capacitor basic units. A detailed analysis and general expressions for the parameters of the topology have been presented. Further, a comparison study between the proposed topology and other recently developed topologies has been discussed in detail. It has been observed that the topology can boost the input voltage in two-steps and that the boosting factor can be controlled by varying a larger number of variables which provides more flexibility for selecting the size, cost and complexity of the inverter. A multicarrier phase disposition PWM technique has been developed to switch the inverter. A 7-level output voltage inverter structure is successfully simulated and experimentally tested. The presented topology is suitable for renewable energy conversion systems and medium voltage high power applications since the blocking voltage of the inverter increases with the boosting factor. From an application point of view, the presented topology can be applied to single phase induction motor drive systems, water pumping systems, and air conditioning systems [26].

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