JPE 17-6-17

https://doi.org/10.6113/JPE.2017.17.6.1563
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Study on a Novel Switching Pattern Current Control Scheme Applied to Three-Phase Voltage-Source Converters

Hongyan Zhao*, Yan Li†, and Trillion Q. Zheng*

*,†School of Electrical Engineering, Beijing Jiaotong University, Beijing, China

Abstract

This paper presents a novel switching pattern current control (SP-CC) scheme, which is applied in three-phase voltage-source converters (VSCs). This scheme can select the optimal output switching pattern (SP) by referring the basic principle of space vector modulation (SVM). Moreover, SP-CC is a method without a carrier wave. Thus, the implementation process is concise and easy. When compared with the conventional hysteresis current control (C-HCC) and the space vector-based hysteresis current control (SV-HCC), the SP-CC has the performances of faster dynamic response of C-HCC and less switching number (SN) of SV-HCC. In addition, it has less harmonic contents in the three-phase current, along with a lower switching loss and a higher efficiency. Moreover, the hysteresis bandwidth and Clarke conversion are not required in the SP-CC. The effectiveness of the presented SP-CC is verified by simulation and experimental test results. In addition, the advantages of the SP-CC, when compared with the C-HCC and SV-HCC, are verified as well.

Key words: Hysteresis current control (HCC), Switching number (SN), Switching pattern current control (SP-CC), Voltage-source converter (VSC)

I. INTRODUCTION

Nowadays, the three-phase voltage-source converter (VSC) is widely applied in electric drive and power systems, e.g. active power filters (APF), uninterrupted power supplies (UPS), etc. Moreover, the VSC has become increasingly important in the application of large-scale distributed power generation systems, such as solar energy, wind energy, and so on [1]-[5]. Dual-loop control is often used in VSCs to achieve a bidirectional power flow, an accurate tracking performance and a convenient debugging process [6], [7]. The major function of an inner-loop current controller is, by referring to the output reference current of the out-loop controller, controlling the AC current to realize a unit power factor of the VSC. Normally, the higher the switching frequency is, the lower the current THD is, while the switching loss increases correspondingly. Hence, improving the current tracking performance and reducing the switching loss are the main targets of inner-loop current controllers.

In terms of switching features, there are two types of current controllers for the VSC. One type is called the classical on-off controller (COFC), which can be implemented by retrieving switching tables [8], optimizing switching cost functions [9], comparing the hysteresis bandwidth [10], etc. The COFC changes the switching states at the end of each control period, which normally results in an unfixed switching frequency. The other type is the pulse width modulation (PWM) controller, which includes the duty-cycle controller [11], [12], one-cycle controller [13]-[17], space vector modulation controller [18], [19], etc. Generally speaking, the PWM controller is implemented by comparing a modulation wave with a triangle carrier wave. Hence, the switching frequency/period of the PWM controller is equal to the frequency/period of the triangle carrier wave, and the switching duty-cycle of each phase keeps changing in every switching period. The PWM controller usually has a good current performance [11]-[19]. However, due to the calculation time of the controller, the time-delay should be considered. Therefore, the PWM controller is difficult to

Manuscript received Sep. 4, 2016; accepted Jul. 29, 2017
Recommended for publication by Associate Editor Sangshin Kwak.
†Corresponding Author: liyan@bjtu.edu.cn
Tel: +86-010-51684911, Beijing Jiaotong University
*School of Electrical Engineering, Beijing Jiaotong University, China

apply in high switching frequency conditions. In addition, it also requires complicated hardware or software, such as a high speed digital processor, etc. As a result, the real-time performance of a PWM controller is worse than that of a COFC in high switching frequency applications.

With COFC, the hysteresis current control (HCC) is the most mature and simplest control scheme [10]. However, the switching frequency of the HCC may be extremely high, especially at the zero crossing point, due to the lacking of coordination among the three-phase hysteresis comparators [20], [21]. Therefore, the work that studies an advanced HCCs-based scheme, which can maintain the advantages and eliminate the drawbacks of the conventional HCC (C-HCC) in various applications, has great significance and value [22]-[26]. For example, in order to reduce the switching frequency/switching number (SN) and current harmonic contents, the space vector-based HCC (SV-HCC) was presented in [20], [21], [27]-[31]. In the SV-HCC, a comparator of the AC current error is used in the α-β frame or the *a*-*b*-*c* frame, and a two or three level hysteresis band is also used. In addition, a switching table or logical calculation is also applied in the SV-HCC. With the SV-HCC, it should be noted that although the SN can be reduced significantly, the selected switching pattern (SP) may not be the optimal, because the most suitable hysteresis band is difficult to set. Moreover, a big current error may emerge in the dynamic process in the SV-HCC.

This paper presents a novel switching pattern current controller (SP-CC) which can be classified as a COFC. The basic principle of the presented SP-CC is to find the voltage vector $\overrightarrow{V_{\text{aim}}}$ that is closest to the reference voltage vector $\overrightarrow{V^*}$ in each control period. Obviously, it is similar to the process of finding the SP that spends the most time during one control period in the space vector modulation (SVM). Then the SP that $\overrightarrow{V_{\text{aim}}}$ corresponds to is selected. Moreover, the SP-CC does not need a hysteresis band, a retrieving switching table and a Clarke or Park transformation. In spite of this, it can obtain the optimal SP with a fast dynamic response. Finally, when compared with the C-HCC and SV-HCC, simulation and experiment results illustrate that the SP-CC can possess a lower current THD and a higher efficiency.

II. Space Vector Model of Three-Phase VSC

The topology of a three-phase VSC is shown in Fig. 1, where e_n (n=*a, b, c*) is the three-phase voltage, i_n is the three-phase current, v_{dc} is the DC bus voltage, L is the AC filter inductance, R_L is the DC load, and s_n is the three-phase power switch. In the n-phase, s_n=0 means the under bridge arms switch on and the upper bridge arms switch off. Conversely, s_n=1 means the opposite. In addition, v_{no} represents the voltage between point 'n' and point 'o'. According to Kirchhoff voltage law, v_{no} can be got as (1).

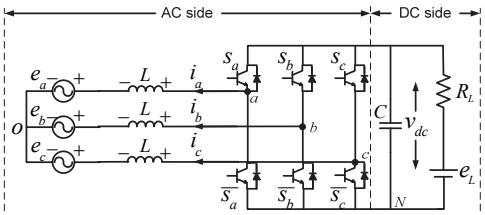


Fig. 1. Topology of a three-phase VSC.

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} v_{dc} + \begin{bmatrix} v_{No} \\ v_{No} \\ v_{No} \end{bmatrix}. \tag{1}$$

Given that the balanced three-phase system satisfies $e_a+e_b+e_c=0$ and $i_a+i_b+i_c=0$, it is possible to obtain $v_{ao}+v_{bo}+v_{co}=0$. Then getting the sum on both sides of equation (1) and letting $v_{ao}+v_{bo}+v_{co}=0$ in the sum, it is found that:

$$v_{No} = -\frac{v_{dc}}{3} \sum_{n=a,b,c} s_n. \tag{2}$$

Therefore, substituting (2) into (1) yields:

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} v_{dc}. \tag{3}$$

Obviously, it can be found from (3) that v_{no} is decided by the SP (s_a s_b s_c). In addition, v_{no} can be expressed out by a space voltage vector whose amplitude is $2v_{dc}/3$ in the complex plane. In addition, due to the limited SP combinations (2^3=8) of the power switches, there are only 8 space voltage vectors, which can be defined as $\overrightarrow{V_k}$ (k=0~7) in the complex plane, i.e.:

$$\begin{cases} \overrightarrow{V_k} = \dfrac{2}{3} v_{dc} \cdot exp(jk\pi/3), \text{ when } k = (1,\cdots,6) \\ \overrightarrow{V_{0,7}} = 0 \end{cases}. \tag{4}$$

Furthermore, for interpretation, the relationship between SP (s_a s_b s_c) and the voltage vector $\overrightarrow{V_k}$ is given in Fig. 2(a).

In balanced three-phase system, three-phase symmetrical variable x_n (including e_n, i_n, v_{Ln}, v_{no}, etc.) can combine into a rotating space vector $\vec{X}$ (corresponds to $\vec{E}$, $\vec{I}$, $\overrightarrow{V_L}$ and $\vec{V}$, respectively). In addition, $\vec{X}$ can be expressed as:

$$\vec{X} = x_a + x_b exp(j2\pi/3) + x_c exp(j4\pi/3). \tag{5}$$

For the sake of the analysis below, as shown in Fig. 1, the reference direction of the current i_n is defined from the DC-side to the AC-side. According to Kirchhoff voltage law, the inductance voltage $\overrightarrow{V_L}$ can be obtained as:

$$\overrightarrow{V_L} = Ld\vec{I}/dt = \vec{V} - \vec{E} \tag{6}$$

where $\vec{E}$ is the rotating voltage vector of the three-phase voltage, $\vec{I}$ is the rotating current vector of the three-phase AC current, and $\vec{V}$ is the rotating voltage vector of the voltage between point 'n' and point 'o'.

From the analysis presented earlier, it is known that, at

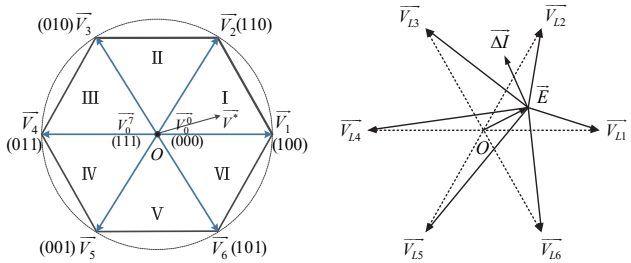


Fig. 2. Distribution of: (a) $\vec{V}_k$; and (b) $\vec{V}_{Lk}$ and $\Delta\vec{I}$.

any time, the voltage vector $\vec{V}$ only corresponds to a specific $\vec{V}_k$ among the 8 space voltage vectors in Fig. 2(a). Therefore, letting $\vec{V}=\vec{V}_k$ in (6), there are 8 inductance voltage vectors that can be obtained, which can be expressed as:

$$\vec{V}_{Lk}=Ld\vec{I}/dt=\vec{V}_k-\vec{E}. \tag{7}$$

In addition, the current error vector $\Delta\vec{I}$ is defined as $\Delta\vec{I}=\vec{I}^*-\vec{I}$, and $\vec{I}^*$ is the reference AC current vector. In order to make $\vec{I}$ trace $\vec{I}^*$, $d\vec{I}/dt$ should be as close to the direction of $\Delta\vec{I}$ as possible. It is equivalent to choose a SP which meets the condition of making sure that $\vec{V}_{Lk}$ has the minimum phase angle with $\Delta\vec{I}$, as shown in Fig. 2(b).

However, the angular conversion and derivation processes are difficult to implement in a digital processor. Hence, by substituting $\Delta\vec{I}/T$ into (6) to replace $d\vec{I}/dt$, the desired output voltage vector $\vec{V}^*$ ($\vec{V}^*=v_{ao}^*+v_{bo}^*e^{j2\pi/3}+v_{co}^*e^{j4\pi/3}$, where v^*_{no} is the desired output voltage between point '*n*' and point '*o*') which corresponds to $\vec{V}$, can be obtained as:

$$\vec{V}^*=L\Delta\vec{I}/T+\vec{E} \tag{8}$$

where T is the digital control period.

From the analysis presented above, it is apparent that there is a linear relationship between $\vec{V}_{Lk}$ and $\Delta\vec{I}$. Therefore, as expected, choosing $\vec{V}_{Lk}$, which has the minimum angle with $\Delta\vec{I}$, is translated into choosing the closest $\vec{V}_k$ to $\vec{V}^*$.

III. Principle of the Presented SP-CC

In SVM [18]-[19], the desired output voltage vector $\vec{V}^*$ can be synthesized by the adjacent vectors $\vec{V}_i$ and $\vec{V}_j$ (which represent the right and left voltage vectors of $\vec{V}^*$ in SVM, respectively) as well as the zero vector $\vec{V}_z$ ($\vec{V}_0$ or $\vec{V}_7$). Therefore, the synthesizing method of $\vec{V}^*$ in SVM can be illustrated as:

$$T_i\vec{V}_i+T_j\vec{V}_j+T_0\vec{V}_z=T\vec{V}^* \tag{9}$$

where T_i, T_j and T_0 represent the consumed time of $\vec{V}_i$, $\vec{V}_j$ and $\vec{V}_z$, respectively.

In addition, substituting v^*_{no} and the desired SP (s_a^* s_b^* s_c^*) into (3) yields:

$$\begin{bmatrix}v_{ao}^*\\ v_{bo}^*\\ v_{co}^*\end{bmatrix}=\begin{bmatrix}2/3 & -1/3 & -1/3\\ -1/3 & 2/3 & -1/3\\ -1/3 & -1/3 & 2/3\end{bmatrix}\begin{bmatrix}s_a^*\\ s_b^*\\ s_c^*\end{bmatrix}v_{dc}. \tag{10}$$

Assume that $\vec{V}^*$ is located in sector I in Fig. 2(a). Then according to the principle of SVM, $\vec{V}_1$ and $\vec{V}_2$ should be selected as $\vec{V}_i$ and $\vec{V}_j$, respectively. Therefore, the desired SP (s_a^* s_b^* s_c^*) can be synthesized by (100) and (110), while (s_a^* s_b^* s_c^*) can be obtained by submitting $\vec{V}_1$ (100) and $\vec{V}_2$ (110) into (9), i.e.:

$$T_i\begin{bmatrix}s_a^*\\ s_b^*\\ s_c^*\end{bmatrix}=T_i\begin{bmatrix}1\\0\\0\end{bmatrix}+T_j\begin{bmatrix}1\\1\\0\end{bmatrix}. \tag{11}$$

Furthermore, substituting (11) into (10) yields:

$$\begin{cases}T_i=\dfrac{v_{ao}^*-v_{bo}^*}{v_{dc}}T\\ T_j=\dfrac{v_{bo}^*-v_{co}^*}{v_{dc}}T\end{cases}. \tag{12}$$

In addition, substituting (12) into equation T_0=T-T_i-T_j yields:

$$T_0=(1-\frac{v_{ao}^*-v_{co}^*}{v_{dc}})T. \tag{13}$$

Similarly, the solution procedure of T_i, T_j and T_0 when $\vec{V}^*$ is located in sector I is also applicable to the condition of $\vec{V}^*$ located in the other sectors in SVM.

Essentially, to the presented SP-CC, the target of choosing an optimal SP is tantamount to choosing a SP that consumes the largest time in one control period T in SVM. For example, if $T_0\geq T_i$ and $T_0\geq T_j$ are both satisfied, the zero-SP (ZSP) is selected in the SP-CC. Furthermore, according to (12), (13) and $T_0\geq T_i$, $T_0\geq T_j$, when $\vec{V}^*$ is located in sector I, the judgment condition of the ZSP selection in the SP-CC is given in (14).

$$\begin{cases}(1-\dfrac{v_{ao}^*-v_{co}^*}{v_{dc}})>\dfrac{v_{ao}^*-v_{bo}^*}{v_{dc}}\\ (1-\dfrac{v_{ao}^*-v_{co}^*}{v_{dc}})>\dfrac{v_{bo}^*-v_{co}^*}{v_{dc}}\end{cases}. \tag{14}$$

The balanced three-phase system satisfies $v_{ao}^*+v_{bo}^*+v_{co}^*=0$. Therefore, for the sake of simplicity, substituting this equation into (14), the judgment condition of the ZSP selection when $\vec{V}^*$ is located in sector I in the SP-CC becomes:

$$v_{ao}^*<\frac{1}{3}v_{dc} \text{ and } v_{co}^*>-\frac{1}{3}v_{dc}. \tag{15}$$

Notice that the necessary condition of $\vec{V}^*$ located in sector I is $v_{ao}^*>v_{bo}^*>v_{co}^*$. Hence, for a more accurate judgment, (15) should be further equivalently transformed into the

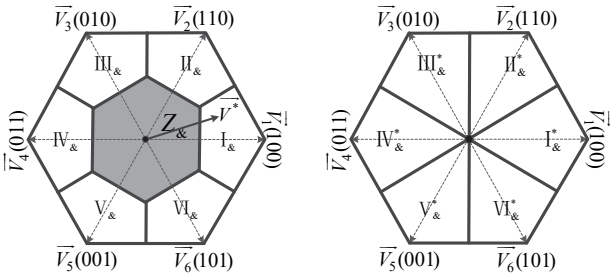


Fig. 3. Regions of: (a) $\vec{V}^*$, and (b) $\vec{I}$ located in the SP-CC.

inequation (16), i.e.:

$$\begin{cases} -\frac{1}{3}v_{dc} < v_{ao}^* < \frac{1}{3}v_{dc} \\ -\frac{1}{3}v_{dc} < v_{bo}^* < \frac{1}{3}v_{dc} \\ -\frac{1}{3}v_{dc} < v_{co}^* < \frac{1}{3}v_{dc} \end{cases}. \tag{16}$$

Similarly, when $\vec{V}^*$ is located in the other five sectors, (16) is also the criteria to decide whether to use the ZSP or not. Therefore, it does not need to detect the sector that $\vec{V}^*$ is located in when the ZSP is selected. In other words, if $\vec{V}^*$ is located in the gray hexagon region $Z_{\&}$ in Fig. 3(a), the ZSP should undoubtedly be selected.

However, if (16) is not satisfied, the non-zero switching pattern (N-ZSP) should be selected. In addition, there are six regions (regions $I_{\&}$ to $VI_{\&}$, do not include $Z_{\&}$) which need a different N-ZSP in the SP-CC, as shown in Fig. 3(a). For interpretation, assume that $v^*_{ao} \geq 0$, $v^*_{bo} \leq 0$ and $v^*_{co} \leq 0$. Then $\vec{V}^*$ is located in region $I_{\&}$, and $\vec{V}_1$ is the closest voltage vector to $\vec{V}^*$. Therefore, the SP (100) should be selected.

It is obviously that, the conditions of the other five regions are similar to region $I_{\&}$. As a result, no matter which region $\vec{V}^*$ is located in, the judgment condition of N-ZSP selection can be summarized as:

$$\begin{cases} s_n = 1, & \text{when } v_{no}^* \geq 0 \\ s_n = 0, & \text{when } v_{no}^* < 0 \end{cases}. \tag{17}$$

Finally, the selection principles of the SP (including the ZSP and the N-ZSP) are given in Table I.

IV. Implementation of the Presented SP-CC

Based on the principle of the SP-CC depicted in section III, the implementation is supplied in this section.

First of all, (18) can be derived from (6), i.e.:

$$\begin{bmatrix} v_{ao}^* \\ v_{bo}^* \\ v_{co}^* \end{bmatrix} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} + \frac{L}{T}\begin{bmatrix} i_a^* - i_a \\ i_b^* - i_b \\ i_c^* - i_c \end{bmatrix}. \tag{18}$$

In addition, according to the application scenarios of the VSC, in steady-state, the phase difference between the three-phase current and the three-phase voltage is always 0° or 180°. Therefore, the three-phase reference current i_n^* can be written as:

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = M\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{19}$$

where M indicates the magnitude ratio of i_n^* to e_n, i.e., $M = i_n^* / e_n$. Therefore, (18) can be further manipulated by substituting (19) into (18), i.e.:

$$\begin{bmatrix} v_{ao}^* \\ v_{bo}^* \\ v_{co}^* \end{bmatrix} = (\frac{L}{T}M + 1)\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} - \frac{L}{T}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \tag{20}$$

To further simplify the control scheme and the implementation algorithm of the presented SP-CC, three variables r_n are proposed as:

TABLE I
Switching Pattern Selection Principle of the Presented SP-CC

First precondition	Second precondition	Region of $\vec{V}^*$ locates	Switching pattern SP
$-\frac{1}{3}v_{dc} < v_{ao}^* < \frac{1}{3}v_{dc}$ and $-\frac{1}{3}v_{dc} < v_{bo}^* < \frac{1}{3}v_{dc}$ and $-\frac{1}{3}v_{dc} < v_{co}^* < \frac{1}{3}v_{dc}$ are not satisfied	$v_{ao}^* \geq 0$, $v_{bo}^* \leq 0$, $v_{co}^* \leq 0$	$I_{\&}$	(100)
	$v_{ao}^* \geq 0$, $v_{bo}^* \geq 0$, $v_{co}^* \leq 0$	$II_{\&}$	(110)
	$v_{ao}^* \leq 0$, $v_{bo}^* \geq 0$, $v_{co}^* \leq 0$	$III_{\&}$	(010)
	$v_{ao}^* \leq 0$, $v_{bo}^* \geq 0$, $v_{co}^* \geq 0$	$IV_{\&}$	(011)
	$v_{ao}^* \leq 0$, $v_{bo}^* \leq 0$, $v_{co}^* \geq 0$	$V_{\&}$	(001)
	$v_{ao}^* \geq 0$, $v_{bo}^* \leq 0$, $v_{co}^* \geq 0$	$VI_{\&}$	(101)
$-\frac{1}{3}v_{dc} < v_{ao}^* < \frac{1}{3}v_{dc}$ and $-\frac{1}{3}v_{dc} < v_{bo}^* < \frac{1}{3}v_{dc}$ and $-\frac{1}{3}v_{dc} < v_{co}^* < \frac{1}{3}v_{dc}$ are satisfied	The last SP is (000) or (100) or (010) or (001)	$Z_{\&}$	(000)
	The last SP is (111) or (011) or (101) or (110)	$Z_{\&}$	(111)

$$\begin{bmatrix} r_a \\ r_b \\ r_c \end{bmatrix} = \frac{T}{L}\begin{bmatrix} v_{ao}^* \\ v_{bo}^* \\ v_{co}^* \end{bmatrix} = (M + \frac{T}{L})\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} - \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \quad (21)$$

According to (21), by substituting r_n into (16), the equation that decides whether or not the ZSP is selected can be further equivalently manipulated into (22), i.e.:

$$\begin{bmatrix} -\frac{T}{3L}v_{dc} \\ -\frac{T}{3L}v_{dc} \\ -\frac{T}{3L}v_{dc} \end{bmatrix} < \begin{bmatrix} r_a \\ r_b \\ r_c \end{bmatrix} < \begin{bmatrix} \frac{T}{3L}v_{dc} \\ \frac{T}{3L}v_{dc} \\ \frac{T}{3L}v_{dc} \end{bmatrix}. \quad (22)$$

Moreover, to further simplify the judgment condition of the ZSP or N-ZSP selection, some binary variables (B_{nx} and B_{ny}) are proposed as:

$$\begin{cases} B_{nx} = 0, & \text{when } r_n \geq (T/3L)v_{dc} \\ B_{nx} = 1, & \text{when } r_n < (T/3L)v_{dc} \\ B_{ny} = 0, & \text{when } r_n \leq -(T/3L)v_{dc} \\ B_{ny} = 1, & \text{when } r_n > -(T/3L)v_{dc} \end{cases}. \quad (23)$$

As a result, the final judgment condition that determines whether the ZSP or N-ZSP is selected can be obtained from (22) and (23), i.e.:

$$\begin{cases} B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy} = 1 \rightarrow \text{ZSP} \\ B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy} = 0 \rightarrow \text{N-ZSP} \end{cases}. \quad (24)$$

On the one hand, when the ZSP is selected, which of the two zero switching patterns (000) or (111) is eventually applied is determined by the following expression:

$$(s_a^{\wedge} + s_b^{\wedge})(s_b^{\wedge} + s_c^{\wedge})(s_a^{\wedge} + s_c^{\wedge}) \quad (25)$$

where $s_n^{\wedge}$ is the switching state of the last control period of the n-phase. If the solution of expression (25) is 0, this means that the SP of the last control period is (000), (001), (010) or (100), so that SP (000) should be applied in this control period. However, if the solution of expression (25) is 1, this means that the SP of the last control period is (111), (110), (101) or (011), so that SP (111) should be applied in this control period. In this way, the switch state of at most one phase is changed when the SP changes in each control period. Therefore, both the SN and the switch noise can be significantly reduced, and the switching loss is also reduced.

On the other hand, when the N-ZSP is selected, the selection principle of the SP is described below. First of all, a binary variable B_{no} is defined, which can be expressed in the form of:

$$\begin{cases} B_{no} = 1, & \text{when } r_n \geq 0 \\ B_{no} = 0, & \text{when } r_n < 0 \end{cases}. \quad (26)$$

According to (17), (21), (26) and Table I, it is known that B_{no}=1 means s_n=1; and B_{no}=0 means s_n=0.

Through both the theoretical analysis and Table I presented above, a switching table of the presented SP-CC can be obtained, as shown in Table II.

TABLE II
SWITCHING TABLE OF THE PRESENTED SP-CC

First precondition	Second precondition	s_a	s_b	s_c
$B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy} = 0$	$B_{ao} = 1$, $B_{bo} = 0$, $B_{co} = 0$	1	0	0
	$B_{ao} = 1$, $B_{bo} = 1$, $B_{co} = 0$	1	1	0
	$B_{ao} = 0$, $B_{bo} = 1$, $B_{co} = 0$	0	1	0
	$B_{ao} = 0$, $B_{bo} = 1$, $B_{co} = 1$	0	1	1
	$B_{ao} = 0$, $B_{bo} = 0$, $B_{co} = 1$	0	0	1
	$B_{ao} = 1$, $B_{bo} = 0$, $B_{co} = 1$	1	0	1
$B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy} = 1$	$(s_a^{\wedge} + s_b^{\wedge})(s_b^{\wedge} + s_c^{\wedge})(s_a^{\wedge} + s_c^{\wedge}) = 0$	0	0	0
	$(s_a^{\wedge} + s_b^{\wedge})(s_b^{\wedge} + s_c^{\wedge})(s_a^{\wedge} + s_c^{\wedge}) = 1$	1	1	1

As a result, to be more intuitive, the switching signal generation rules of the presented SP-CC method can be summarized as:

$$\begin{aligned} s_a &= (B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy})(s_a^{\wedge} + s_b^{\wedge})(s_b^{\wedge} + s_c^{\wedge})(s_a^{\wedge} + s_c^{\wedge}) \\ &\quad + (\overline{B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy}})B_{ao} \\ s_b &= (B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy})(s_a^{\wedge} + s_b^{\wedge})(s_b^{\wedge} + s_c^{\wedge})(s_a^{\wedge} + s_c^{\wedge}) \\ &\quad + (\overline{B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy}})B_{bo} \\ s_c &= (B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy})(s_a^{\wedge} + s_b^{\wedge})(s_b^{\wedge} + s_c^{\wedge})(s_a^{\wedge} + s_c^{\wedge}) \\ &\quad + (\overline{B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy}})B_{co} \end{aligned} \quad (27)$$

where '^' means the value of last period and '—' means the logical 'NOT'. For example, when $\overrightarrow{V^*}$ is located in region $I_{\&}$, it can be found from table II that $B_{ax}B_{ay}B_{bx}B_{by}B_{cx}B_{cy}$=0 and B_{ao}=1, B_{bo}=0, B_{co}=0. Then the expected SP can be obtained by submitting the results of (23), (25) and (26) into (27), i.e., s_a=1, s_b=0, s_c=0.

To further simplify the presented algorithm, the value of v_{dc} in (22) can be replaced by v_{dc}^* in the steady state of the whole system. Therefore, $v_{dc}^*/3L$ and T/L can be regarded as two constants that are represented by P_1 and P_2, respectively. Recalling (21), it is obvious that r_n can be calculated by Fig. 4(a) in the open-loop control, where M is given. In addition, r_n can be calculated by Fig. 4(b) in the closed-loop control, where M is obtained by the outer-loop controller. Moreover, P_2 is no longer required, as shown in Fig. 4(b), because M can compensate the affection of P_2 in the closed-loop control system.

Generally speaking, the outer-loop controller can be either a proportional integral (PI) regulator [32], a sliding mode controller [33]-[34] or a single-input space vector controller [35], etc., so as to generate the reference current amplitude of the inner-loop [36], [37]. In this paper, a conventional PI regulator is adopted as the outer-loop controller. With the PI regulator, the closed-loop control flows of the C-HCC, the SV-HCC and the presented SP-CC are shown in Fig. 5.

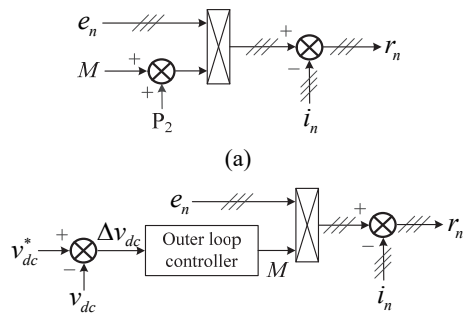


Fig. 4. Calculation process of r_n in: (a) open-loop control; and (b) closed-loop control.

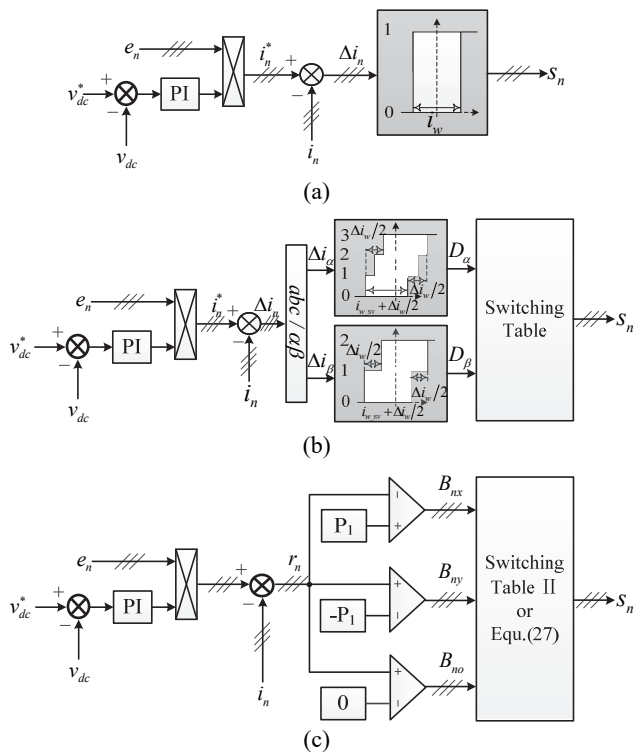


Fig. 5. Closed-loop control of: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.

V. Simulation and Experimental Verification

In this section, the C-HCC, the SV-HCC and the presented SP-CC are verified by simulation and experimental test results. In addition, control performance comparisons among the three methods are also given. The basic specifications of the electrical circuit and control loops in the verification process are summarized in Table III.

A. Simulation Verification

A simulation is carried out by MATLAB/Simulink. In order to obtain a comprehensive comparison among the three related control methods in this paper, four groups of different parameter combinations are adopted in the simulation verification process, as shown in Table IV.

TABLE III
Specifications of Electrical Circuit and Control Loops

Parameters	Simulation	Experiment
Voltage of AC source (peak value)	60 V	60V
Frequency of AC source (f)	50 Hz	50 Hz
Given DC voltage (v^*_{dc})	150 V	200 V
Load of DC-side (R_L)	10 Ω	33Ω
Inductance of AC (L)	2.3 mH	2.3 mH
Capacitance of DC(C)	4700uF	4700uF
K_p and K_i of outer-loop	0.005 and 0.2	0.005 and 0.2

TABLE IV
Four Groups of Simulation Parameter Combinations

Parameters Combination	Control Period	C-HCC	SV-HCC	
	T/μs	i_w/A	i_{w_sv}/A	Δi_w/A
Combination 1	100	0	0	2
Combination 2	100	0.1	0.2	2
Combination 3	25	0	0	0.8
Combination 4	25	0.1	0.2	0.8

The four groups of parameter combinations include different T, different hysteresis bandwidths i_w in the C-HCC, different hysteresis bandwidths i_{w_sv} and bandwidth steps $\Delta i_w/2$ between different-level comparison units in the SV-HCC. Because there is only one time switch action in one T for each switch when HCC-based methods are implemented with digital control, the possible maximum switching frequency is half the digital control frequency. Therefore, the purpose of T is set to 100μs and 50μs is to limit the switching frequency to less than 5 kHz and 20 kHz. In addition, the bandwidth selection relies on the requested control accuracy. A smaller hysteresis bandwidth can get a smaller current tracking error. However, it has a higher switching frequency expense. Therefore, there is always a compromise between the control accuracy and the switching frequency. In parameter combinations 1 and 3, the i_w of C-HCC and the i_{w_sv} of SV-HCC are both set to 0A to get the highest control accuracy under the conditions of T being equal to 100μs and 25μs, respectively. In parameter combinations 2 and 4, the i_w of C-HCC and the i_{w_sv} of SV-HCC are set to 0.1A and 0.2A to make a comparison with the parameter combinations 1 and 3, respectively. The current tracking error in the C-HCC reaches twice the permitted i_w, i.e., $2i_w$ [17]. Therefore, to get a similar control performance with the C-HCC, the i_{w_sv} of SV-HCC is set to twice i_w, i.e., 0.2A in parameter combinations 2 and 4. The function of Δi_w in the SV-HCC is to apply the ZSP systematically to reduce the switching frequency. Because T=100μs in parameter combinations 1 and 2 is relatively large, the Δi_w of SV-HCC is set to 2A. However, due to the small T in parameter combinations 3 and 4, i.e., T=25μs, the Δi_w of SV-HCC is set to 0.8A.

It should be noted that parameter combination 1 is adopted in the simulation processes of Fig. 6 to Fig. 13, and parameter combinations 1 to 4 are adopted in the comparison simulation

processes of the three control methods of Fig. 14 and Fig. 15.

Fig. 6 shows simulation results when the work mode of the VSC changes from inverter to rectifier. In the simulation, a 200V DC source e_L is series to the load R_L at the beginning of the simulation, and it is shorted after 0.1s. Therefore, the VSC works in the inverter mode before 0.1s. Then it changes into the rectifier mode at 0.1s. In addition, the operation power is 1 kW (0.75 kW for grid-connection and 0.25 kW for a DC load R_L) when the VSC works in the inverter mode, and the operation power is 2.25 kW when the VSC works in the rectifier mode. As can be seen in Fig. 6, the three-phase voltage and current are both sinusoidal. Before 0.1s, the phase current has a 180° phase difference with respect to the voltage, which illustrates that the VSC works in inverter mode. As expected, after 0.1 s, the phase difference of the phase current to the three-phase voltage changes from 180° to 0°. This illustrates that the VSC begins to work in the rectifier mode at 0.1s. Meanwhile, at the moment e_L is shorted, the change process of the phase current is relatively smooth. This illustrates that the fault-tolerance of the SP-CC is good even when a large disturbance emerges. In addition, it can be seen from Fig. 6 that the DC voltage v_{dc} can reach the reference 150 V all the time. However, inevitably but reasonably, v_{dc} has an overshoot due to the fact that e_L is shorted at 0.1 s.

Fig. 7 shows the simulation result when two VSCs form a back to back structure. Both of the VSCs are controlled by the presented SP-CC. One VSC (designated as VSC1) works in the rectifier mode and the other (designated as VSC2) works in the grid-connected inverter mode. Therefore, VSC2 can be regarded as a load, or to be more exact, as a nonlinear load of VSC1. The operating power of the back to back system is 1.125kW at the beginning, and it is increased to 2.25kW at 0.1s. Fig. 7 shows waveforms of the DC bus voltage in the back to back system, three-phase voltage and current of VSC1, the three-phase currents of VSC2, the DC bus nonlinear load current, and the grid-connected active and reactive power of VSC2. From these waveforms, it can be seen that when VSC1 is controlled by the SP-CC it has a nonlinear load of VSC2. However, the control performance of the SP-CC is still good, which illustrates that the SP-CC has a good transient response performance.

Fig. 8 shows simulation results when the VSC works in the rectifier mode and has a RL series load. At the beginning, the DC load is only R=10Ω. At 0.08s, the load changes to a RL series load "10Ω+5mH", and at 0.1s, the RL load step changes into "10Ω+100mH". From Fig. 8 it can be seen that the three-phase current changes smoothly and without a big current distortion during the step changing process of the RL load. Moreover, the phase current keeps a synchronous phase angle with the grid voltage all the time, which shows that the VSC controlled by the SP-CC still has a unit power factor when it has a RL series load. However, as can be seen in Fig. 7, at the two RL load step changes, the dynamic processes are

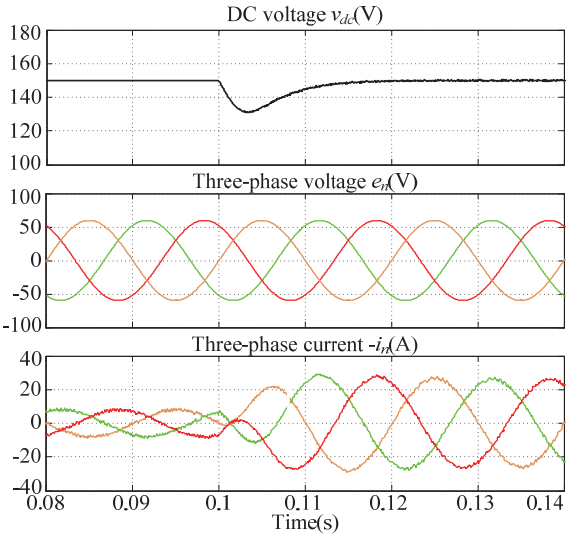


Fig. 6. Waveforms when the three-phase VSC works from the inverter mode to the rectifier mode.

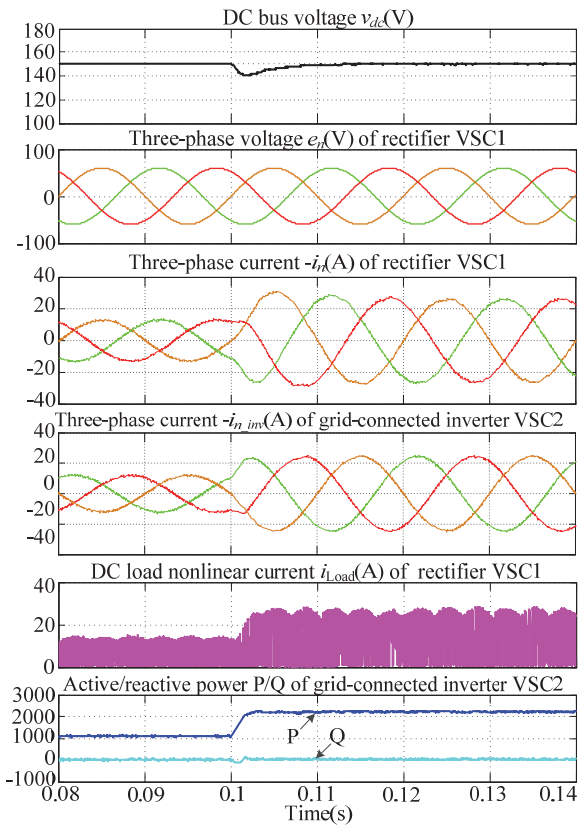


Fig. 7. Waveforms of a three-phase rectifier with a nonlinear grid-connected inverter load.

different. At 0.08s, since the value of the load L is relatively small, i.e., "5mH", the phase current and DC voltage are not seriously affected seriously. However, at the moment of 0.1s, since the value of the load L is relatively big, i.e., "100mH", the phase current and DC voltage are seriously affected and the dynamic adjustment process is long. All of these phenomena are due to the fact that the inductance current

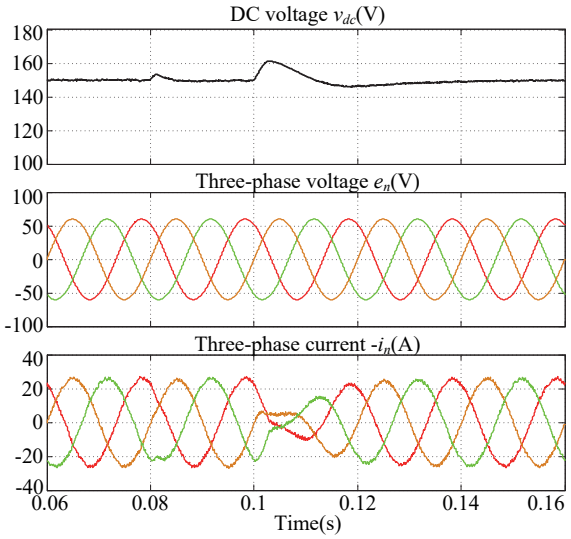


Fig. 8. Waveforms when DC-side RL series load step changes from "10Ω" to "10Ω+5mH", and then to "10Ω+100mH".

cannot change suddenly and that it is equivalent to a piece of wire (or short circuit) in the steady-state in a DC system.

For verifying the advantages of the SP-CC, comparative tests among the C-HCC, SV-HCC and SP-CC are performed.

Fig. 9 shows transient response comparisons of the three methods when the VSC works in the grid-connected inverter mode with a single current control loop. In the simulation process, before 0.1s, the grid-connected active current command value is 12.5A (the grid-connected power is 1.125kW); and at 0.1s, the active current command value changes to 25A (the grid-connected power is 2.25kW). From Fig. 9 it can be seen that the controlled grid-connected current is automatically adjusted with a change of the current command. From the comparison of the three figures in Fig. 9, it is easy to see that the dynamic adjustment processes of the C-HCC, the SV-HCC and the presented SP-CC are almost the same. This illustrates that the transient response performances of the three methods are similar.

The simulation results from Fig. 10 to Fig. 13 are the current control performance comparisons among the three current control methods in this paper. The operation power is 2.25kW. As mentioned before, the parameter combination 1 is adopted in the simulation process of Fig. 10 to Fig. 13. In the parameter combination 1, the hysteresis bandwidths of the C-HCC and SV-HCC are set as: i_w=0 A for C-HCC; and i_w=0 A, Δi_w=2 A for SV-HCC. Due to these settings, both the C-HCC and SV-HCC can achieve a superior AC current control performance for themselves, respectively.

Fig. 10 shows the trajectories of i_α and i_β of the three-phase current of the three methods in the α-βframe. From Fig. 10, it can be seen that the current fluctuation of the C-HCC is much larger than that of the SV-HCC. It can also be seen that the current fluctuation of the SV-HCC is a bit larger than that of the presented SP-CC. Therefore, it turns out that the presented SP-CC has less harmonic contents than the C-HCC and the SV-HCC. In addition, Fig. 11 shows the current tracking error trajectories of the three methods among three fundamental periods in the α-β reference frame. Notice that the C-HCC has a much larger current error range than the SV-HCC and the SP-CC. It can be found that the current error amplitude of the SV-HCC is a bit larger than that of the SP-CC, which is coincides with the simulation results of Fig. 10. It should be noted that both the C-HCC and the SV-HCC can limit the current error in a certain circular area. However, the presented the SP-CC forms a cirque current error trajectory, which is due to the influence of eliminating P_2 in Fig. 4(b) and Fig. 5(c). In addition, it can be seen from the simulation results of Fig. 6 that the modification of eliminating P_2 in Fig. 4(b) and Fig. 5(c) does not impact the control performances in both the AC-side and the DC-side.

Fig. 12 and Fig. 13 show simulation waveforms of the sector number (S_N) of the current vector $\vec{I}$ locates and the selected voltage vector $\overline{V_k}$ of the three methods, respectively. From the simulation results of Fig. 12(a) and Fig. 13(a) it can be seen that the interphases dependency of the C-HCC leads to a large current oscillation (the part in the red line ellipse) and an irregular switching-states changing process. However, in the SV-HCC, the current oscillation can be suppressed evidently and the switching-state changing process is more regular than that of the C-HCC which can be seen in Fig. 12(b) and Fig. 13(b), respectively. However, when compared with the C-HCC and the SV-HCC, the ZVSP-HCC has the smallest current oscillation and a more optimized switching-state changing process. Therefore, the ZVSP-HCC has the highest current control accuracy and the best power quality among the three control methods.

Fig. 14 and Fig. 15 show the SN of the a-phase bridge arm and the instantaneous THD value of the a-phase current i_a of the three current control methods from 0-0.2 s in the simulation process, respectively. As mentioned before, for the purpose of restricting the switching frequency below 5 kHz and 20 kHz, the digital control frequency is set to 10 kHz and 40 kHz in the four parameter combinations, respectively.

In the simulation test, the control frequency is 10 kHz (control period T=100μs), i.e., the situation of the parameter combinations 1 and 2 are adopted, the i_w of C- HCC is set to 0 A and 0.1A, and the i_{w_sv} of SV-HCC is set to 0 A and 0.2 A, respectively. In terms of the SN of the a-phase bridge arms of the three current control methods, as shown in Fig. 14(a) and (b), the SV-HCC and the presented SP-CC can achieve a better reduction than the C-HCC, and the SN of the presented SP-CC is a little less than that of the SV-HCC. In addition, from Fig. 15 (a) and (b), it can be seen that the instantaneous THDs of the a-phase currents i_a of the C-HCC and SV-HCC fluctuate significantly and do not have clear difference between each other. However, the instantaneous THD of the SP-CC is evidently lower than those of the C-HCC and

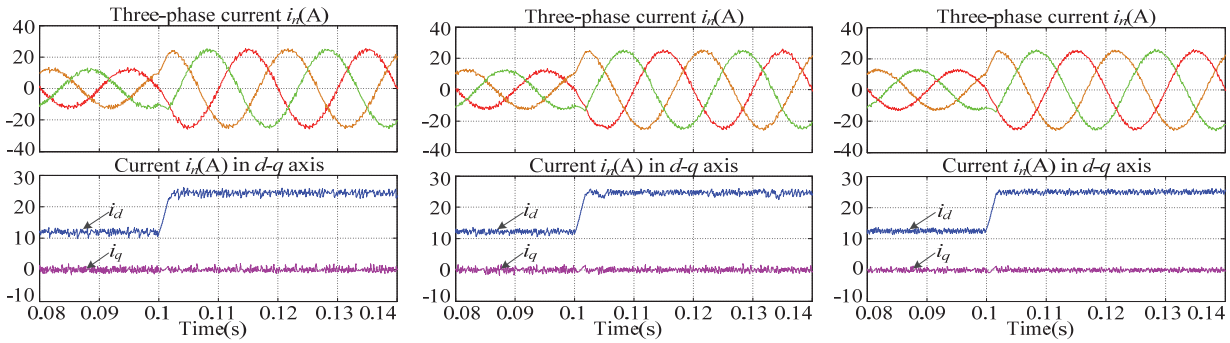


Fig. 9. Transient response of the three methods when current control is adopted: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.

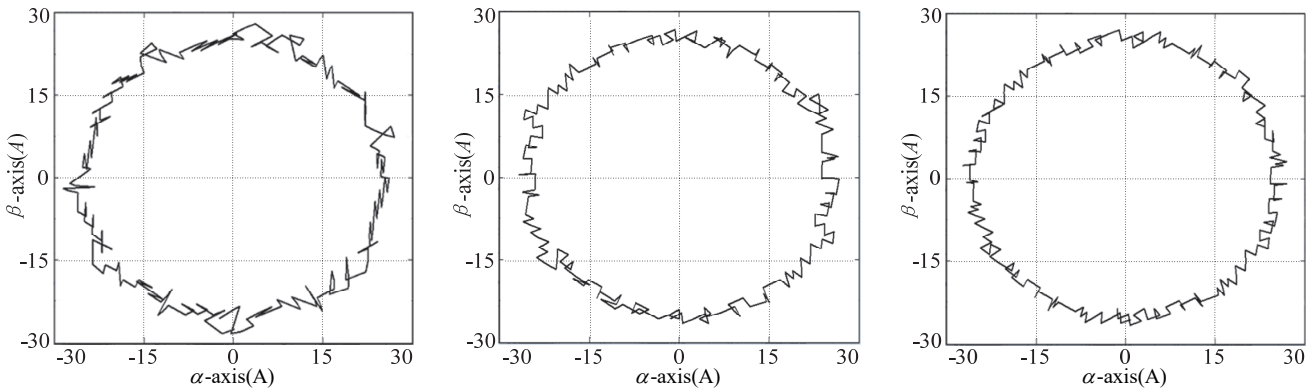


Fig. 10. Trajectories of the three-phase currents in the α-β reference frame of the three methods when parameter combination 1 is adopted in one fundamental period of the grid voltage: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.

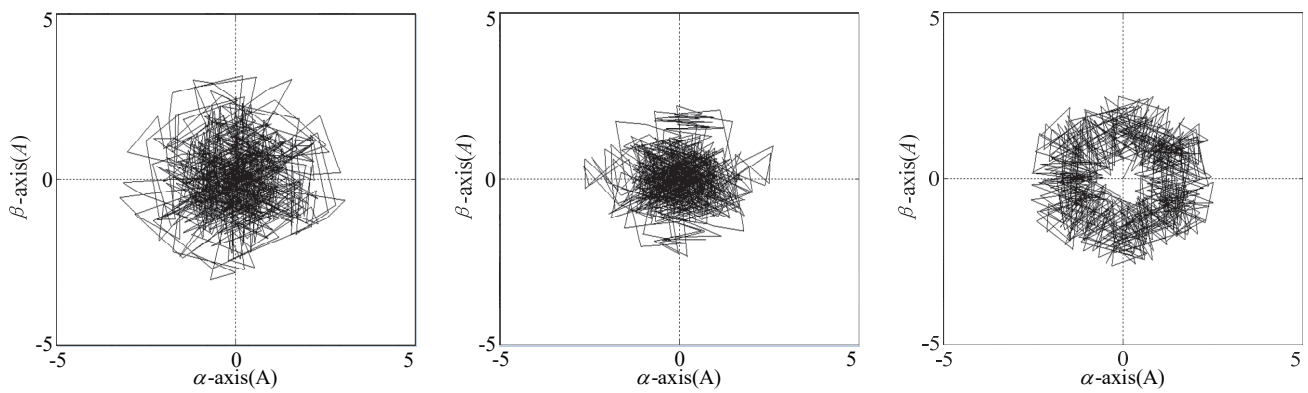


Fig. 11. Trajectories of the three-phase current tracking error in the α-β reference frame of the three methods when parameter combination 1 is adopted in one fundamental period of the grid voltage: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.

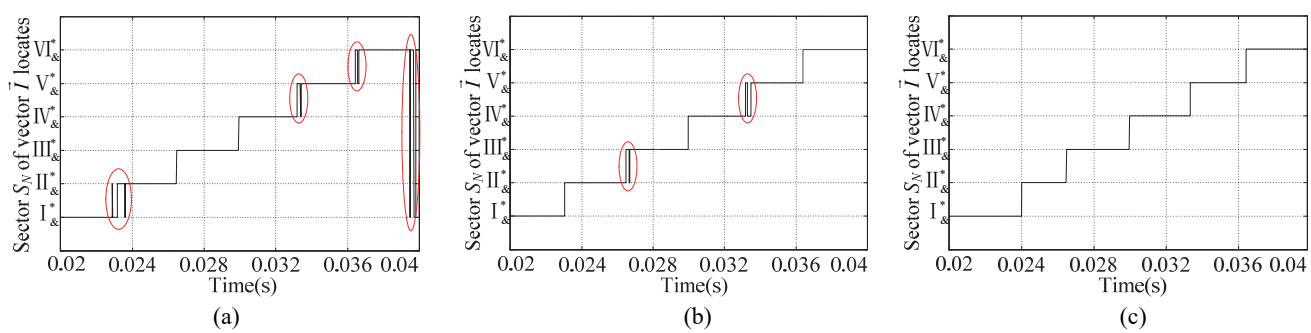


Fig. 12. Sector S_N of the three-phase current rotation vector $\vec{I}$ locates of the three methods when combination 1 is adopted in one fundamental period of the grid voltage: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.

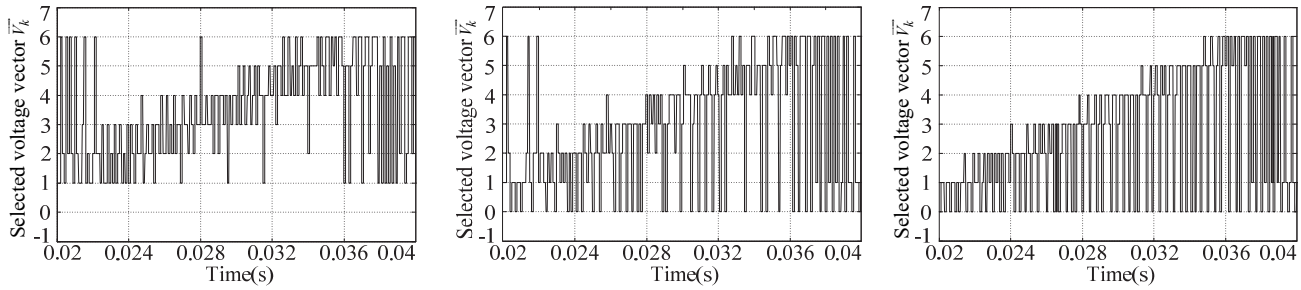


Fig. 13. Selected space voltage vector $\overline{V_k}$ of the three methods when parameter combination 1 is adopted in one fundamental period of grid voltage: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.

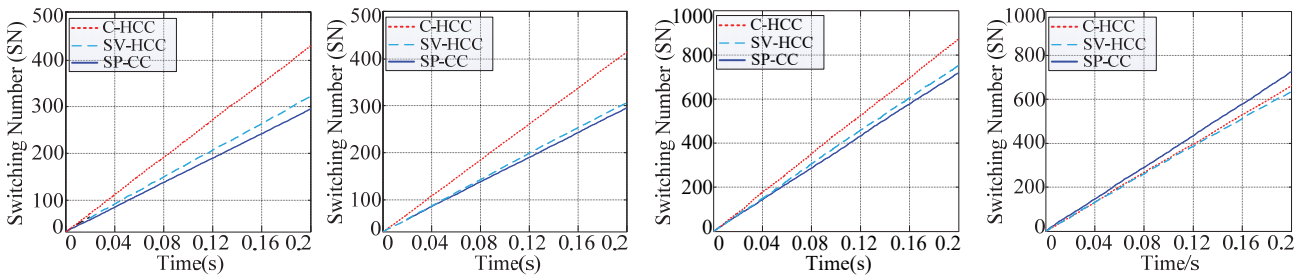


Fig. 14. Switching number SN of the a-phase bridge arm during 0-0.2 s of the three methods when the four groups of parameter combinations are adopted: (a) Parameter combination 1; (b) Parameter combination 2; (c) Parameter combination 3; and (d) Parameter combination 4.

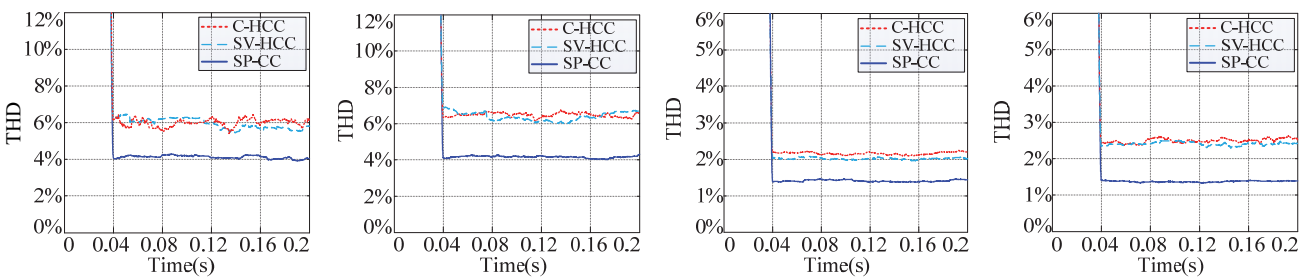


Fig. 15. Instantaneous THD of the a-phase current i_a of the three methods when the four groups of parameter combinations are adopted: (a) Parameter combination 1; (b) Parameter combination 2; (c) Parameter combination 3; and (d) Parameter combination 4.

SV-HCC. As a result, it turns out from the comparison results of Fig. 14(a) and (b) and those of Fig. 15(a) and (b) that, when the control frequency is 10 kHz, the presented SP-CC can achieve a lower SN and a better current control performance than both the C-HCC and the SV-HCC.

In the simulation test, the control frequency is 40 kHz (control period T=25μs), i.e., the situation of the parameter combinations 3 and 4 are adopted. Due to the smaller control period than the test of 10 kHz, the Δi_w of SV-HCC is set to 0.8 A. It should be noted that the i_w of C-HCC and the i_{w_sv} of SV-HCC are kept the same as the test of 10 kHz. Generally speaking, for all of the three current control methods, because of the shorter control period than the test of 10 kHz, the SN increases and the current THD decreases. The comparison results between Fig. 14(c) and (d) show that due to the increasing of hysteresis bandwidth in parameter combination 4 when compared to that in parameter combination 3, the SNs of both the C-HCC and the SV-HCC are even lower than the presented SP-CC. However, for the same reason, it can be known from the comparison results between Fig. 15(c) and (d) that the instantaneous current THD of both the C-HCC and the SV-HCC become larger. However, in particular, the instantaneous current THD of the presented SP-CC is superior to those of the other two HCC methods in the all of the comparison results of the 4 parameter combinations.

From the simulation comparison results of Fig. 14 and Fig. 15 and the analysis presented earlier, it can be concluded that the SN of the SV-HCC is lower than that of the C-HCC and that the instantaneous current THD of the SV-HCC is similar to that of the C-HCC. Furthermore, it is apparent that the presented SP-CC, when compared with the C-HCC and SV-HCC, can always achieve the lowest THD of the AC current under any parameter combinations. Moreover, on the basis of low current THD performance, the presented SP-CC has the lowest SN among the three current control methods when the i_w of C-HCC and the i_{w_sv} of SV-HCC are both set

to 0A, which can make the two HCCs have the lowest current THD for themselves. Although the increasing of the i_w of C-HCC and the i_{w_sv} of SV-HCC can make the two HCC methods achieve a lower SN than the SP-CC as shown in Fig. 14(d), the THD becomes worse. Therefore, the main advantage of the presented SP-CC is reducing the current THD, and concurrently, maintaining a relatively low SN.

B. Experiment Verification

The C-HCC, the SV-HCC and the SP-CC were tested using a VSC prototype, as shown in Fig. 16, and the VSC works in rectifier mode. In addition, the current THD is measured by FLUKE-43B, while the power loss is measured by an analyzer WT1600. The specifications are shown in Table III and parameter combination 1 is adopted.

The experiment results in Fig. 17 show the *a*-phase upper bridge arm switching signals s_a and current i_a of the three methods. In addition, the experiment results in Fig. 18 show the *a*-phase current THD of the three methods. Moreover, the operation power is 1.2 kW and the DC bus reference voltage is 200 V in the experiment tests. As shown in Fig. 17, it can be seen that the SN reaches 34, 27 and 23 for the three methods in one fundamental period. In addition, both the current ripple and the SN of the presented SP-CC are minimal among the three methods. In addition, as shown in Fig. 18, the THD values of the three methods are 4.8%, 4.8% and 3.8%. Obviously, it can be seen that the current THDs of the C-HCC and the SV-HCC are almost the same, and that they are larger 26.3% than the current THD of the presented SP-CC. According to the analysis of the experiment results in Fig. 17 and Fig. 18, the advantages of the SP-CC to C-HCC and SV-HCC are demonstrated. In addition, the experiment results are fully coincided with the simulation results.

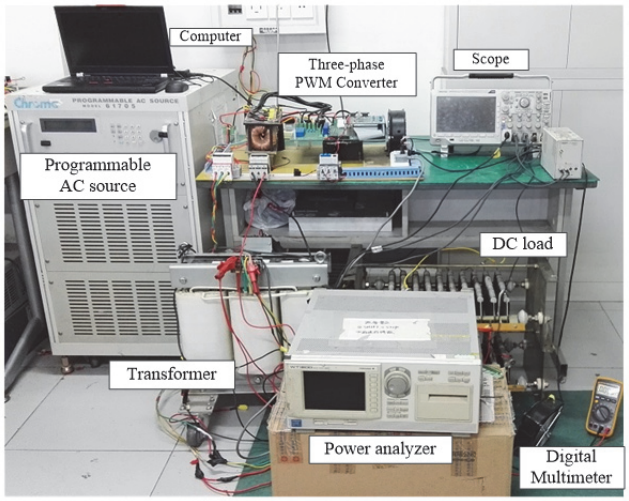
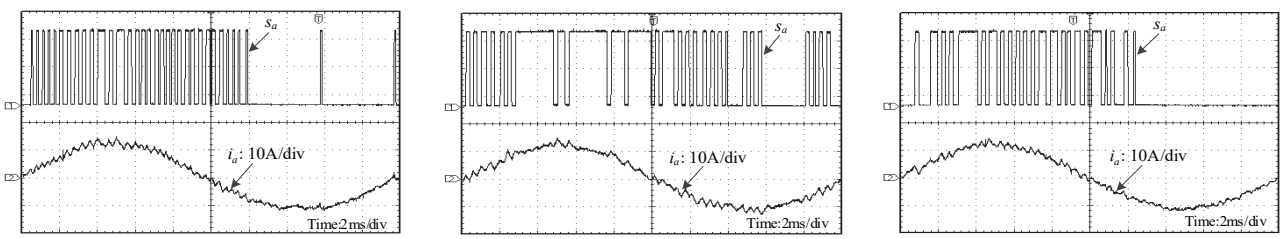


Fig. 16. Layout of the three-phase VSC experiment prototype.

TABLE V
EFFICIENCY COMPARISON OF THE THREE METHODS

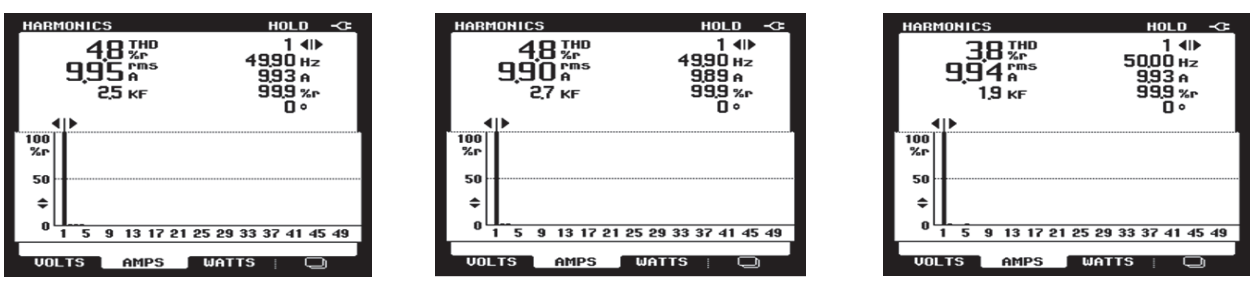
Control methods	Input Power P_{in}/W	Output Power P_{out}/W	Power loss P_{loss}/W	Efficiency η
C-HCC	1325.1	1204.4	120.7	90.89%
SV-HCC	1314.0	1204.1	109.9	91.64%
SP-CC	1311.5	1205.8	105.7	91.94%

Fig. 19 shows the input and output powers which are obtained by the WT1600. Table V summarizes the data obtained by the WT1600 and gives power loss and efficiency comparisons of the three methods. From Table V it can be seen that under the same experiment conditions of the three methods, the SP-HCC has the highest efficiency and the lowest power loss. It can also be seen that the efficiency of the SV-HCC is slightly lower than that of the SP-HCC.



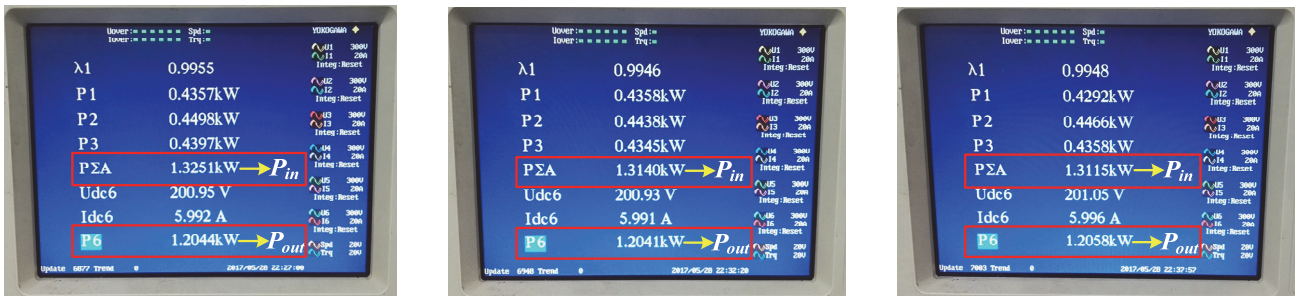
(a) (b) (c)

Fig. 17. Waveforms of the a-phase upper-bridge switching signals and i_a of the three methods: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.



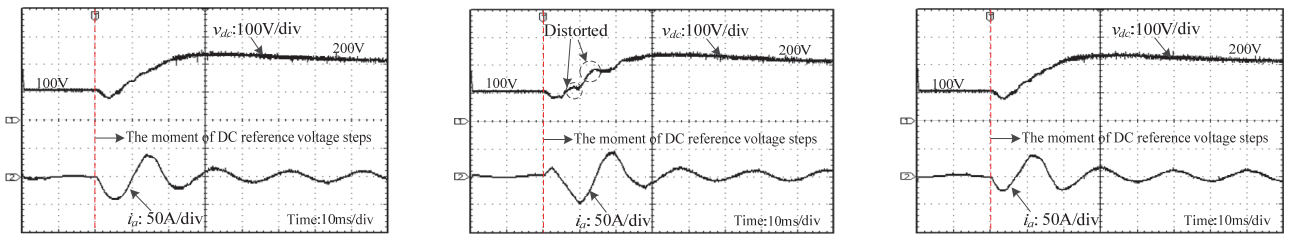
(a) (b) (c)

Fig. 18. Harmonic contents of the a-phase currents i_a of the three methods: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.



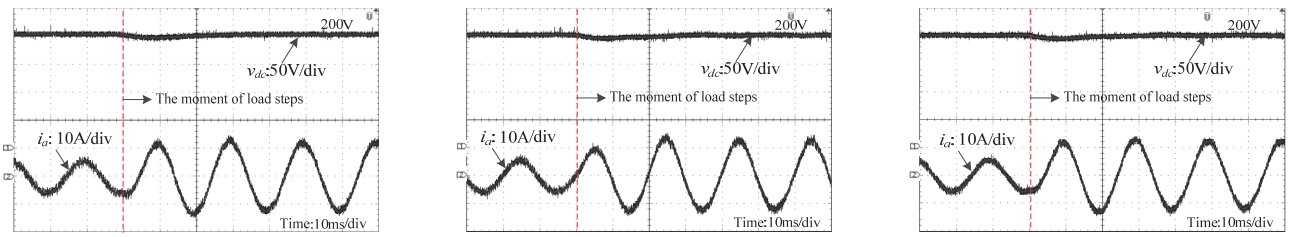
(a) (b) (c)

Fig. 19. Measurement results of the input power P_{in} and output power P_{out} of the three methods: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.



(a) (b) (c)

Fig. 20. Ascent stage waveforms of the DC bus voltage v_{dc} and a-phase current i_a of the three methods when the DC bus voltage reference value steps from 100V to 200V: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.



(a) (b) (c)

Fig. 21. Waveforms of the DC bus voltage v_{dc} and a-phase current i_a of the three methods when the DC-side load resistor steps from 60Ω to 33Ω: (a) C-HCC; (b) SV-HCC; and (c) SP-CC.

However, the efficiency of the C-HCC is the lowest among the three methods. The efficiency comparison is fully coincided with the SN comparison which was obtained from the simulation results of Fig. 14(a) and Fig. 17. Therefore, as a result, the highest SN (or switching frequency) that can cause a higher switching loss of the C-HCC leads to its lowest efficiency. On the other hand, the presented SP-CC has the highest efficiency with the lowest SN, along with the best current control accuracy and performance.

To compare the transient/dynamic response performance of the three current control methods, a step change of the DC bus reference voltage is given from 100 V to 200 V in the experiment test shown in Fig. 20, and a step change of the DC load is given from 60Ω to 33Ω in the experiment test shown in Fig. 21. As shown in Fig. 20, the ascent stage of the DC voltage v_{dc} and *a*-phase current i_a, in both the C-HCC and the presented SP-CC, are similar. This means that the dynamic response processes of the C-HCC and SP-CC are close to each other. However, the ascent stage of the DC voltage has a little distortion in the SV-HCC, since the DC voltage control loop cannot adjust the reference value in time when a current error is large which is an inherent phenomenon of the SV-HCC. Nevertheless, the total dynamic adjustment time of the DC voltage v_{dc} and *a*-phase current i_a are similar among the three methods. As shown in Fig. 21, when the DC load step changes, all of the dynamic adjustment processes of the three methods are similar. In

TABLE VI
COMPREHENSIVE PERFORMANCE COMPARISON OF THE THREE METHODS

Category	Performance comparison
Algorithm Complexity	SP-CC <≈SV-HCC > C-HCC
Number of hysteresis band	SP-CC (not required) < C-HCC (i_w) < SV-HCC(i_{w_sv} and Δi_w)
Dependence on system	SP-CC (need L and T) > C-HCC ≈ SV-HCC (not required)
Transient response	SP-CC ≈ C-HCC ≈ SV-HCC
THD	SP-CC < SV-HCC ≈ C-HCC
SN	SP-CC <≈ SV-HCC < C-HCC
Efficiency	SP-CC >≈ SV-HCC > C-HCC

'>' means 'more or better', '<' means 'less or worse' and '≈' means 'similar.
'>≈' means 'similar or lightly higher, '<≈' means 'similar or lightly lower/simpler.

consideration of the simulation results in Fig.9 and the experiment results in Fig. 20 and 21, it can be concluded that the C-HCC, the SV-HCC and the presented SP-CC have similar transient/dynamic performances.

Table IV summarizes the results of a comparative study based on the theoretical analysis and experimental results for the C-HCC, the SV-HCC and the presented SP-CC. From Table IV it can be seen that the presented SP-CC has a lower current THD and a relatively lower SN, while having higher system efficiency than the C-HCC and the SV-HCC.

VI. CONCLUSION

In this paper, a novel switching pattern current control (SP-CC) scheme is presented for three-phase VSCs. Since it is a COFC method based on the principle of SVM, the SP-CC can choose the optimal SP. With the SP-CC, the current error can be reduced in the correct direction. Comparison results with the C-HCC and the SV-HCC are obtained by simulation and experiment tests. They are consistent with each other, and fully illustrate the feasibility and superiority of the presented SP-CC. Moreover, the presented SP-CC can combine the fast transient response performance of the C-HCC and the small SN characteristic of the SV-HCC. It can also achieve less current harmonic content, while achieving a lower switching loss and a higher efficiency. In addition, with the presented SP-CC, the hysteresis band is not required, and only the logical operation is required. Obviously, the only information required for the implementation of the SP-CC is the control period and the AC filter inductance value, which leads to easy and simple debugging/computational processes of the SP-CC. As a result, the presented SP-CC can possess a lower current THD with a higher efficiency than the C-HCC and the SV-HCC.

REFERENCES

[1] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron*., Vol. 24, No. 3, pp. 654-664, Mar. 2009.

[2] X. Guo and X. Jia, "Hardware-based cascaded topology and modulation strategy with leakage current reduction for transformerless PV systems," *IEEE Trans. Ind. Electron*., Vol. 62, No. 12, pp. 7823-7832, Dec. 2016.

[3] IEA-PVPS. (2005, Oct.). Cumulative installed PV power [Online]. Available: www.iea-pvps.org

[4] X. Guo, B. We, T. Zhu, Z. Lu, L. Tan, X. Sun, and C. Zhang, "Leakage current suppression of three phase flying capacitor PV inverter with new carrier modulation and logic function," *IEEE Trans. Power Electron*., DOI: 10.1109/TPEL.2017.2692753.

[5] X. Guo, "Three phase CH7 inverter with a new space vector modulation to reduce leakage current for transformerless photovoltaic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, Vol. 5, No. 2, pp. 708-712, Jun. 2017.

[6] F. Xu, M. Cheng, J. Zhang, and K. Zhou, "Investigation of control scheme for PWM VSR under three-phase voltage unbalance conditions," in *Power Electronics for Distributed Generation Systems (PEDG), 2010 2nd IEEE International Symposium on*, pp. 835-840), 2010.

[7] X. Guo, W. Wu, and Z. Chen, "Multiple-complex-coefficient-filter- based phase-locked loop and synchronization technique for three-phase grid interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron*., Vol. 58, No. 4, pp. 1194-1204, Apr. 2011.

[8] A. Bouafia, F. Krim, and J.-P. Gaubert, "Fuzzy-Logic-Based Switching State Selection for Direct Power Control of Three-Phase PWM Rectifier," *IEEE Trans. Ind. Electron*., Vol. 56, No. 6, pp. 1984-1992, Jun. 2009.

[9] P. Cortés, J. Rodríguez, P. Antoniewicz, and M. Kazmierkowski, "Direct power control of an AFE using predictive control," *IEEE Trans. Power Electron.*, Vol. 23, No. 5, pp. 2516-2523, Sep. 2008.

[10] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "Novel current error space phasor based hysteresis controller using parabolic bands for control of switching frequency variations," *IEEE Trans. Ind. Electron*., Vol. 54, No. 5, pp. 2648-2656, Oct. 2007.

[11] C. T. Pan and J.-J. Shieh, "A family of closed-form duty cycle control laws for three-phase boost AC/DC converter," *IEEE Trans. Ind. Electron*., Vol. 45, No. 4, pp. 530-543, Aug. 1998.

[12] M. Hartmann, S. D. Round, H. Ertl, and J. W. Kolar, "Digital current controller for a 1 MHz, 10 kW three-phase VIENNA rectifier," *IEEE Trans. Power Electron.*, Vol. 24, No. 11, pp. 2496-2508, Nov. 2009.

[13] Y. Tang, P. C. Loh, P. Wang, and F. H. Choo, "One-cycle controlled three-phase PWM rectifiers with improved regulation under unbalanced and distorted input voltage conditions," *IEEE Power Electronics and Drive Systems Conference*, pp. 579-584, 2009.

[14] D. V. Ghodke, Sreeraj E. S., K. Chatterjee, and B. G. Fernandes, "One-cycle-controlled bidirectional AC-to-DC converter with constant power factor," *IEEE Trans. Ind. Electron*., Vol. 56, No. 5, pp. 1499-1510, May 2009.

[15] T. Jin, L. Li, and K. M. Smedley, "A universal vector controller for three phase PFC, APF, STATCOM, and grid-connected inverter," in *Proc. IEEE. Appl. Power Electron. Conf. Expo.*, Vol. 1, pp. 594-600, 2004.

[16] Q. Chongming and K. M. Smedley, "Unified constant-frequency integration control of three-phase standard bridge boost rectifier," in *Proc. IEEE. Power Electron. Congr. CIEP*, pp. 131–135, 2000.

[17] Q. Chongming, K. M. Smedley, and F. Maddaleno, "A single-phase active power filter with one-cycle control under unipolar operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 51, No. 8, pp. 1623-1630, Aug. 2004.

[18] O. Vodyakho, T. Kim, S. Kwak, and C. S. Edrington, "Comparison of the space vector current controls for shunt active power filters," *IET Power Electron.*, Vol. 2, No. 6, pp. 653-664, Nov. 2009.

[19] A. Bouafia, J.-P. Gaubert, and F. Krim,"Predictive direct power control of three-phase pulse width modulation (PWM) rectifiers using space-vector modulation (SVM)," *IEEE Trans. Power Electron.*, Vol. 25, No. 1, pp. 228-236, Jan. 2010.

[20] M. Mohseni and S. M. Islam, "A new vector-based hysteresis current control scheme for three-phase pwm voltage-source inverters," *IEEE Trans. Power Electron.*, Vol. 25, No. 9, pp. 2299-2309, Sep. 2010.

[21] K. M. Rahman, M. R. Khan, M. A. Choudhury, and M. A. Rahman, "Variable band hysteresis current controllers for PWM voltage source inverters," *IEEE Trans. Power Electron.*, Vol. 12, No. 6, pp. 964-970, Nov. 1997.
[22] R. Ramchand, K. Sivakumar, A. Das, C. Patel, and K. Gopakumar, "Improved switching frequency variation control of hysteresis controlled voltage source inverter-fed IM drives using current error space vector," *IET Power Electron*, Vol. 3, No. 2, pp. 219-231, Mar. 2010.
[23] J. A. Suul, K. Ljokelsoy, T. Midtsund, and T. Undeland, "Synchronous reference frame hysteresis current control for grid converter applications," *IEEE Trans. Ind. Electron.*, Vol. 47, No. 5, pp. 2183-2194, Sep./Oct. 2010.
[24] H. T. Mokui, M. Mohseni, and M. A. S. Masoum, "Implementation of space vector based hysteresis current control for full converter wind generation system," *Innovative Smart Grid Technologies Asia. IEEE*, pp. 1-7, 2011.
[25] A. Dey, P. P. Rajeevan, R. Ramchand, K. Mathew, and K. Gopakumar, "A space-vector-based hysteresis current controller for a general n-level inverter-fed drive with nearly constant switching frequency control," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 1989-1998, May 2013.
[26] C. Bharatiraja, S. Jeevananthan, R. Latha, and V. Mohan, "Vector selection approach-based hexagonal hysteresis space vector current controller for a three phase diode clamped MLI with capacitor voltage balancing," *IET Power Electron.*, Vol. 9, No. 7, pp. 1350-1361, 2016.
[27] B.-H. Kwon, T.-W. Kim, and J.-H. Youm, "A novel SVM-based hysteresis current controller," *IEEE Trans. Power Electron.*, Vol. 13, No. 2, pp. 297-307, Mar. 1998.
[28] A. Fereidouni and M. A. S. Masoum, "A new space-vector Hysteresis current-control modulation for active power filter applications," *Power Tech, 2015 IEEE Eindhoven.*, 2015.
[29] M. P. Kazmierkowski, M. A. Dzieniakowski, and W. Sulkowski, "Novel space-vector based current controllers for PWM-inverters," *IEEE Trans. Power Electron.*, Vol. 6, No. 1, pp. 158-166, Jan. 1991.
[30] C. T. Pan and T. Y. Chang, "An improved hysteresis current controller for reducing switching frequency," *IEEE Trans. Power Electron.*, Vol. 9, No. 1, pp. 97-104, Jan. 1994.
[31] E. Aldabas, L. Romeral, A. Arias, and M. G. Jayne, "Software-based digital hysteresis-band current controller," in *Proc. Electric Power Appl.*,Mar., pp. 184-190, 2006.
[32] T.-S. Lee, "Input–output linearization and zero-dynamics control of three-phase AC/DC voltage-source converters," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 11-12, Jan. 2003.
[33] J. F. Silva, "Sliding-mode control of boost-type unity-power-factor PWM rectifiers," *IEEE Trans. Ind. Electron.*, Vol. 46, No. 3, pp. 594-603, Jun.1999.
[34] K. Jezernik and B. Mohorko, "Variable structure system control of unity power factor boost converter," in *Proc. PEMC'96,* Vol. 3, pp. 213-217, 1996.
[35] J. G. Hwang and P. W.Lehn, "A single-input space vector for control of AC–DC converters under generalized unbalanced operating conditions," *IEEE Trans. Power Electron*, Vol. 25, No. 8, pp. 2068-2081, Aug. 2010.
[36] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: A survey," *IEEE Trans. Ind. Electron.*, Vol. 45, No. 5, pp. 691-703, Oct. 1998.
[37] Z. Li, Y. Li, P. Wang, H. Zhu, C. Liu, and W. Xu, "Control of three-phase boost-type PWM rectifiers in stationary frame under unbalanced input voltage," *IEEE Trans. Power Electron.*, Vol. 25, No. 10, pp. 2521-2530, Oct. 2010.

Hongyan Zhao was born in Hebei Province, China, in 1988. He received his B.S. and M.S. degrees in Electrical Engineering from Yanshan University, Qinhuangdao, China, in 2010 and 2013, respectively. Since 2013, he has been working towards his Ph.D. degree in Electrical Engineering from Beijing Jiaotong University, Beijing, China. His current research interests include three-phase grid-connected systems, renewable power systems and electric vehicles.

Yan Li was born in Heilongjiang Province, China, in 1977. She received her B.S. and M.S. degrees in Electrical Engineering from Yanshan University, Qinhuangdao, China, in 1999 and 2003, respectively; and her Ph.D. degree in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2009. From 1999 to 2009, she was at Yanshan University. Since 2009, she has been in the School of Electrical Engineering, Beijing Jiaotong University, Beijing, China. Her current research interests include multiple-input dc/dc converters, renewable power systems and PV grid-tied systems.

Trillion Q. Zheng (Qionglin Zheng) (M'06-SM'07) was born in Jiangshan, Zhejiang Province, China, in 1964. He received his B.S. degree in Electrical Engineering from Southwest Jiaotong University, Sichuan, China, in 1986; and his M.S. and Ph.D. degrees in Electrical Engineering from Beijing Jiaotong University, Beijing, China, in 1992 and 2002, respectively. He is presently working as a University Distinguished Professor at Beijing Jiaotong University. He directs the Center for Electric Traction, founded by Ministry of Education, China. His current research interests include the power supplies and AC drives of railway traction systems, high performance and low loss for power electronics systems, PV based converters and control, and active power filters and power quality correction. He holds 17 Chinese patents, and has published over 60 journal articles and more than 100 technical papers in conference proceedings. From 2003 to 2011, he served as the Dean of the School of Electrical Engineering at Beijing Jiaotong University. He is presently working as the Deputy Director of the Council of the Beijing Society for Power Electronics, and as a Council Member of the China Electrotechnical Society. He received an Excellent Teacher Award from the Beijing Government (1997), and a Youth Award of Railway Science and Technology of Zhan Tianyou (2005). He was Laureates of the Youth Elite of Science and Technology of the Railway Ministry of China (1998), and a Zhongda Scholar in the areas of power electronics and motor drive, by the Delta Environmental and Educational Foundation (2007).