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Improved Trigger System for the Suppression of Harmonics and EMI Derived from the Reverse-Recovery Characteristics of a Thyristor

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Abstract

This paper analyses the harmonic pollution to power grids caused by thyristor-controlled devices. It also formulates a mathematic derivation for the voltage spikes in thyristor-controlled branches to explain the harmonic and EMI derived from the reverse-recovery characteristics of the thyristor. With an equivalent nonlinear time-varying voltage source, a detailed simulation model is established, and the periodic dynamic switching characteristic of the thyristor can be explicitly implied. The simulation results are consistent with the probed results from on-site measurements. An improved trigger system with gate-shorted circuit structure is proposed to reduce the voltage spikes that cause EMI. The experimental results indicate that a prototype with the improved trigger system can effectively suppress the voltage spikes.

Key words: Electromagnetic interference (EMI), Harmonic, Thyristor, Trigger system, Voltage spike

I. INTRODUCTION

With the rapid development of power electronics, Flexible AC Transmission System (FACTS) equipment is being widely applied in power systems [1]-[3]. The extensive development of electronic systems and telecommunications has led to major concerns in terms of electromagnetic pollution. Among the concerned parameters, the EMI (Electro Magnetic Interference) and harmonics which are generated by the switch process of power electronic switches, have received a great deal of attention [4]-[6]. The EMI and harmonics may affect normal operation or cause a malfunction of sensitive equipment positioned nearby if appropriate immunity measures are not taken. Furthermore, the harmonics increase the additional harmonic loss, which causes resonance. Some researchers have focused on the phenomenon where a Thyristor-controlled Static Var Compensator (SVC) brings harmonic to a grid system and its neighbouring devices [7]. In addition, they have proposed harmonic circuit models to analyse the effects of power electronics devices [8], [9]. These sensitive electronic units are vulnerable to electromagnetic disturbances from the FACTS equipment itself or from neighbouring devices, which leads to unit malfunctions and damages [10]. Since the EMI problems associated with FACTS equipment are unavoidable, the electromagnetic emissions should be monitored and evaluated to set an appropriate immunity level to guarantee the correct operation of the secondary control units [11]. At a rough estimate, in term of the noise emission level in power systems, the noise produced by the semiconductor switching process is one of the strongest noises [12]. The non-ideal dynamic characteristics of the semiconducting switching devices gives rise to current spikes in the controlled branches, which introduces energy loss, EMI and harmonic pollution [13] into the grid system in practical engineering applications [14]. A great number of studies on reducing switching loss and EMI have been proposed [15]-[18].

To predict the instantaneous junction temperature, its rise and the energy loss during the turn-on and turn-off processes, an

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outline of a measuring device is proposed [19], [20]. Moreover, the proposed model can express the interaction among the semi-conducted components in FACTS devices [21]. These models are effective tools in the actual design of high power inverters [22]-[24].

A proper method to suppress EMI is to minimize its generating source. In this study, a novel solution for the suppression of noise sources is proposed. Through a novel trigger system, the voltage spike of the thyristor is reduced, which results in a significant EMI reduction. Since it is one of the technically mature types of SVC equipment, the Thyristor Switched Capacitor (TSC) is analysed as an example in this paper.

This paper is organized as follows. Firstly, a theory formula of the interference current is derived with consideration of the periodic switching characteristic of a thyristor, and a model of the electromagnetic emission is also established. Secondly, based on the macro model for a thyristor, a new concrete model of the TSC is proposed. Thirdly, an improved trigger system with a gate-shorted structure is designed and implemented to suppress the current spikes in the thyristor-controlled branch. Experimental results, which are consistent with the theoretical analysis, are also discussed in this paper.

II. Analysis and Model

A. Reverse Recovery Voltage Peak Mechanism of a Thyristor

To analyse the switching transition mechanism of a thyristor, the reverse recovery process is firstly described in this paper. The characteristic curves of the current and voltage during turn-on process are shown in Fig. 1.

The dynamic characteristic of the thyristor includes three stages: the turning on state, the expanding state and the turning off state [25]. The characteristic curve of the current and voltage during the turn-on process is shown in Fig. 1. Starting with a trigger signal, the anode current gradually rises to a stable value after the delay process, while the terminal voltage gradually falls to the conducting-state voltage from the blocking voltage.

To switch the thyristor from its on-state mode to the reverse blocking mode, it is necessary to remove the free carriers to enable the formation of a depletion region that can support a high electric field. The process of switching the P-i-N rectifier from the on-state to the blocking state is referred to as reverse recovery. The turning-off process is a two-stage process that is divided into the reverse recovery time t_{rr} and the gate recovery time t_{gr}.

After the reverse recovery process, the thyristor recovers the reverse blocking capacity. However, the excess carriers in the base region still exist. The thyristor changes to the reliable turning off state after a period of gate recovery time t_{gr}. The reverse charge Q_{gr} is the time integral of the reverse recovery current, i.e.

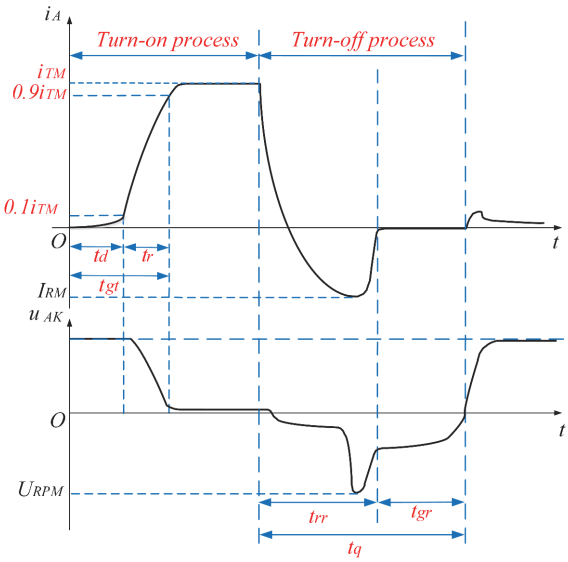


Fig. 1. Voltage and current curves during the turning-on and turning-off processes.

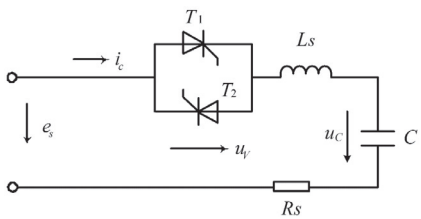


Fig. 2. Single-phase equivalent circuit of a TSC.

$$Q_{rr} = \int_{t_1}^{t_2} i_{rr} dt \tag{1}$$

The turn-off time t_q increases the switching loss and greatly limits its usage. The turning off switch loss P_{on} can be expressed quantitatively as:

$$P_{on} = fI_R U_R t_{rr} / 4.4 \tag{2}$$

where f represents the switching frequency, I_R is the reverse recovery current, U_R represents the reverse recovery voltage, and t_{rr} is the recovery time. Therefore, suppressing the reverse recovery voltage and minimizing the reverse time are two efficient methods to reduce the switching loss and to control the temperature rise [26].

The peak reverse current and the turn-off time can be reduced by reducing the minority carrier lifetime in the drift region of the P-i-N rectifier structure. In this paper, a novel solution to improve the reverse recovery process of a thyristor is proposed.

B. The Modeling and Simulation

The core switching units of SVCs are antiparallel thyristors, which are noise sources in the main loop. The equivalent of a typical single-phase TSC is shown in Fig. 2, in which antiparallel couple thyristors *T1 & T2* are used as a solid switch.

R_s is the contact resistance, which is in parallel with the self-healing low-voltage compensating capacitor C. L_s is the equivalent inductance of the main loop. u_V is the terminal

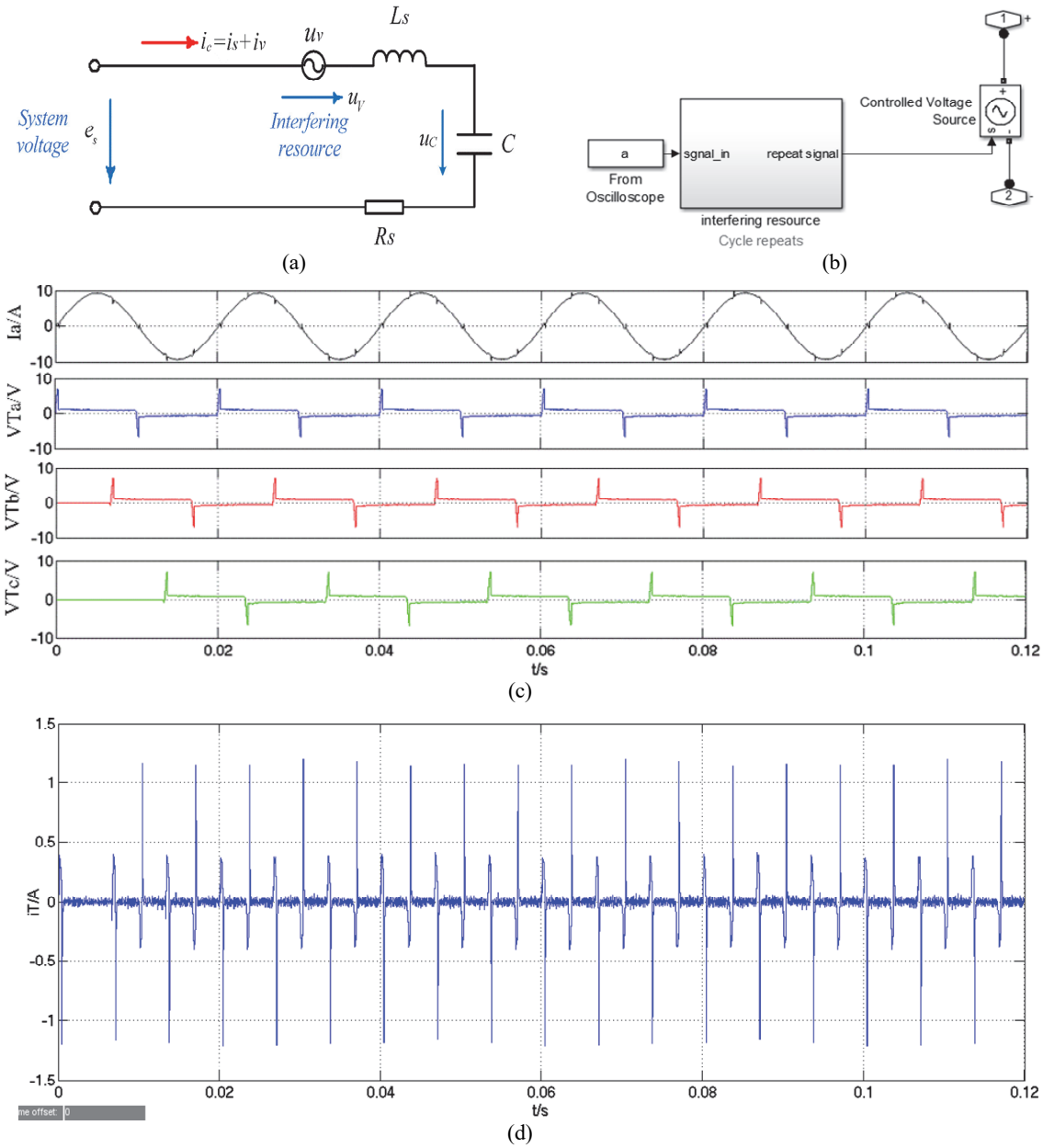


Fig. 3. Simulation and results. (a) Equivalent circuit of model. The excitation of the equivalent circuit contains two sources: the system voltage and the interfering resource. (b) The simulation subsystem of the interfering resource. (c) The simulation result of the capacitor current and the interference source. (d) The simulation result of the interference current.

voltage of the thyristors. u_c is the voltage drop of the compensating capacitor. e_s is the voltage of the grid. i_c is the current of the capacitor.

In accordance with the substitution theorem in the TSC branch, the non-linear switch can be replaced with an equivalent voltage source. As shown in Fig. 3(a), based on the superposition theorem, the current of the TSC branch is considered as an effect of the two voltage source, i.e.,

$$i_c = i_s + i_v \tag{3}$$

where i_s is the current response of the system voltage, and i_v is the current response of the equivalent interfering resource.

A simulation platform using MATLAB/SIMULINK is built as follows. Discrete date exported from an oscilloscope is imported to the workplace of MATLAB and modelled as a subsystem of the interfering resource as shown in Fig. 3(b). In this case, the main circuit of the TSC branch is in a delta connection with the switch inside. The power grid voltage is 400V (phase to phase), and the value of the shunt capacitors is 80μF with a 0.5Ω internal resistance. The stray inductance is assumed as 3μH [27]. The simulation result is shown in Fig. 3(c), in which i represents the current of flowing the shunt capacitors, and *VTa*, *VTb* and *VTc* represent the thyristors' terminal voltages for three phases, respectively. The interference current component brought by the interference source is shown in Fig. 3(d).

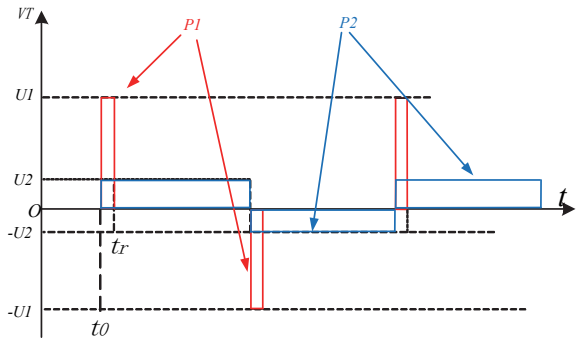


Fig. 4. The simplified voltage waveform between the terminals of the switch.

C. Frequency Domain Analysis

The inertial system has the same current response if the signals have the same impulse to time, even if they have different shapes. The waveform of the terminal voltage of the switch can be simplified as shown in Fig. 4, where the periodic waveform is simplified as two pulse series, *P1* and *P2*.

Considering the periodic pulse P1, regardless of the negative pulse, this study puts emphasis on analysing the spectrum of the positive pulse series whose pulse width is τ and whose period is T.

The amplitude-frequency response can be expressed as:

$$F_n = \frac{1}{T}\int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} e^{-jn\Omega t}dt = \frac{\tau}{T}\times Sa(n\Omega\tau/2)(n=0,\pm1,\pm2,...) \quad (4)$$

with:

$$Sa(x) = \sin x / x \quad (5)$$

where $\Omega=2\pi/T$ is the fundamental frequency and $\omega=n\Omega$. The envelope curve of F_n is the spectral line of a positive square wave.

The line spectrum envelope, which is the curve of $Sa(\omega\tau/2)$, has a zero-point when $\omega=2m\pi/\tau(m=0,\pm1,\pm2,...)$. Therefore, the narrower the pulses become, the higher frequency of zero-points get. As shown in Fig. 5, the spectral range of the pulse where $\tau=1ms$ and $T=20ms$ is much wider than the first two situations.

As the component P2 in Fig. 4, the quasi-square wave, which is the steady terminal voltage of the thyristors, can be expressed by a Fourier series as:

$$e = U_m^{(n)}\sum_{n=1}^{\infty}\sin(n\omega t)\left(n=1,3,5\ldots\right) \quad (6)$$

where:

$$U_m^{(n)} = \frac{4U_2}{n\pi} \quad (7)$$

Based on the principle of superposition, the steady components of certain can be expressed as:

$$U_m^{(n)}\angle 0 = \left[R + j\left(n\omega L - \frac{1}{n\omega C}\right)\right]\dot{I}^{(n)} \quad (8)$$

This implies that:

$$\dot{I}^{(n)} = \frac{U_m^{(n)}}{\sqrt{R^2+\left(n\omega L-\frac{1}{n\omega C}\right)^2}}\angle\beta \quad (9)$$

where:

$$\beta = -\arctan\left(\frac{n^2\omega^2LC-1}{n\omega RC}\right) \quad (10)$$

In addition, the maximal value of $I^{(n)}$ occurs when:

$$n_0 = \sqrt{\frac{\frac{2L}{C}-R^2}{2\omega^2L^2}} \quad (11)$$

Thus, the current that respond to the pulse *P2* in Fig. 4 is expressed as:

$$i^{(n)}(t) = \sum_{n=1}^{\infty}\frac{4A_m\sin(n\omega t+\beta)}{\pi\sqrt{n^2R^2+(n^2\omega L-\frac{1}{\omega C})^2}}(n=1,3,5...) \quad (12)$$

where *Am* is the amplitude of the current.

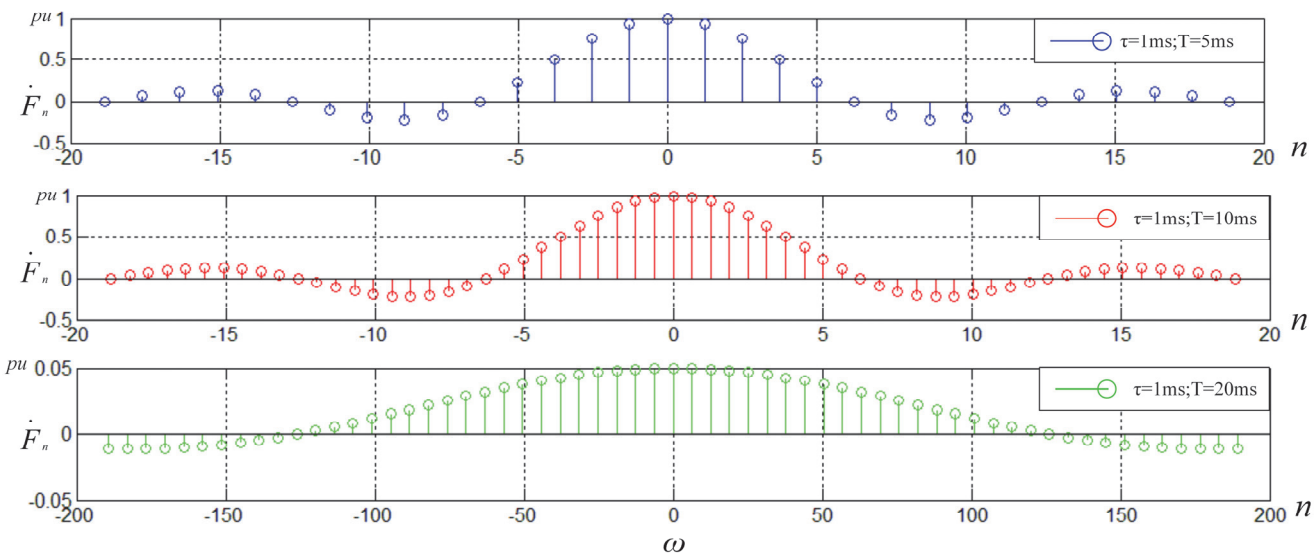


Fig. 5. The spectrum lines of different pulses.

The above analysis implies that the interference current is brought into grid by the TSC in its steady operation state. The harmonic component does not decay with an increasing of the harmonic order. Instead, it reaches the maximum value at a certain order.

Consequently, the interference component *P2*, which is caused by the terminal voltage, mainly consists of the odd harmonics caused by a terminal voltage drop. In addition, the turn-on spike, which is the component *P1*, can cause a high-frequency glitch with a broad spectrum, which increases the switch loss.

Therefore, the pulse *P1* has a greater contribution to EMI. In other words, the influence of *P2* is almost negligible. In this paper, the influence of *P2* is ignored. Therefore, to be effective in EMI reduction, *P1* should be significantly reduced.

III. The Improved Trigger System with a Gate-Shorted Structure

A. Improved Trigger System with a Gate-Shorted Circuit

Considering that reducing the terminal voltage and restraining the reverse recovery pulse voltage can suppress the EMI phenomenon, an improved topology, where a relay is employed to connect the antiparallel thyristors' gate poles together, is proposed.

An equivalent circuit of the improved topology is shown in Fig. 6(a). R_L is the equivalent resistance in the semiconductor device. *S* is a relay used as a switch. *K1 (K2)*, *A1 (A2)* and *G1 (G2)* are the cathode poles, anode poles and gate poles of thyristors *T1* & *T2*, respectively. In the case of a positive half-cycle, the current flows from A to B. Thyristor *T1* is in the turn-on state and *T2* is in the turn-off state. The current flows through R_L and *T1*, and then back to B. Once the thyristor *T1* is triggered, the relay *S* is turned on to connect the two gate poles *G1* and *G2*, while the trigger signal of *T1* can be marked or removed. The thyristor's turn-on state voltage generates the current to the trigger thyristor *T1* through *K2, G2, S* and *G1*. A similar analysis can be adapted to the case of negative half-cycle current.

B. Internal Mechanism of the Improved Trigger System

The essence of this method is using the principle of positive feedback, which is shown as Fig. 6(b). Two thyristors trigger each other by the connection of G1 and G2. The current $I_{trigger}$ increases along with the grid voltage. Once the voltage rises to the current generated on the resistor, it is sufficient to trigger the thyristor, and the thyristor whose A-K terminal voltage is positive is turned on. Therefore, the improved trigger system has the properties of a self-trigger. When the voltage reverses in a period, the thyristor can be turned on automatically without intervention from any detecting or triggering circuits.

The connection of G1 and G2 provides an additional transfer channel for the base carrier, which helps accelerate the reverse-recovery process of the thyristor. Thus, the dv/dt can be

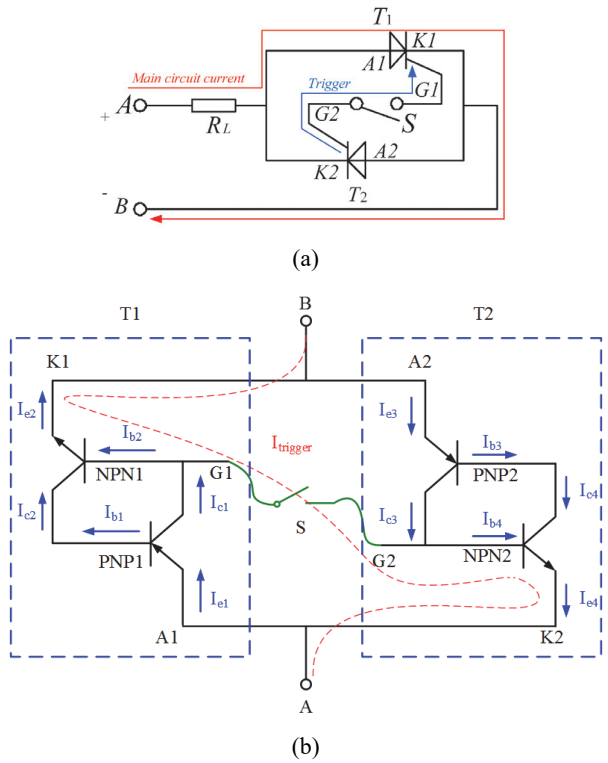


Fig. 6. The improved switch structure with a gate-shorted circuit. (a) The topology of the improved trigger system. (b) The internal mechanism of the improved trigger system.

reduced, resulting in a mitigation of the EMI.

The current of the main circuit can be expressed as:

$$I_{trigger} = \frac{U_{AB}}{R_{KG1} + R_{KG2} + R_L} \tag{13}$$

According to the correlative parameters, the resistance between the K pole and G pole of the thyristor (R_{KG1} and R_{KG2}) is about 20Ω, and R_L is a small resistance. The gate trigger current is about 100mA. According to Equation (13), the thyristor can be turned on when U_{AB} is just about 4V.

C. Control Strategy of the Improved Trigger System

A signal control diagram is shown as Fig. 7(a).

Firstly, the thyristors are turned on by the zero-cross signal of a MOC3083 chip as the traditional solution. In this way, the switch S does not need to withstand the high voltage stress of the power grid. When the main loop has not been conducted, the grid voltage stress is withstood by the MOC3083, whose designed isolation surge voltage is 7500V (peak AC voltage), which is much higher than the grid voltage. When one of the thyristors is triggered, if the switch *S* is connected in this situation, the voltage between the terminals of the thyristors is decreased to the turn-on state voltage of the thyristors. This is only about 1V or less, which is much lower than the grid voltage. Therefore, the switch S is always safe in this situation.

Secondly, after checking and making sure that the main loop has been conducted properly, the switch S is turned on by the

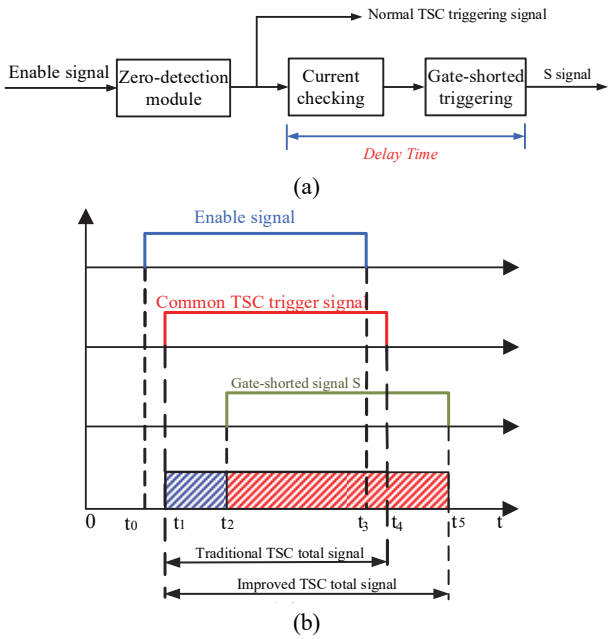


Fig. 7. Control strategy. (a) Control strategy diagram. (b) Sequence of the control signals of the control strategy.

control system. After the switch S is connected, the triggering signal of the MOC3083 chip which is sent from the DSP is short circuited, and the trigger signals of the thyristors are replaced by the current of the gate-shorted circuit. Current checking is an essential step before the triggering of the gate-shorted module. If the switch S is turned on while the thyristor is not in the turn-on state, the voltage between the thyristor's terminals may be high enough which results in a large current flow via the resistance between K-G poles and damages the thyristors. When using the control strategy proposed in this study, the above problem is solved. If the thyristor *T2* is turned off when the current decreases to zero, the thyristor *T1* is turned on when the voltage on its *A-K* terminal changes to positive and the trigger signal is added to its *G* pole. The current $I_{trigger}$ increases along with the grid voltage. Once the voltage rises to the current generated on the resistor, it is sufficient to trigger the thyristor, and the thyristor *T1* is triggered. Therefore, the maximal voltage that the switch *S* needs to withstand is only the voltage that generates the trigger current.

Thirdly, the parallel thyristors take turns to trigger each other in the steady operation state through the connection of two gate poles.

If the capacitor needs to be removed from the grid, the DSP cancels the trigger signal and sends an OFF signal to the switch *S*, which results in a disconnection of two gate poles. After that, the thyristors enter the turn-off state when the current crosses the zero due to the lack of a trigger current.

The sequence of the trigger signal is shown in Fig. 7(b). t_0 is the time when the control system generates the ON signal, t_0-t_1 is the common delay time when the traditional TSC receive the ON signal, and t_1-t_2 is the delay time of the current detection

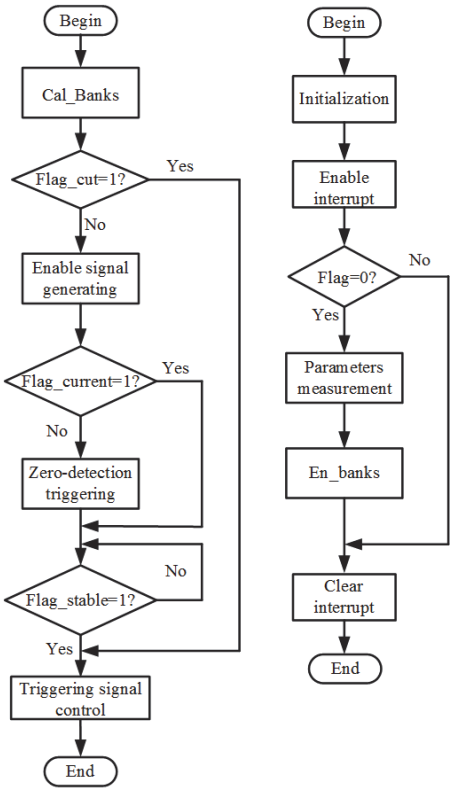


Fig. 8. Flowchart of the control procedure. (a) Main program. (b) Subprogram of En_banks. The control program is executed according to the flowchart.

and the action of switch *S*. t_3 is the time when the control system generates the OFF signal, t_3-t_4 is the delay time of the traditional TSC, t_3-t_5 is the delay time of the TSC with the improved trigger system. Compared with the common control strategy, this control strategy has no delay time when it responds to the ON signal. Meanwhile, this control strategy has a delay time of t_4-t_5 when it responds to the OFF signal. Therefore, the proposed control strategy sacrifices the TSC's fast response time to the OFF signal.

D. Implementation of the Hardware and Software

The DSP used in this device is a TMS320F28335 with a 150-MHz maximum processing speed. It is suitable for the electronic control fields.

The DSP computes sampled values in real time such as the values of V, I, P and Q. Then the DSP estimates the number of capacitor banks and generates a signal to switch the capacitors. The improved trigger system uses an Omron micro relay MY2N-CR-J as the gate-shorted switch in this study.

The procedure mainly consists of a main program, an ADC measurement subprogram, a capacitor bank triggering subprogram named En_bank and a protection interrupt. Flowcharts of the main program and the subprogram En_bank are shown in Fig. 8(a) and Fig. 8(b).

After initialization, the program samples and measures the parameters. Then it step into the subprogram En-banks. If the

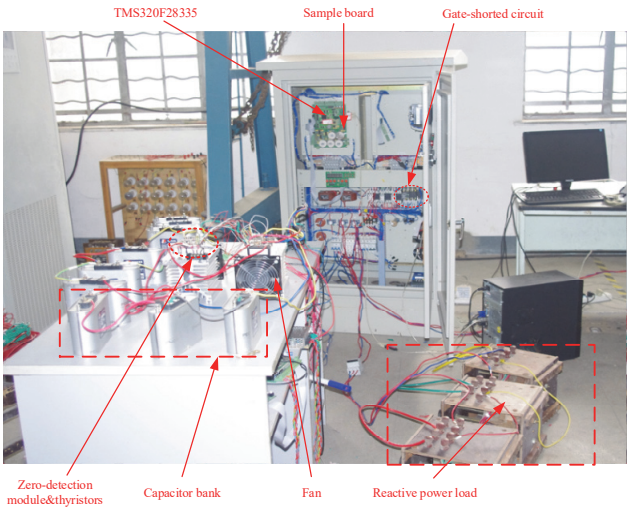
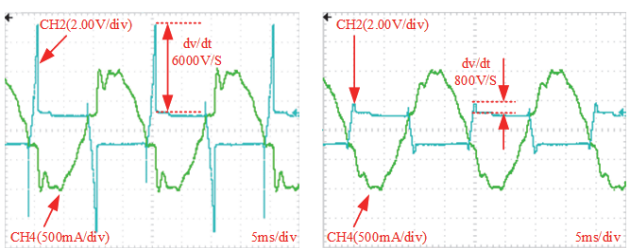


Fig. 9. TSC prototype with the improved trigger system.

TABLE I
PRACTICAL VALUES OF THE PARAMETERS

Parameter	Value
Power grid voltage	400V
Rated power of reactive load	4731var
The capacitance of each capacitor	39μF
Total number of the banks	3
Gate-shorted switch	MY2N-CR-J
Zero-detection module	MOC3083
DSP controller	TMS320F28335



(a) (b)

Fig. 10. Experimental results of the terminal voltage (CH1) and line current waves (CH4) of the TSC. (a) Without the improved trigger system. (b) With the improved trigger system.

main program finishes one loop, the interrupt Timer1 is enabled and the Flag is set to 0. Therefore, the cycle time of the main program is controlled to 1.667ms. The subprogram of En-banks loop executes all the time as shown in Fig. 8(b). In each loop, the subprogram completes the task as follows:

1) It displays some calculated parameters, such as the active power, system voltage, current of the compensating branches, etc.
2) In subprogram Cal_Banks, the number of capacitor banks is generated and the flag Flag_cut represents whether the compensating branches need to be removed from the grid system. The flag Flag_current presents the state of this branch.

If Flag_current is equal to 0, it is the first time to put the compensating branches into operation. In this case, the Zero-detection triggering module works. After the confirmation of the flag Flag_stable, which represents the operation state, the short-gated switch *S* can be turned on. If Flag_current keeps its value as 1, the current has already existed in the main loop and the short-gated switch S is kept turning on. In this case, the trigger signal of the zero-detection module can be marked.

IV. EXPERIMENT AND RESULTS

A. Experimental Parameters

A TSC prototype with the improved trigger system has been designed according to the former analysis, as shown in Fig. 9. Table I shows the values of the experimental parameters. The reactive load consists of a resistance of 14Ω connected in series with an inductance of 24mH in each phase. The capacitance of each power capacitor is 39μF and its rated voltage is 400V (phase voltage). The improved triggering structure consists of an Omron micro relay MY2N-CR-J and a zero-detection chip MOC3083. The microprocessor is a DSP TMS320F28335.

B. Experimental Results

To show the impact of the terminal voltage on current spikes, an experiment at a low voltage of 80V is conducted and the results are shown as Fig. 10(a) and Fig. 10(b).

Fig. 10(a) shows a waveform of a common TSC, while Fig. 10(b) shows a waveform of a TSC with the improved trigger system. Comparing Fig. 10(a) with Fig. 10(b), it is obvious that the voltage spike is significantly decreased, which is helpful for EMI mitigation. The current spike derived from the terminal voltage of the thyristor does have a remarkable influence on the waveform of the capacitor current. Fig. 10(a) shows that a thyristor triggered by a common device has a reverse voltage of 7V and that the process lasts almost 1ms. Fig. 10(b) shows that the spike of the terminal voltage is reduced to 1V by the improved trigger system. Furthermore, according to the pervious analysis in Equation (1) and Equation (2), the suppression of U_R and t_{rr} can significantly reduce the switching loss during the turning off period. It is significant that the age of the thyristor is longer when the heat of thyristor is reduced.

Without the improved trigger system, the THD of thyristors' terminal voltage is about 127.05% (relative to the fundamental), while the THD of the thyristors' current is about 27.11% (relative to the fundamental). When the improved trigger system is active, the THD of the thyristor's terminal voltage is reduced to about 49.36% (relative to the fundamental), while the THD of the thyristors' current is about 10.39% (relative to the fundamental). It is obvious that the improved trigger system is effective, and that the main harmonic components, 3rd, 5th, 7th, 9th and 11th have been significantly suppressed.

The field test results at the rated voltage (380V phase-phase) are also given in Fig. 15. Fig. 15(a) shows the thyristors'

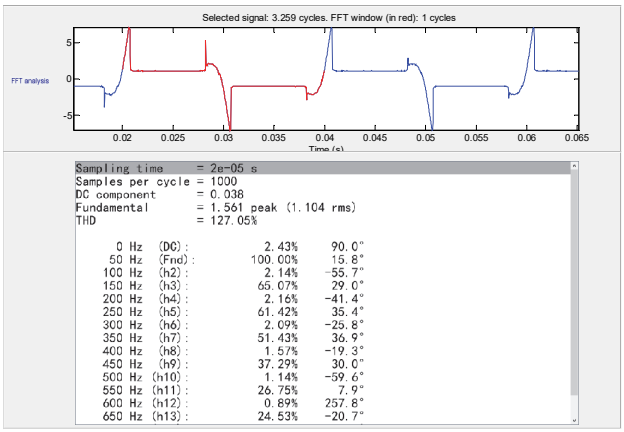


Fig. 11. Total Harmonic Distortion of the thyristor's terminal voltage without the improved trigger system.

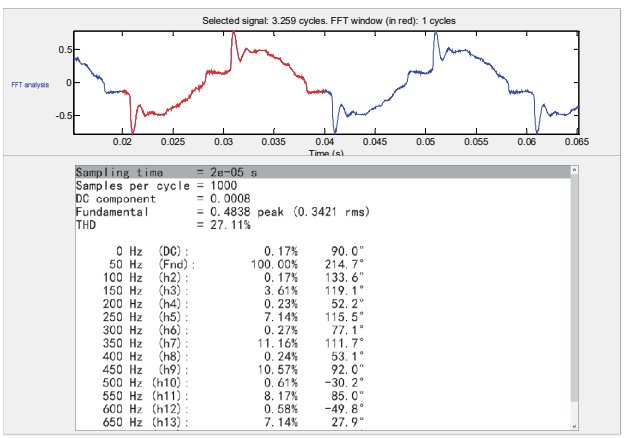


Fig. 12. Total Harmonic Distortion of the thyristor's line current without the improved trigger system.

TABLE II
TOTAL HARMONIC DISTORTION CONTRADISTINCTIONS OF THE EXPERIMENT TEST RESULTS

Parameter	Without	With
$\mathbf{THD_U}$	127.05%	49.36%
$\mathbf{THD_I}$	27.11%	10.39%

waveform without the improved trigger system, and Fig. 15(b) shows thyristor's waveform with the improved trigger system.

As shown in Fig. 15(a) and Fig. 15(b), when comparing the waveform of the TSC with and without the improved trigger system under the rated condition, the voltage spikes are significantly decreased.

Similarly, the Matlab FFT tool is also employed to analyse harmonic distortion. FFT results are shown in Fig. 16 to Fig. 19, and the THD contradistinction of the field test results are shown in TABLE III.

Without the improved trigger system, the THD (Total Harmonic Distortion) of the thyristors' terminal voltage is about 120.29% (relative to the fundamental), while the THD of the thyristor's current is about 6.52% (relative to the fundamental). When the improved trigger system is active, the

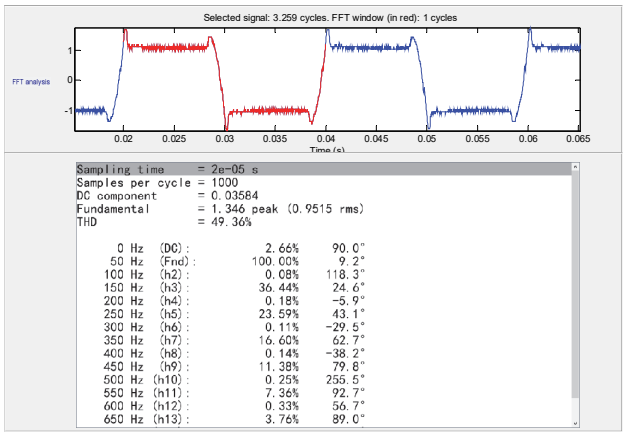


Fig. 13. Total Harmonic Distortion of the thyristor's terminal voltage with the improved trigger system.

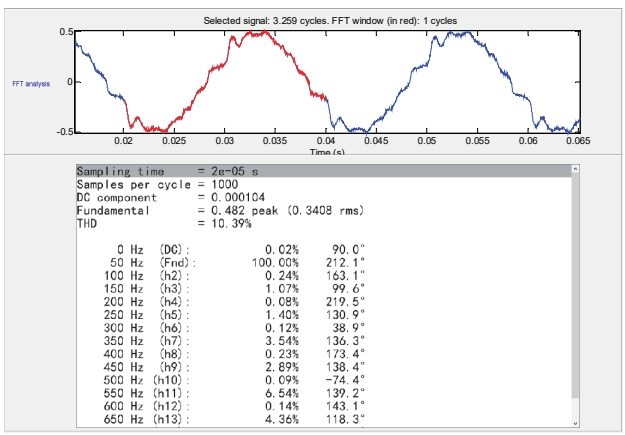
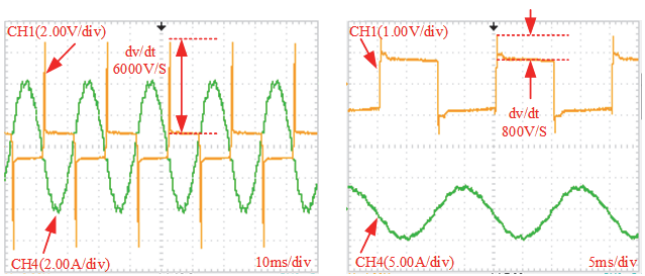


Fig. 14. Total Harmonic Distortion of the thyristor's line current with the improved trigger system.



(a) (b)

Fig. 15. Field test results of the terminal voltage (CH1) and line current waves (CH4) of the TSC. (a) Without the improved trigger system. (b) With the improved trigger system.

THD of the thyristor's terminal voltage is reduced to about 52.32% (relative to the fundamental), while the THD of the thyristor's current is about 5.45% (relative to the fundamental).

From these results, it is obvious that the improved trigger system is effective, and that the main harmonic component has been significantly suppressed.

The loss reduction is mainly based on a reduction of the voltage RMS. Seen from the contradistinction of the test results, the RMS of the fundamental component decreases when employing the improved trigger system when compared with

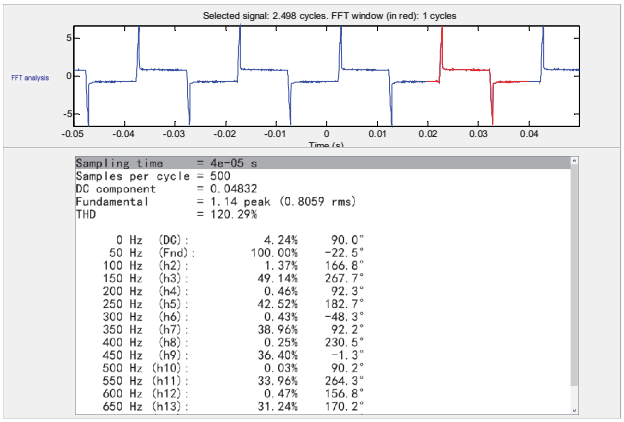


Fig. 16. Total Harmonic Distortion of the thyristors' terminal voltage without the improved trigger system in a field test.

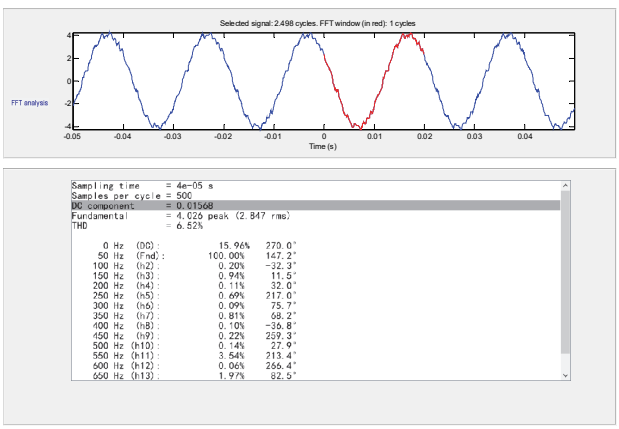


Fig. 17. Total Harmonic Distortion of the thyristors' line current without the improved trigger system in a field.

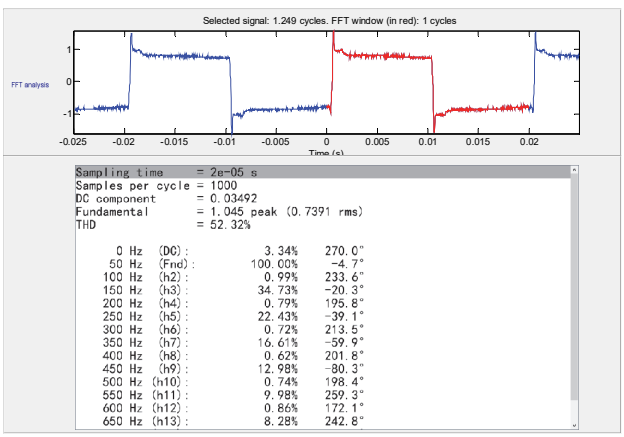


Fig. 18. Total Harmonic Distortion of the thyristors' terminal voltage without the improved trigger system in a field test.

TABLE III
TOTAL HARMONIC DISTORTION CONTRADISTINCTION OF FIELD TEST RESULTS

Parameter	Without	With
THD_U	120.29%	52.32%
THD_I	6.52%	5.45%

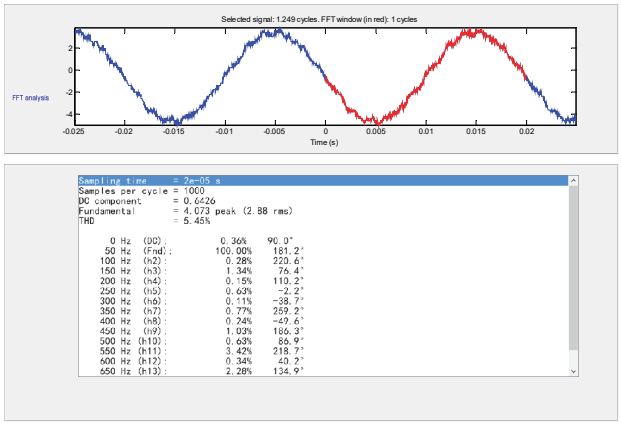


Fig. 19. Total Harmonic Distortion of the thyristors' line current with the improved trigger system in a field test.

the traditional solution. The loss caused by voltage spikes only occupies a minor proportion of the rated power. However, the thyristor device's operation current is large, and the device is usually under long-time operation. The integral of the voltage spike and the current's product is amazing. Thus, the loss reduction is considerable. Although the share of the current spike is small, it is a huge waste of resources when the devices are under the large current operation state for a long period of time. Using the improved trigger system can reduce the dv/di of high frequencies switch devices based on thyristors, which is helpful for EMI mitigation.

V. CONCLUSIONS

In this paper, a mathematical model of a thyristor is established based on the dynamic change of the terminal voltage. Mathematical analysis and experimental results indicate that the dynamic switching process is the principal cause of the current spikes in the SVC branch. Based on the mathematical derivation and results, an improved triggering system and a related control strategy are proposed. The results of a contrast experiment illustrate that the improved triggering module is an efficient method to suppress the current spikes caused by the dynamic switching process of a thyristor. Meanwhile, the switching loss under the power frequency can also be reduced. However, there are still some differences between the simulation results and the measured field data due to difficulties such as identifying stray parameters and the accuracy of the measuring instruments. Due to the TSC's high penetration and long-time steady operation in power systems, the improvement in the interference and energy consumption are of great significance. In the large-scale application of thyristor-switched devices, the suppression of voltage spikes demonstrates its unique advantages in terms of reducing the electromagnetic interference and the switching loss.

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